osmo-clock-gen - Feature #3856

Use SAMD21 instead of SAMD11

03/24/2019 10:32 AM - laforge

Status:	Resolved	**Start date:**	03/24/2019
Priority:	Normal	**Due date:**	
Assignee:	mschramm	**% Done:**	100%
Category:			
Target version:	hw-v2		

Description

The SAMD11 is a bit too constraining when it comes to computing the PLL parameters / register values for the Si5351C. Let's upgrade to a SAMD21 to get more flash + RAM.

History

#1 - 03/24/2019 10:39 AM - laforge

- Target version set to hw-v2

#2 - 04/06/2019 04:48 PM - laforge

- Status changed from New to In Progress

- % Done changed from 0 to 10

Likely candidate ATSAMD21E18A-MUT in QFN32

#3 - 05/08/2019 03:14 PM - laforge

- Status changed from In Progress to Stalled

- Assignee changed from laforge to mschramm

I have an incomplete branch in laforge/wip branch, but won't have time to continue this at the moment. Asking mschramm to take over

#4 - 05/15/2019 07:02 PM - mschramm

- Status changed from Stalled to In Progress

- % Done changed from 10 to 30

SAM D21E inserted, proper supply connections ongoing. UEXT UART is now different from the one on the debug header (UEXT on SERCOM1; 2.5mm jack and TagConnect UART on SERCOM3) - I think we must go on with a 4-layer-PCB, given the requested features #3858 and esp. #3857. #3905 only needs more PCB space and a header but must follow the other tasks, as the pins needed for #3857 have priority.

#5 - 05/29/2019 07:45 PM - mschramm

- Status changed from In Progress to Resolved

- % Done changed from 30 to 100

design of v2 done