128K x 8 Bit CMOS Flash Memory

FEATURES

- Fast Read Access Time: 90ns
- Single 5 Voltage Supply
- 128 Byte Page Write Operation
  - Single TTL Level Write Signal
  - Latched Address and Data
  - Automatic Write Timing
  - Automatic Page Erase Before Write
- Fast Write Cycle Time
  - Page Write Time: 10ms
  - Chip Erase Time: 10ms
- Low Power Dissipation
  - 100μA: Standby (max)
  - 40mA: Operating (max)
- Hardware and Software Data Protection
- $\overline{\text{Data}}$ Polling and Toggle Bit
- Reliable CMOS Floating-Gate Technology
  - Endurance: 100,000
  - Data Retention: 10 Years
- JEDEC Standard Byte-wide Pinout
  - 32-Pin DIP/PLCC/TSOP1

GENERAL DESCRIPTION

The KM29C010 is a 131,072×8 bit Flash Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

Writing data into the KM29C010 is very simple. Writing the KM29C010 is performed on a page basis; 128 bytes of data are loaded into the page buffer and then simultaneously written into the array.

The KM29C010 features $\overline{\text{Data}}$ polling and Toggle bit schemes that signal the processor an early completion of a write cycle without requiring any external hardware.

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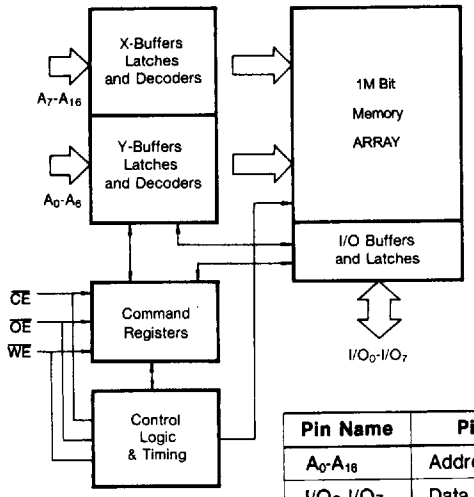
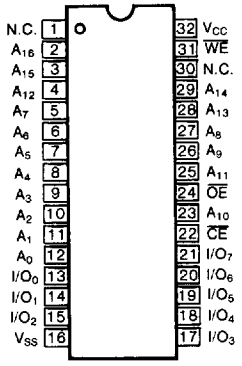
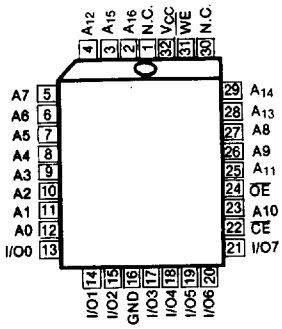
BLOCK DIAGRAM



PIN CONFIGURATION

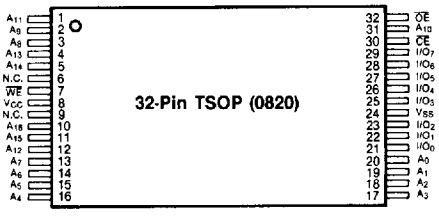


KM29C010



KM29C010J

Pin Name	Pin Function
A_0-A_{16}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
N.C.	No Connection*
V_{CC}	+5V
GND	Ground



KM29C010T

* Don't Care

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Short Circuit Output Current	I_{OS}	5	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Note: Voltage reference to V_{SS}, T_A=0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, all addresses* (Note 1)	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}$=V_{IH}, all I/O's=open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}$=V_{CC}−0.2, all I/O's=open	—	100	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to 5.5V	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0		V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 8.4MHz.
2. V_{IL}(min) = −3.0V for ≤10ns Pulse.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1.0 MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IO}=0V	—	6	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{DATA}$-Polling	$I/O_7=\overline{D_7}$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
L	L	H	Toggle Bit	I/O_6	Active
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

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AC CHARACTERISTICS

Note: $T_A=0°C$ to $70°C$, $V_{CC}=5V\pm10\%$, unless otherwise noted.

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L=100pF$

READ CYCLE

Parameter	Symbol	KM29C010-09*		KM29C010-10		KM29C010-12		KM29C010-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		100		120		150		ns
Chip Enable Access Time	t_{CE}		90		100		120		150	ns
Address Access Time	t_{AA}		90		100		120		150	ns
Output Enable Access Time	t_{OE}		40		40		50		60	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	30	0	30	0	40	0	50	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns

*Preliminary Product

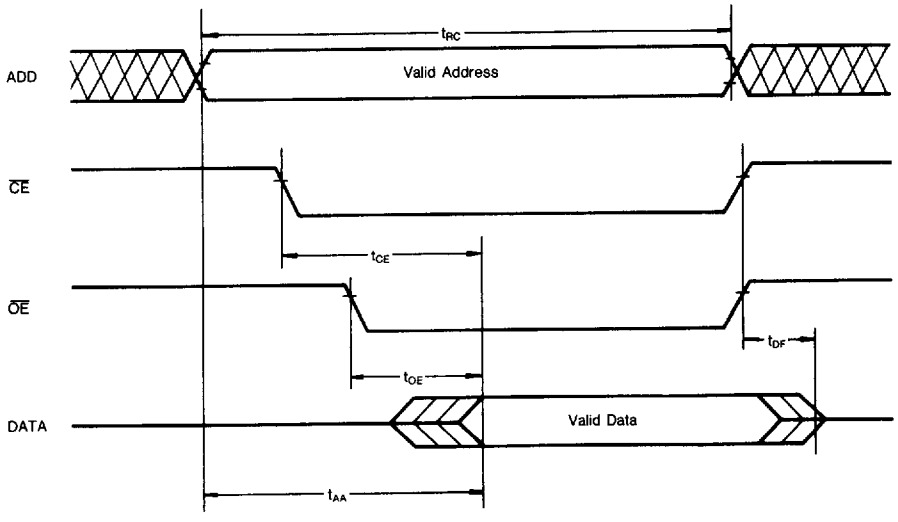
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}		10	ms
Address Set-Up Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
Write Set-Up Time	t_{CS}	0	—	ns
Write Hold Time	t_{CH}	0	—	ns
$\overline{CE}$ Pulse Width	t_{CW}	90	—	ns
Output Enable Set-Up Time	t_{OES}	0	—	ns
Output Enable Hold Time	t_{OEH}	0	—	ns
$\overline{WE}$ Pulse Width	t_{WP}	90	—	ns
Data Set-Up Time	t_{DS}	50	—	ns
Data Hold Time	t_{DH}	0	—	ns
Byte Load Cycle Time	t_{BLC}	0.1	150	μs
Last Byte Loaded to Data Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a raising edge of $\overline{WE}$.

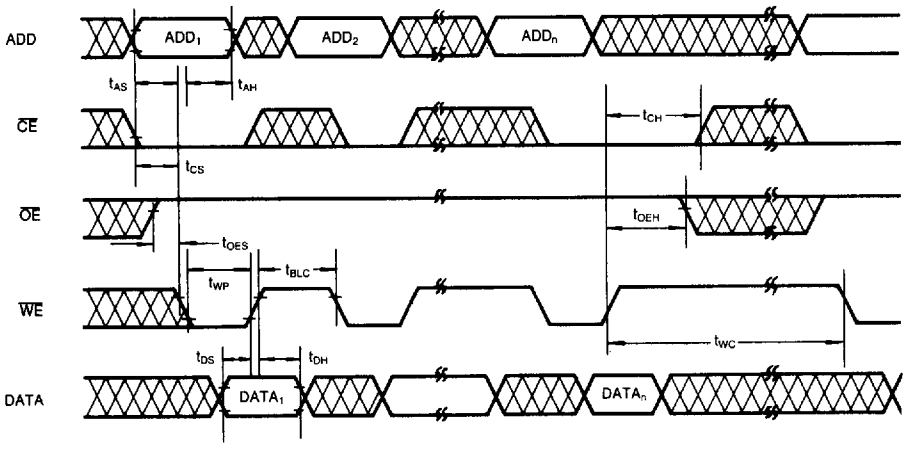
TIMING DIAGRAMS

READ CYCLE ($\overline{WE}$=V_{IH})

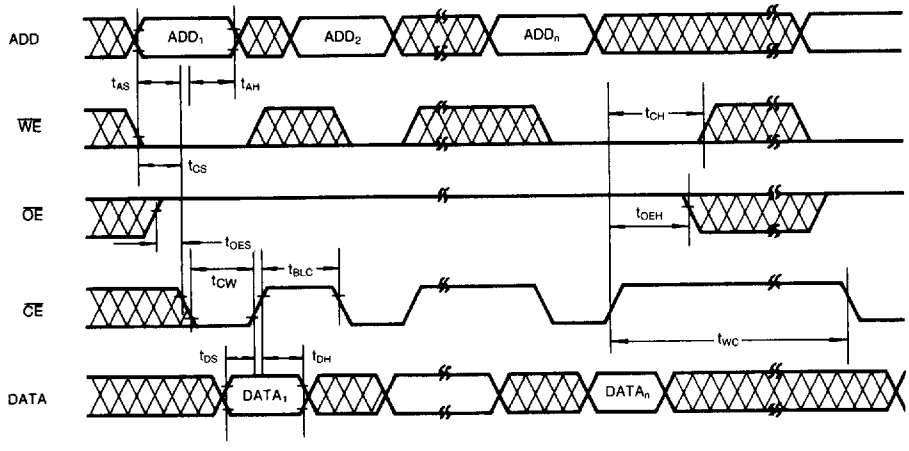


TIMING DIAGRAM (Continued)

PAGE PROGRAM CYCLE ($\overline{WE}$ Controlled Write Cycle)

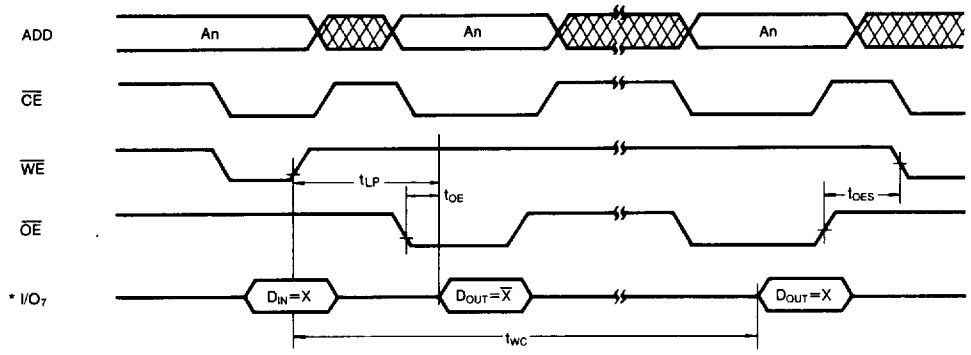


PAGE PROGRAM CYCLE ($\overline{CE}$ Controlled Write Cycle)



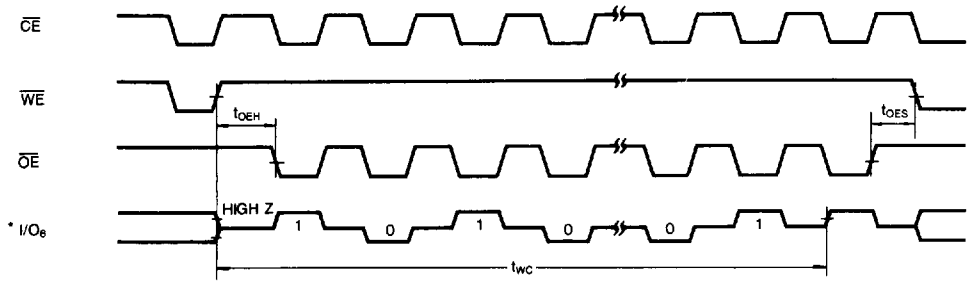
TIMING DIAGRAMS (Continued)

DATA POLLING CYCLE



* During the write cycle, I/O_7 will produce an inverted data of the last I/O_7 data, loaded into the Flash.

TOGGLE BIT CYCLE



*During the write cycle, I/O_6 will toggle between '1' and '0'

DEVICE OPERATION

READ

Reading data from the KM29C010 is similar to reading data from a SRAM. Read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high a read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

STANDBY

Current consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and $I/O_0 \sim I/O_7$ are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA LOADING

A byte load is performed by appling a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low and $\overline{OE}$ high. On each $\overline{WE}$, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_6) order and can be renewed in a data loading period.

PAGE WRITE

The KM29C010 is renewed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the write of its page will be erased to read data FFh. Once the bytes of a page are loaded into the device, they are simultaneously written during the internal write period. After the first byte data have been loaded into the device, successive bytes are entered in the same manner.

The nonvolatile write starts if $\overline{WE}$ stay high for the least t_{BLC} maximum (150μs) after the last $\overline{WE}$ low to high transition. The page address for the nonvolatile write is the "X" address ($A_7 \sim A_{16}$) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase period and a program cycle. During the erase period, the existing data of the locations being addressed during the loading period are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page.

The KM29C010 also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM29C010 to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM29C010 has a protection feature against $\overline{WE}$ noises; a $\overline{WE}$ noise the width of which shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when Vcc is less than V_{WI}=3.0V(min), the write inhibit Vcc level. During power-up, the KM29C010 automatically prevents any write operation for a period of 10ms(max.) after Vcc reaches the V_{WI} level. This will protect the chip from a false write during power up transiention. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit from inadvertent writings.

** SOFTWARE DATA PROTECTION **

The KM29C010 has the JEDEC standard software data protection scheme for enhanced protection of stored data.

The shceme does not affect normal write operation if it is not enabled through a SDP enable software algorithm. The protection mode can be enabled by executing short SDP enable software alogrithm, followed by a page write operation. Once the protection mode is enabled, the KM29C010 will not write any data if the SDP enable software algorithm is not proceded. The data protection function can be disabled by excuting a SDP disable software algorithm. Power transitions will not reset the SDP-feature. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

DATA POLLING

The KM29C010 features $\overline{DATA}$-polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. During the write period, any attempt to read of the last byte loaded the EEPROM will produce, at I/O_7, an inverted data of the last I/O_7 data loaded into the EEPROM. True data will be produced at all I/O's once the write cycle has been completed.

TOGGLE BIT

The KM29C010 also provides toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, subsequent attempts to read the EEPROM will toggle I/O_6 from "1" to "0" and "0" to "1". Once the write cycle is complete, the toggling will stop and valid data will be read.

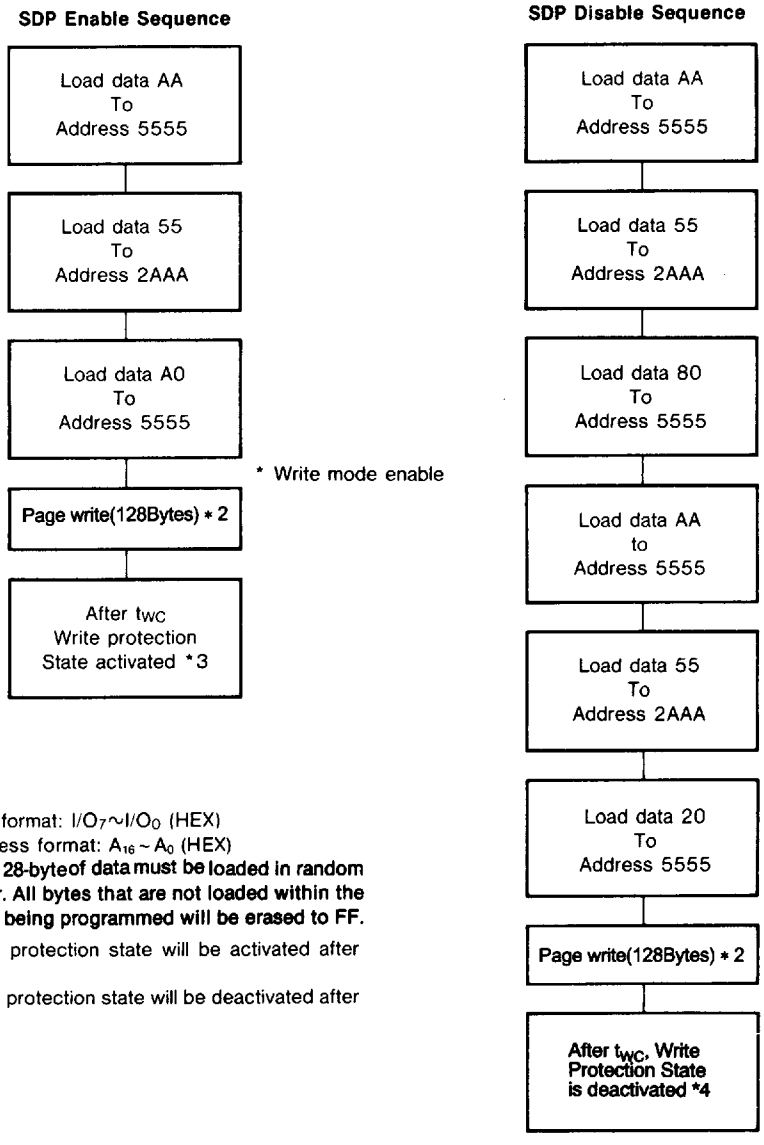
ENDURANCE AND DATA RETENTION

The KM29C010 is designed for applications requiring up to 100,000 write cycles per page and ten years of data retention. This means that each bit can be reliably written 100,000 times without degrading device opera-

DEVICE OPERATION (Continued)

tion, and this device features an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in 32 bits. And hence, significant improvements in the endurance and data retention characteristics are achieved.

SOFTWARE DATA PROTECTION ALGORITHM *1



Note 1. Data format: $I/O_7 \sim I/O_0$ (HEX)
Address format: $A_{16} \sim A_0$ (HEX)

2. 1 to 128-byteof data must be loaded in random order. All bytes that are not loaded within the page being programmed will be erased to FF.
3. Write protection state will be activated after twc.
4. Write protection state will be deactivated after twc.

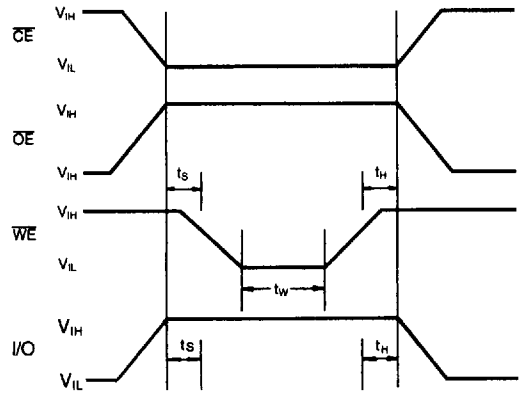
SOFTWARE CHIP ERASE

The KM29C010 may be erased at one time by using a six byte software command code. The erase code consists of six byte load commands to specific address location and specific data patterns. Once the code has been entered the device will set each byte to the high state (FFh). After the software chip erase has been initiated, the device will internally auto-timed the erase operation so that external clocks are not required.

HIGH VOLTAGE CHIP ERASE

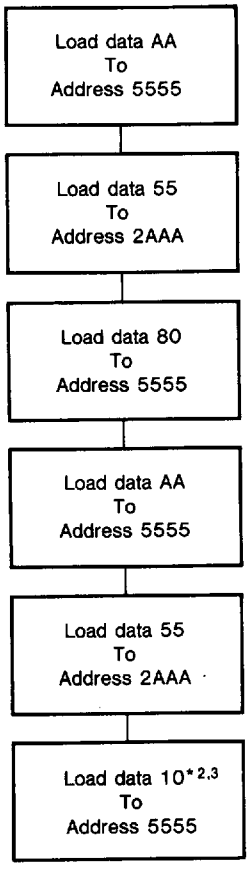
The contents of the KM29C010 may be set to the high state (FFh) by using an externally timed high voltage operation. $\overline{OE}$ is first raised to 12 volts with $\overline{CE}$ low and $\overline{WE}$ high: When $\overline{WE}$ pulsed low for a minimum of 10ms, the contents of the KM29C010 is erased.

HIGH VOLTAGE CHIP ERASE WAVEFORMS



$t_S = t_H = 5\mu sec$ (min)
$t_W = 10msec$ (min)
$V_H = 12.0V$

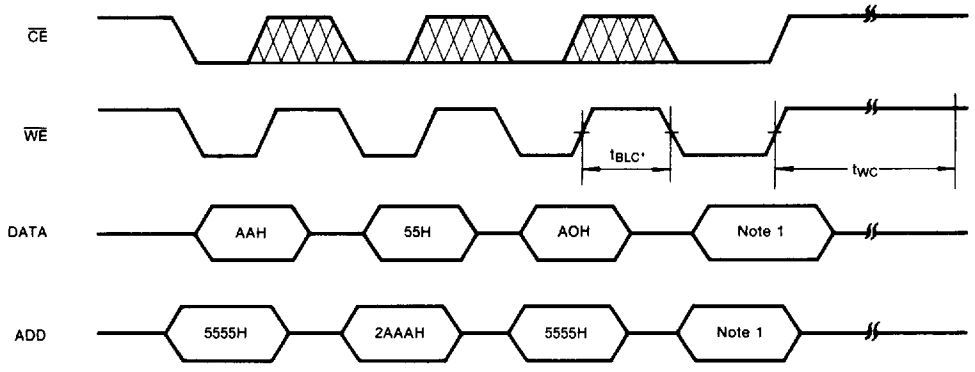
SOFTWARE CHIP ERASE ALGORITHM*1



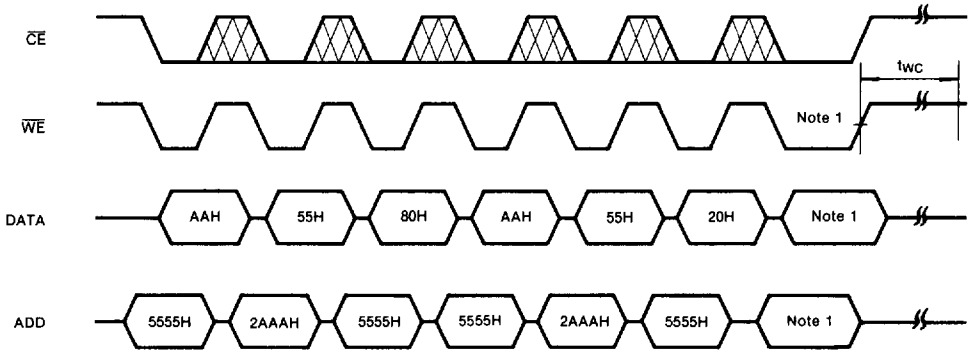
Notes for software ship erase code;
1. Data format: $I/O_7 \sim I/O_0$ (Hex.)
   Address format: $A_{14} \sim A_0$ (Hex.)
2. Data polling may be used to determine the end of the erase cycle by checking any address for data equal to FFh.
3. After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within twc.

TIMING DIAGRAM OF SOFTWARE DATA PROTECTION

SDP ENABLE TIMING SEQUENCE



SDP DISABLE TIMING SEQUENCE



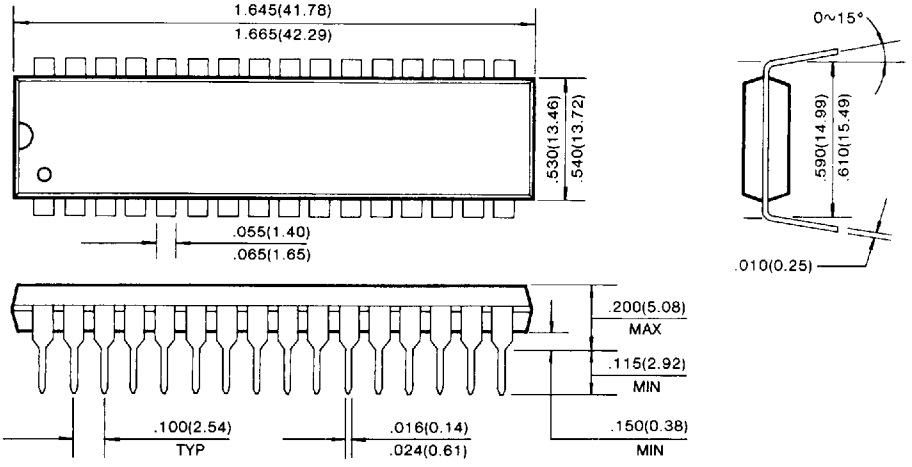
* $\leqslant t_{BLC}$ max.

Note 1: 1 to 128 byte to data maybe loaded in random order.

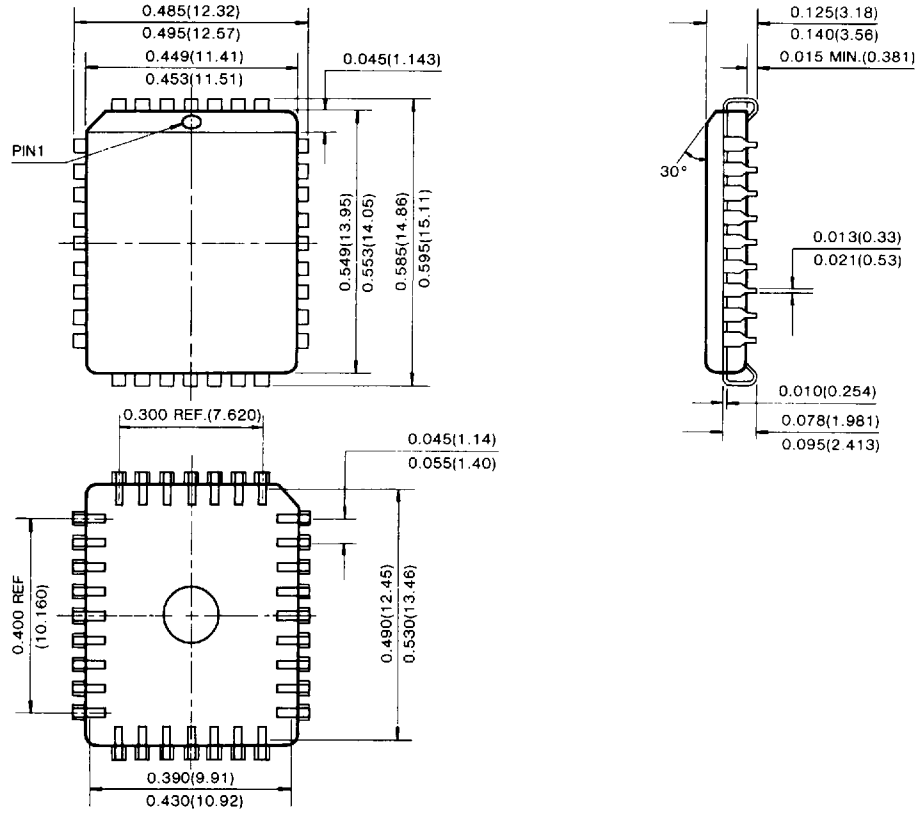
PACKAGE DIEMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER



32 PIN THIN SMALL OUTINE PACKAGE (Forward Type)

Unit: Inches (millimeters)