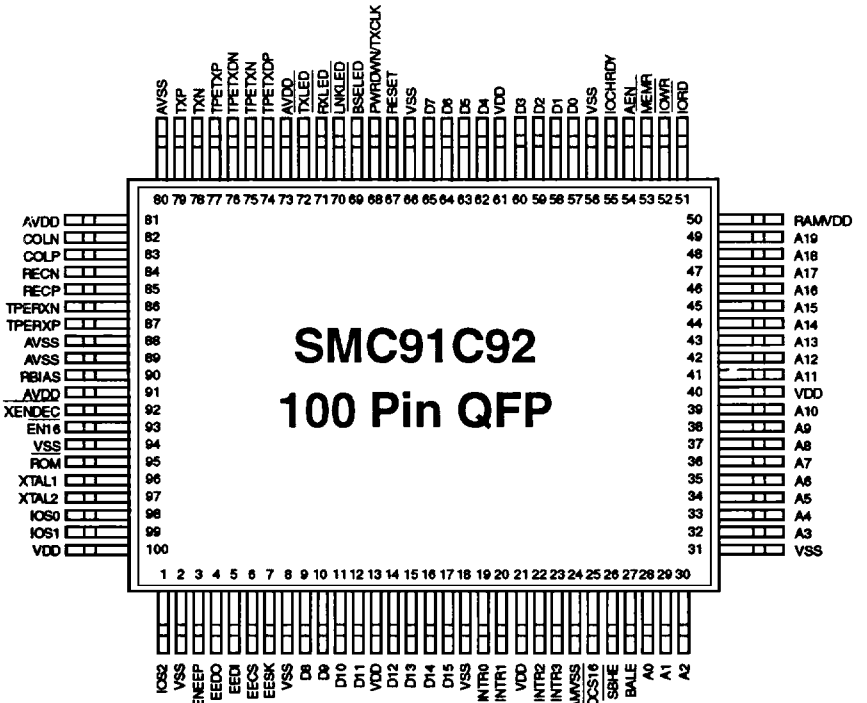
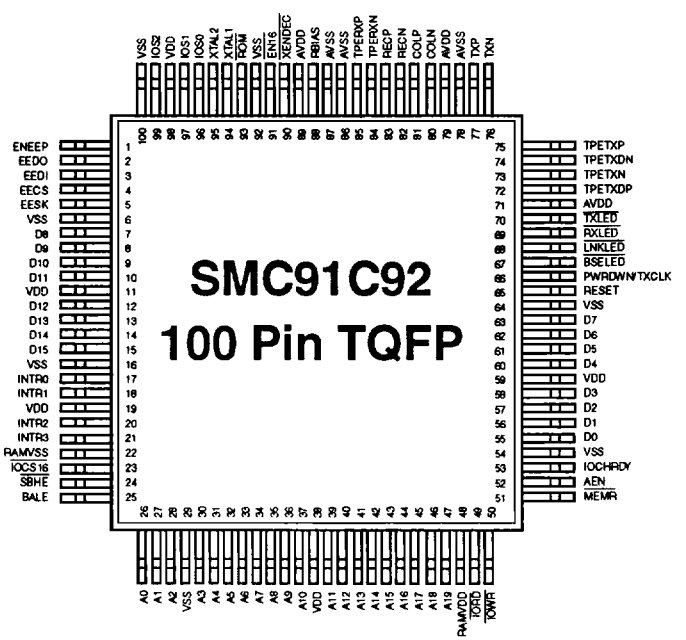
PIN CONFIGURATION





to any of its registers, including its packet memory. The SMC91C92 does not use any DMA services, virtually decoupling network traffic from local or system bus utilization. For packet memory management, the SMC91C92 integrates a unique hardware Memory Management Unit (MMU) with enhanced performance and decreased software overhead. The MMU provides better performance than ring buffers or linked lists. The SMC91C92 is portable to different CPU and bus platforms due to its flexible bus interface, flat memory structure (no pointers), and its loosely coupled buffered architecture (not sensitive to latency).

OVERVIEW

Unlike SMC91C92, LAN controllers typically fall into fixed access, ring buffer or linked list memory structures.

Fixed access areas are the simplest to access but generally offer little flexibility and performance, limiting the controller to handling one packet at a time and then requiring CPU intervention.

Ring buffers allow queuing of packets, but suffer from memory fragmentation problems, out of order removal/addition problems, and are inflexible when it comes to moving packets between receive and transmit areas.

Linked lists are highly flexible, but impose a high software overhead, and do waste memory resources for the purpose of implementing the multi-level lists.

A unique architecture allows the SMC91C92 to combine high performance, flexibility, high integration and simple software interface.

The MMU (Memory Management Unit) architecture used by the SMC91C92 combines the simplicity and low overhead of fixed areas with the flexibility of linked lists, and its performance exceeds the performance of the other methods.

Packet reception and transmission are determined by memory availability. All other resources are always available if memory is available. To complement this flexible architecture, all ISA bus interface functions are incorporated in the SMC91C92, as well as a 4608 byte packet RAM and serial EEPROM-based setup. The user can select or modify configuration choices.

The SMC91C92 integrates most of the 802.3 functionality, incorporating the MAC layer protocol, the physical layer encoding and decoding functions with the ability to handle the three pair AUI interface. For twisted pair networks, the integration goes beyond that, and integrates the twisted pair transceiver as well as the link integrity test functions.

The SMC91C92 is a true 10BASE-T single chip able to interface a system or a local bus.

Installation and Run-time diagnostics are provided with directly-driven LEDs. 802.3 statistics gathering capabilities are also provided to facilitate network management.

The SMC91C92 offers:

- High integration:
  - Single chip adapter including:
    - Packet RAM
    - ISA bus interface
    - EEPROM interface
    - Encoder decoder with AUI interface
    - 10BASE-T transceiver

High performance:

Back-to-back packet handling with no CPU intervention:

Queues transmit packets

Queues receive packets

Stores results in memory along with packet

Queues interrupts

Optional single interrupt upon completion of transmit chain.

Fast block move operation for load/unload:

CPU sees packets bytes as if stored contiguously.

Handles 16 bit transfers regardless of address alignment.

Access to packet through fixed window.

Fast bus interface:

Compatible with ISA type and faster buses.

Flexibility:

Flexible packet and header processing:

Can access any byte in the packet.

Can immediately remove undesired packets from queue.

Can move packets from receive to transmit queue.

Can alter receive processing order without copying data.

Can discard or enqueue again a failed transmission.

Resource allocation:

Memory dynamically allocated for transmit and receive.

Can automatically release memory on successful transmission.

Configuration:

Uses non-volatile jumperless setup via serial EEPROM.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
QFP	TQFP				
57-60 62-65 9-12 14-17	55-58 60-63 7-10 12-15	Data Bus	D0-D15	I/O24	Input/Output. 16 bit data bus used to access the SMC91C92 internal registers and buffer memory. Data bus has weak internal pullups. The data bus can be directly connected to the system data bus without additional buffering.
28-30 32-39 41-49	26-28 30-37 39-47	Address	A0-A19	I	Input. Address lines used to determine the SMC91C92 I/O location being accessed. Also used for external ROM support through the SMC91C92.
67	65	Reset	RESET	IS	Input. Active high reset. This input is not considered active unless it is high for at least 100ns.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
QFP	TQFP				
19, 20, 22, 23	17, 18, 20, 21	Interrupts	INTR0-3	O24	Outputs. Active high signals produced when an enabled interrupt condition occurs. Only one of them is selected to be used; the other three are tri-stated. The interrupt selected is determined by the value of INT SEL1-0 bits in the Configuration Register.
54	52	Address Enable	AEN	I	Input. Used as I/O address qualifier. I/O address decode is only enabled when AEN is low.
27	25	Address Latch	BALE	ISP	Input. The falling edge of this input is internally used to latch address lines and $\overline{SBHE}$. Transparent latches are used to enable valid decodes as early as possible. Schmitt trigger input with internal pullup.
51	49	$\overline{I/O\ Read}$	$\overline{IORD}$	IS	Input. Active low signal used by the host processor to read the SMC91C92 registers. Schmitt trigger input.
52	50	$\overline{I/O\ Write}$	$\overline{IOWR}$	IS	Input. Active low signal used by the host processor to write into the SMC91C92 registers. Schmitt trigger input.
53	51	$\overline{Memory\ Read}$	$\overline{MEMR}$	ISP	Input. Active low signal used by the host processor to read from the external ROM. Schmitt trigger input with internal pullup.
55	53	Ready	IOCHRDY	OD24	Output. Optionally used by the SMC91C92 to extend host cycles.
95	93	$\overline{ROM\ Select}$	$\overline{ROM}$	O4	Output. Active low signal used to enable an external eight bit wide ROM. This output can only go active when the $\overline{MEMR}$ input is low and the address bus contains a valid ROM address.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
QFP	TQFP				
25	23	I/O 16	IOCS16	OD24	Output. Active low signal indicating to the system that the present data transfer is a 16 bit I/O cycle. Addresses A15-A4 and AEN are used to generate it. This is an open drain output with 24 mA current sink.
26	24	Byte High	SBHE	I	Input. When low, indicates a transfer of data on the upper byte of the data bus.
98, 99, 1	96, 97, 99	I/O Base	IOS0-IOS2	IP	Input. External switches connected to these inputs determine the EEPROM area to be used for SETUP as a way of providing multiple installation options. These inputs have internal pullups.
72	70	Transmit LED	TXLED	OD16	Transmit LED output when XENDEC = 1.
		Transmit Enable	TXEN	O162	Active low Transmit Enable output to external ENDEC when XENDEC = 0.
69	67	Board Select LED	BSELED	OD16	Board Select LED output when XENDEC = 1.
			RXD	IP	NRZ receive data input from external ENDEC when XENDEC = 0.
71	69	Receive LED	RXLED	OD16	Receive LED output when XENDEC = 1.
		Receive Clock	RXCLK	IP	Receive clock from external ENDEC when XENDEC = 0.
70	68	Link LED	LNKLED	OD16	Link LED output when XENDEC = 1.
			TXD	O162	NRZ transmit data output to external ENDEC when XENDEC = 0.
3	1	Enable EEPROM	ENEEP	IP	Input. This active high input enables the EEPROM to be read or written by the SMC91C92. Internally pulled up. Must be grounded if no EEPROM is connected to the SMC91C92.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
QFP	TQFP				
90	88	Bias Resistor	RBIAS	Analog Input	A bias resistor is connected between this pin and ground. Nominal value is 22 kohm 1%.
96 97	94 95	Crystal 1 Crystal 2	XTAL1 XTAL2	I_{CLK}	An external 20 MHz crystal should be connected across these pins. If an external 20 MHz TTL clock is used instead, it should be connected to XTAL1 with a 390 ohm pullup and XTAL2 should be left floating.
93	91	$\overline{\text{Enable 16 Bit}}$	$\overline{\text{EN16}}$	IP	Input. When low, the SMC91C92 is configured for 16 bit operation. Typically grounded using the AT bus extension ground. Internally pulled up, will stay high if there is no 16 bit extension (XT bus).
13, 21, 40, 50, 61, 100	11, 19, 38, 48, 59, 98	Power	VDD		+5V power supply pins.
2, 8, 18, 24, 31, 56, 66, 94	100, 6, 16, 22, 29, 54, 64, 92	Ground	VSS		Ground pins.
80, 88, 89	78, 86, 87	Analog Ground	AGND		Analog ground for ENDEC.
73, 81, 91	71, 79, 89	Analog Power	AVDD		Analog VDD for ENDEC.
85 84	83 82	AUI Receive	RECP RECN		Differential inputs. Line receivers connected to the AUI receive pair for carrier sensing and data recovery.
79 78	77 76	AUI Transmit	TXP/$\overline{\text{COLL}}$ TXN/$\overline{\text{CRS}}$		Differential outputs when $\overline{\text{XENDEC}}$ = 1. Connected to AUI transmit pair. Carries Manchester encoded transmit data. Externally pulled up by 150 ohm resistors. When $\overline{\text{XENDEC}}$ = 0, these pins are inputs from the external ENDEC used for collision detection and carrier sense functions.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
QFP	TQFP				
83 82	81 80	AUI Collision	COLP COLN		Differential inputs. Connected to AUI collision pair. A collision is indicated by a 10 MHz signal at this input pair.
87 86	85 84	TPE Receive	TPERXP TPERXN		Differential inputs. Receive pair from twisted pair.
77 75	75 73	TPE Transmit	TPETXP TPETXN		Differential outputs. Transmit pair to twisted pair.
74 76	72 74	TPE Transmit Delayed	TPETXDP TPETXDN		Differential outputs. Transmit pair delayed for pre-distortion purposes.
7	5	EEPROM Clock	EESK	O4	Output. 4 μsec clock used to shift data in and out of a serial EEPROM.
6	4	EEPROM Select	EECS	O4	Output. Used for selection and command framing of the serial EEPROM.
4	2	EEPROM Data Out	EEDO	O4	Output. Connected to the DI data input line of the serial EEPROM.
5	3	EEPROM Data In	EEDI	ID	Input. Connected to the DO data output line of the serial EEPROM.
92	90	$\overline{\text{External}}$ $\overline{\text{Endec}}$	$\overline{\text{XENDEC}}$	IP	Input. When tied low, expects an external encoder/decoder to be used with the SMC91C92. If high or left open, the internal encoder/decoder is used and all inputs from the external encoder/decoder are ignored. This pin has an internal pullup.
68	66	Transmit Clock	PWRDWN/ TXCLK	IP	Powerdown input. Keeps device in powerdown when high and $\overline{\text{XENDEC}}$ = high. When $\overline{\text{XENDEC}}$ = low, it carries transmit clock input.

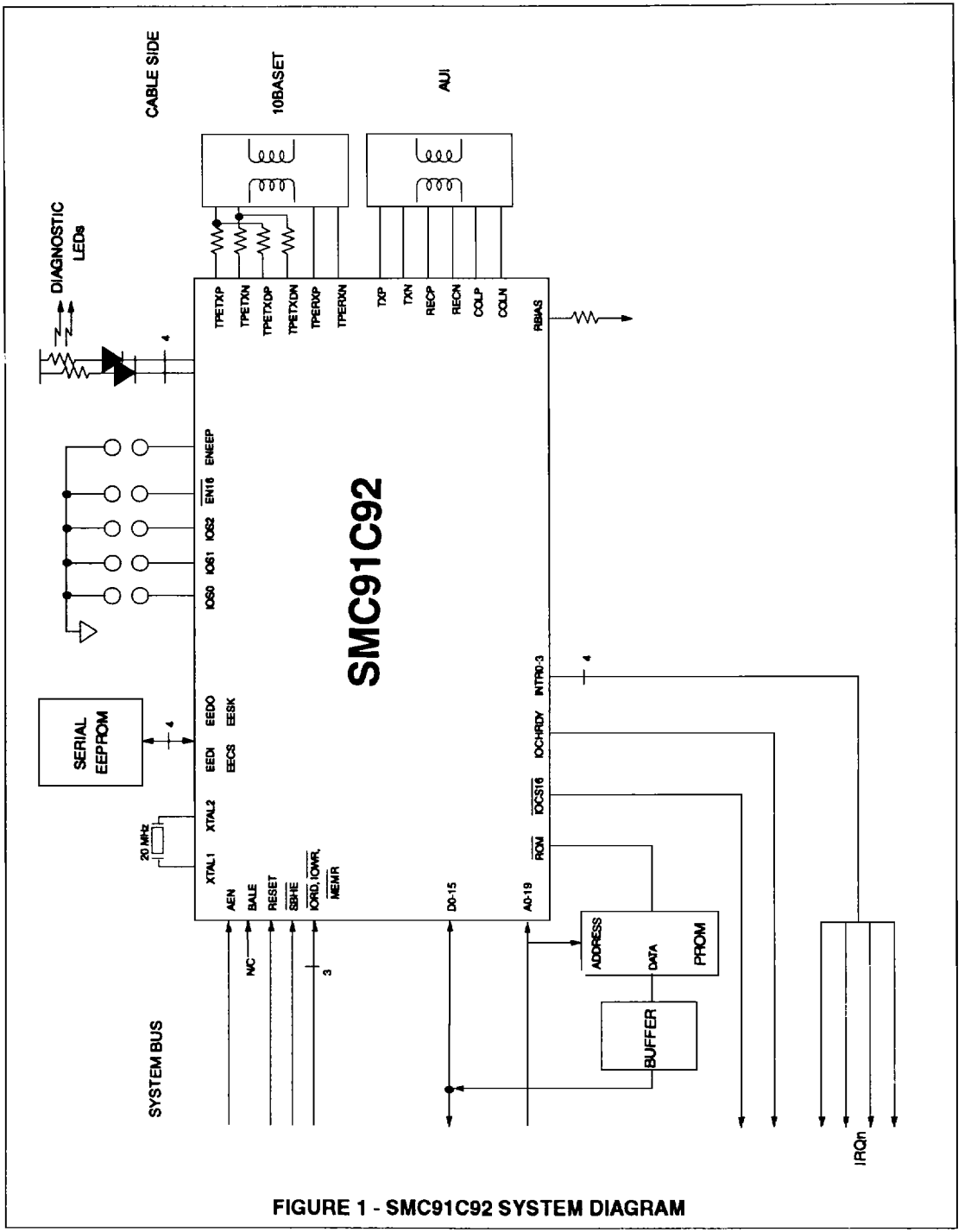


FIGURE 1 - SMC91C92 SYSTEM DIAGRAM

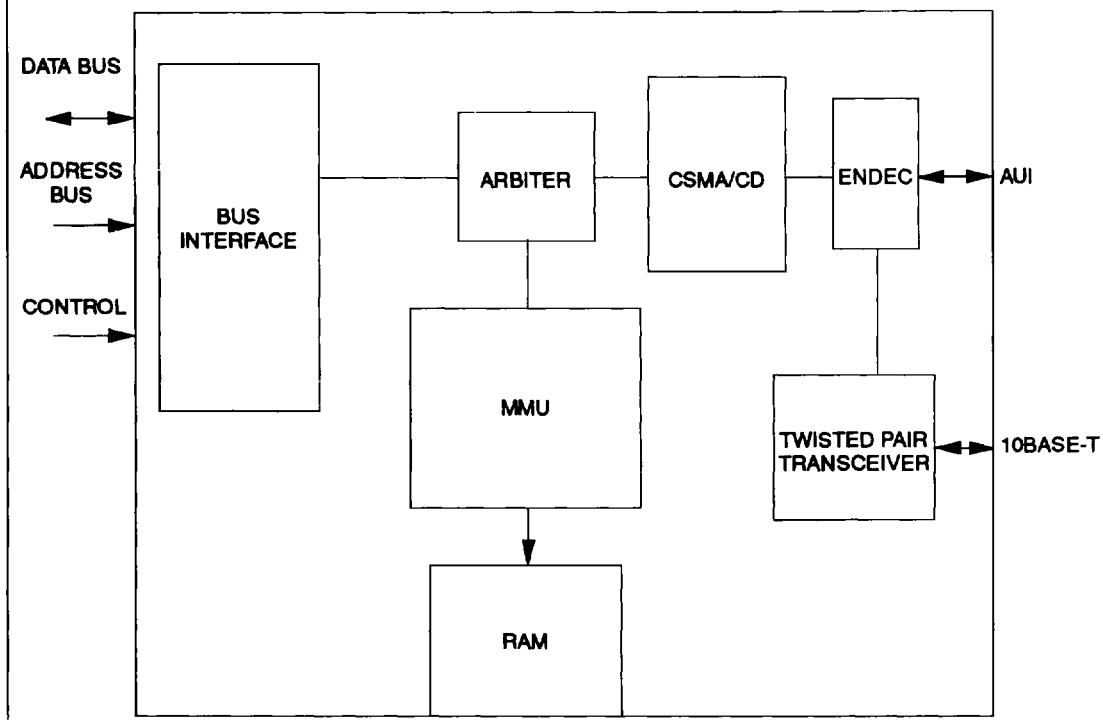


FIGURE 2 - SMC91C92 INTERNAL BLOCK DIAGRAM

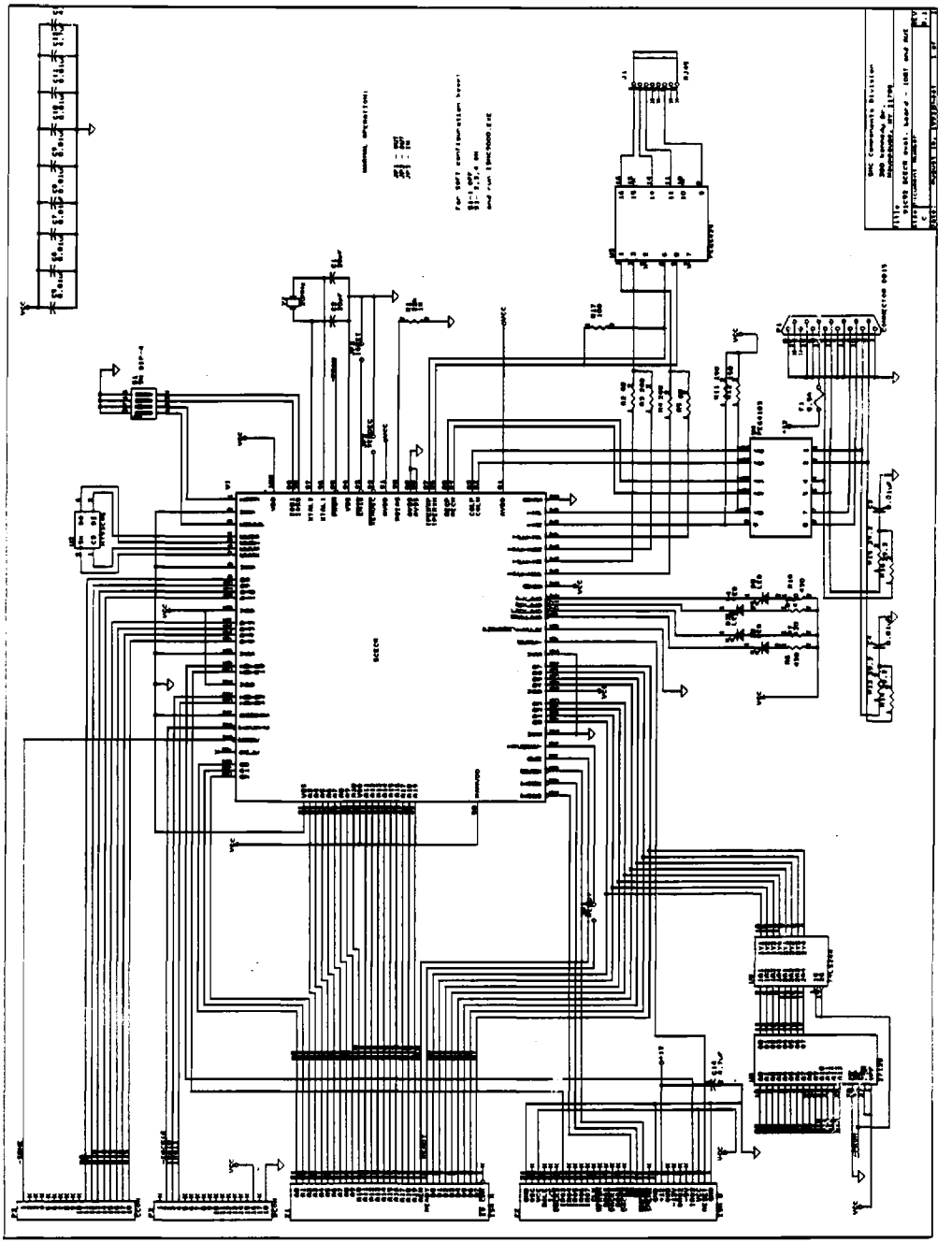


FIGURE 3A - SMC91C92 10BASE-T AND AUI SCHEMATIC

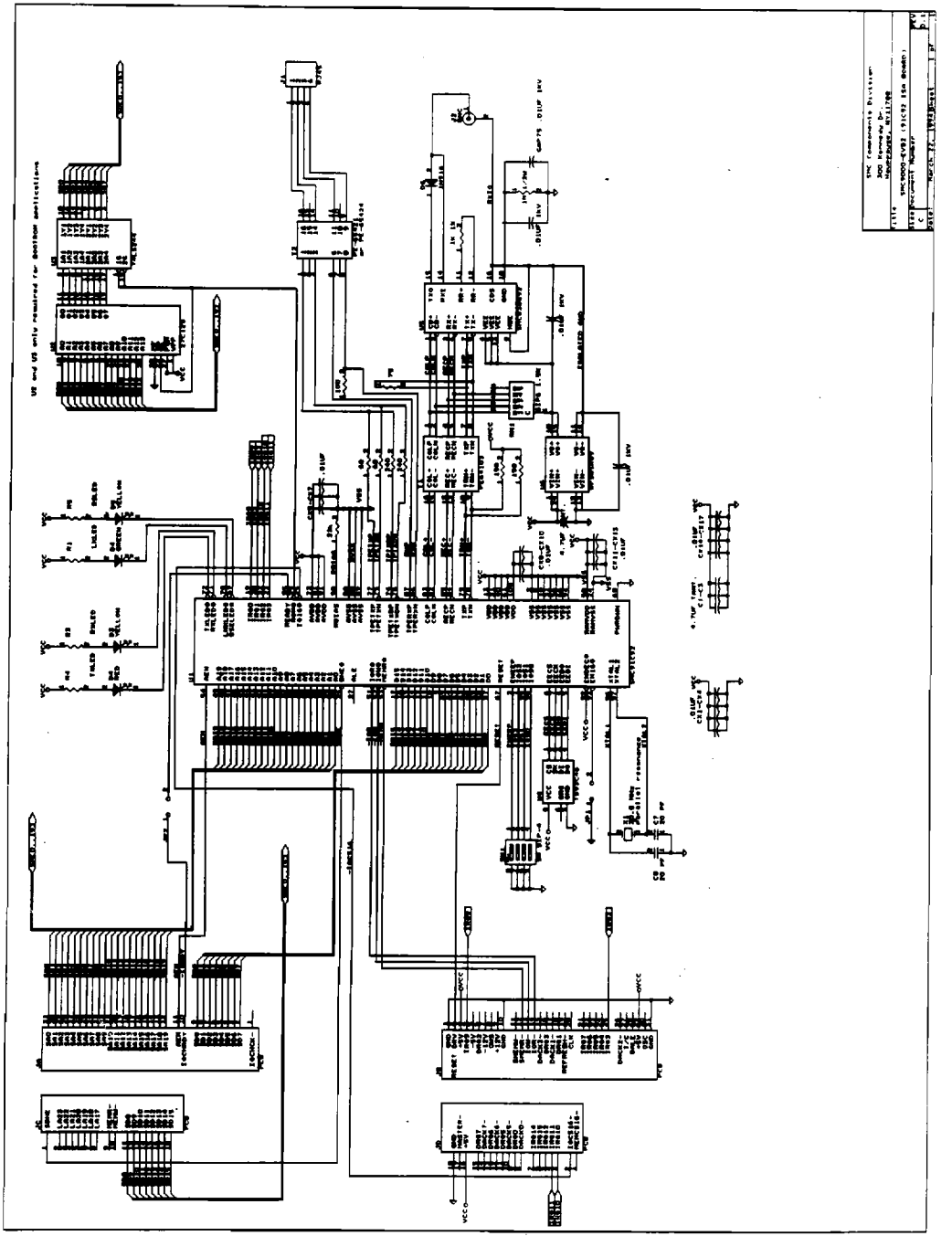


FIGURE 3B - SMC91C92 10BASE-T AND COAX SCHEMATIC