General Description

The PSB 2197, SmartLink-P, implements the subscriber access functions for a digital terminal to be connected to a two-wire U_{PN} interface.

The PSB 2197 SmartLink-P is an optimized device for TE applications, covering the complete layer-1 and basic layer-2 functions for digital terminals.

The PSB 2197 SmartLink-P combines the functions of the U_{PN} transceiver with reduced loop length (one channel of the OCTAT-P PEB 2096) and a simple HDLC controller for signaling data onto one chip.

A pulse width modulator is included to provide an LCD-contrast control or a ring tone signal.

The serial control port of the SmartLink-P is compatible to most serial interfaces of microcontrollers. In addition it provides the microcontroller clock signal as well as an undervoltage detector and reset generation including a watchdog function.

The Terminal Repeater function of the SmartLink-P allows to cascade two telephones which are controlled by one U_{PN} interface from the line card or to extend the loop length by using an IEC-Q transceiver.

The SmartLink-P can also be used as a simple HDLC controller which provides the TIC-bus access procedure. In this mode, the U_{PN} transceiver is inactive.

The PSB 2197 SmartLink-P interfaces to voice/data devices via the IOM-2 interface and provides an additional bit clock and strobe signal for standard codecs. The upstream B-channel information may be muted or loop back the downstream data.

The PSB 2197 SmartLink-P is a 1-micron CMOS device offered in a P-DSO-28 package. It operates from a single 5-V supply.

Note: U_{PN} in the document refers to a version of the U_{P0} standard with a reduced loop length.

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<th>Type</th>
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<td>PSB 2197-T</td>
<td>P-DSO-28-1 (SMD)</td>
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Features

- Cost/performance-optimized U_{PN} interface transceiver, compatible to PEB 2096 OCTAT-P or PSB 2196 ISAC-P TE
- HDLC controller with 2 × 4-byte FIFO per direction
- IOM-2 interface for terminal application including bit clock and strobe signal
- Uplink MUTE function
- Selective B-channel loop back
- Serial control port
- Pulse width output LCD-contrast control or ring tone generation
- CPU clock and reset output
- Watchdog timer
- Test loops
- Advanced CMOS technology
- Low power consumption: active: 100 mW max.
Block Diagram of the SmartLink-P TR-Mode

Block Diagram of the SmartLink-P TE-Mode