Enhanced Serial Communication Controller (ESCC2)

General Description
The Enhanced Serial Communication Controller ESCC2 (SAB 82532) is a multiprotocol data communication controller with two symmetrical serial channels. It has been designed to implement high speed communication links and to reduce hardware and software overhead needed for serial synchronous/asynchronous communications.

The version 82532N-10 of the ESCC2 opens a wide area for application which use time division multiplex methods (e.g. time-slot oriented PCM systems, systems designed for packet switching, ISDN applications).

General Features
Serial Interface
- Two independent full-duplex serial channels
  - On-chip clock generation or external clock source
  - On-chip DPLL for clock recovery of each channel
- Two independent baud rate generators
- Independent time-slot assignment for each channel with programmable time-slot length (1 - 256 bits)
- Async, sync character oriented (MONOSYNC/BISYNC) or HDLC/SDLC modes (including SDLC LOOP)
- Transparent receive/transmit of data bytes without framing
- NZR, NRZI, FM and Manchester encoding
- Modern control lines (RTS, CTS, CD)
- CRC support:
  - HDLC/SDLC: CRC-CCITT or CRC-32
  - (automatic handling for transmit/receive direction)
  - BISYNC: CRC-16 or CRC-CCITT
  - (support for transmit direction)
- Support of bus configuration by collision detection and resolution
- Statistical multiplexing
- Continuous transmission of 1 to 32 bytes possible
- Programmable preamble (8 bit) with selectable repetition rate (HDLC/SDLC and BISYNC)
- Data rate up to 10 Mbit/s
- Master clock mode with data rate up to 4 Mbit/s

Applications
- Universal, multiprotocol communication board for Workstation- and PC-boards
- Terminal controllers
- Computer peripherals
- Time-slotted packet networks
- Multimaster communication networks
- LANs

Protocol Support (HDLC / SDLC)
- Various types of protocol support depending on operating mode
  - Auto-mode (automatic handling of S- and I-frames)
  - Non-auto mode
  - Transparent mode
- Handling of bit oriented functions
- Support of LAPB / LAPD / SDLC / HDLC protocol in auto-mode (I- and S-frame handling)
- Modulo 8 or modulo 128 operation
- Programmable time-out and retry conditions
- Programmable maximum packet size checking

MP Interface and Ports
- 64-byte FIFOs per channel and direction (byte or word access)
- 8/16-bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte and word access)
- Efficient transfer of data blocks from/to system memory via DMA or interrupt request
- Support of Daisy Chaining and Slave Operation with Interrupt Vector generation
- 8-bit programmable bidirectional universal port

<table>
<thead>
<tr>
<th>Type</th>
<th>Package</th>
<th>Max. Data Rate Clocked</th>
<th>Time-Slot Mode</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>ext.</td>
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<tr>
<td></td>
<td></td>
<td>int.</td>
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<td></td>
<td></td>
<td>(DPLL)</td>
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<tr>
<td>SAB 82532-N</td>
<td>P-LCC-68-1</td>
<td>2 Mbit/s</td>
<td>no</td>
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<tr>
<td>SAB 82532-N-10</td>
<td>P-LCC-68-1</td>
<td>10 Mbit/s</td>
<td>yes</td>
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</tbody>
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Siemens Aktiengesellschaft
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