RL56CSMV/6

AnyPort™ Multi-Service Access Processor

The RL56CSMV/6 is a member of the Conexant™ AnyPort™ family of multi-service access processors, and provides a complete solution to the transport of multiple media types between circuit-switched remote access and a variety of back-end networks (Table 1). AnyPort processors are ideally suited for the network infrastructures resulting from the convergence of voice and data networking, addressing new requirements such as Voice and Fax over packet networks, ISDN and Cellular Data, while maintaining support of traditional PSTN Data/Fax needs.

The processor and data pumps use an internal core voltage of +2.5V, supplied by external pins (VCORE), for low power consumption.

The RL56CSMV/6 transcends existing modem solutions by providing a complete system solution for multi-service remote access. The combined DSP/RISC architecture provides an ideal engine to run Conexant's extensive suite of field-proven modulations, echo cancellers, voice coders, and communications protocols. In addition, performing functions such as T.38, V.120, async-to-sync HDLC conversion for PPP, V.110, and synchronous HDLC for PPP on ISDN connections, in the access processor allows system designers to reduce system overhead and increase scalability.

The RL56CSMV/6 is a low-power system providing six communication channels in a single package. Powerful and downloadable DSP-based data pumps employ on-chip SRAM to allow upgrades to future voice and communication modulation schemes. An advanced RISC microcontroller manages three dual data pumps simultaneously. An innovative host interface to the Multi-Service Access Processor system uses a shared SDRAM memory to increase data throughput while reducing system cost and space. A programmable time slot selection feature provides direct digital connection to a T1/E1/PRI framing device.

A 35mm BGA package houses the RL56CSMV/6 with extra balls available for thermal vias to minimize heat. A built-in phase lock loop (PLL) minimizes board noise while easing design. A quick-wake sleep mode further reduces power consumption on idle channels.

Features

Generic

- Six access channels in one package
- +3.3V/+2.5V operation with +5V tolerant inputs
- Downloadable controller firmware and data pump code
- Advanced RISC Machines (ARM) architecture
- Low-power sleep mode with quick wake
- Glueless interface to Conexant Bt8370 T1/E1/PRI framer with time slot selection
- Built-in phase lock loop (PLL)

Signaling

- DTMF detection and generation
- Multi-frequency tone support for legacy network equipment (R1 and R2)

Data

- Data modem modes
  - PSTN: ITU-T V.90, K56flex, K56Plus, V.34 (33.6 kbps), V.FC, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, and V.21; Bell 212A and 103
  - ISDN: 64/56 kbps ISDN Basic Rate Interface B Channel HDLC control, or data pass-through mode for HDLC processing elsewhere in the central site system
- Internal error correction and data compression (ECC)
  - V.42 LAPM and MNP 2-4 error correction
  - V.42 bis and MNP 5 data compression
  - MNP 10EC™ enhanced cellular
- Async/sync HDLC conversion
- V.120 ISDN data
- V.110 cellular data
- LAP-B X.75

Voice

- Baseline configuration:
  - G.723.1 and G.723.1 Annex A
  - G.711 µ-law and A-law
  - G.729 Annex A and Annex B
  - G.168 128 ms Network Echo Canceller
- Patented robust jitter buffer
- Voice API using Mailbox Messages

FAX

- Fax modem send and receive rates up to 33600 bps
- V.34, V.17, V.33, V.29, V.27 ter, and V.21 channel 2, Group 3, T.30 protocol and Class 1, 2 supported
- T.38 real-time fax protocol

Communications software-compatible AT commands

Table 1. RL56CSMV/6 Family Models and Functions

Model/Order/Part Numbers			Supported Interface/Functions			
Marketing Model Number	Part Number	Package	VCORE Pins	Data	Fax	Voice
RL56CSMV/6-35LP	R7181-34	371-Pin 35 mm BGA	+2.5V	Yes	Yes	Yes

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Technical Specifications

General Description

The RL56CSMV/6 provides the processing core for six channels of a central site Remote Access Server supporting high speed T1/E1/PRI digital lines. The OEM adds two oscillators, SDRAM, and discrete components to complete the Multi-Service Access Processor system.

The access processor includes a full-featured, self-contained data/fax/Voice modem solution shown in Figure 1. Data modem handshake, fax modem protocol, voice codecs, and ISDN data connection functions are supported and controlled through the AT command set.

Digital Data Pump (DDP)

The DDP is a +3.3V/+2.5V Conexant data pump supporting PSTN data/fax modem operation, ISDN B Channel call termination mode, and voice coding/decoding. The DDP executes internal code including downloadable modules from on-chip memory.

Digital data transfers serially between the T1/E1 framer device and the DDP at a data rate up to 8.192 Mbps. The T1/E1 framing device provides a strobe signal and the DDP TSA logic detects where the data for the channel starts in the serial TDM data stream using a programmable counter. The DDP performs PCM µ-law or A-law conversion and synchronizes with an external network clock.

ARM Microcontroller (MCU)

The ARM MCU performs the command processing and interfaces to the central site system controller via a 16-bit parallel host interface. Two 64-word deep FIFOs are used for improved data throughput between the access processor and system controller. This single powerful RISC processor controls six separate channels. A SDRAM loader is available to support download from the central site system controller on startup, if desired.

Access Processor Operation

In data modem modes, each channel can independently connect to PSTN data modems at rates up to 56 kbps or ISDN terminal adapters at rates up to 64 kbps. A downloadable architecture allows for software download. For PSTN modems, complete handshake and data rate negotiations are performed. By optimizing the modem configuration for line conditions, the DDP can connect at the highest data rate that the channel can support from 56 kbps to 300 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standard are supported. Asynchronous to synchronous conversion is supported inside the controller to ease PPP processing in PSTN data mode.

When the remote end is an ISDN terminal adapter, the RL56CSMV/6 provides HDLC control including HDLC Flag generation/detection, bit stuffing/extraction, and CRC generation/checking. V.120, V.110, and LAP-B X.75 are also supported. V.120 is a standard for encapsulating asynchronous data communications traffic into ISDN data streams.

In fax modem mode, the RL56CSMV/6 supports Group 3 facsimile send and receive speeds of 33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, and 2400 bps. Fax modem modes support T.30 and T.38 fax requirements. Fax data transmission and reception performed by the access processor are controlled and monitored through the EIA-578 Class 1 and Class 2 command interface. Both transmit and receive fax data are buffered within the access processor.

In Voice mode, the CSMV/6 encodes PCM audio data from the line into Real-Time Protocol (RTP) packets for the Host, and decodes RTP packets from the Host, to output PCM audio data to the line. In Voice mode, DTMF digits can be detected and transmitted, and a Voice Activity Detector can be enabled.

Access Processor Firmware

Access processor firmware performs processing of general modem control, command sets, error correction and data compression, fax class 1 and class 2, voice coding and decoding (optional), and central site system controller interface functions.

The firmware is provided in object code form for executing from external SDRAM after download on startup using the ROM-coded Boot Loader. Equipment designers can add their own functions in firmware using commonly available development tools and the C programming language.

Hardware Interface Signals

The RL56CSMV/6 interface is illustrated in Figure 2.

The 371-pin BGA package identifying pin locations for the RL56CSMV/6 is shown in Figure 3.

The RL56CSMV/6 pin signals in the 371-pin BGA are listed by location in Table 2 and by interface in Table 3.

The RL56CSMV/6 application signals are listed by interface in Table 4.

Additional Information

Additional information is described in the RL56CSMV/6 AnyPort Multi-Service Access Processor Hardware Interface Description (Order No. 100469, formerly 1192), the RL56DDP Designer's Guide (Doc. No. 1141), the CSMV/6 AnyPort™ Multi-Service Access Processor Software Interface Description (Doc. No. 100597, formerly 1148), and the Command Reference Manual (Doc. No. 100468, formerly 1195).

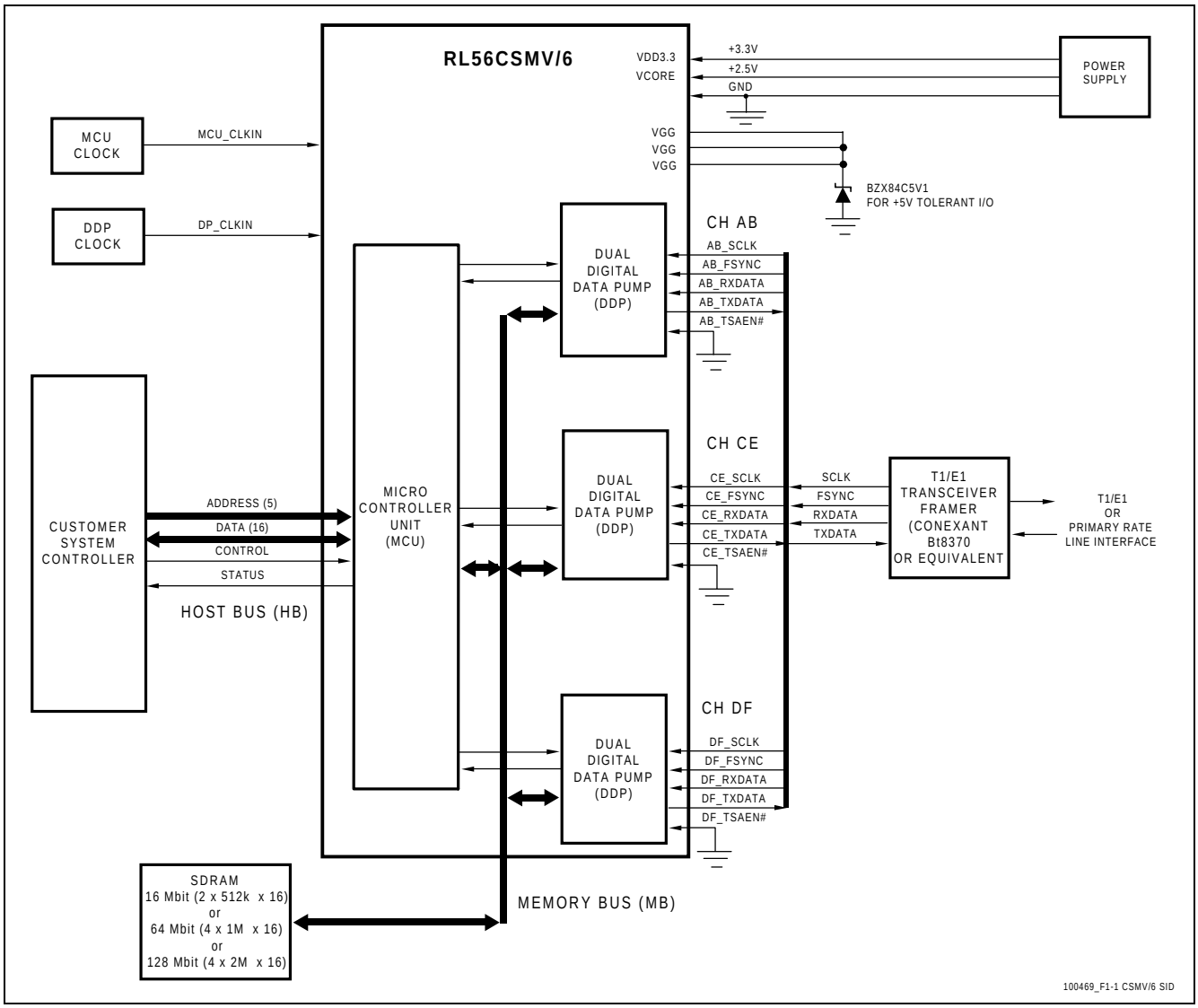


Figure 1. RL56CSMV/6 Implementation Example Block Diagram

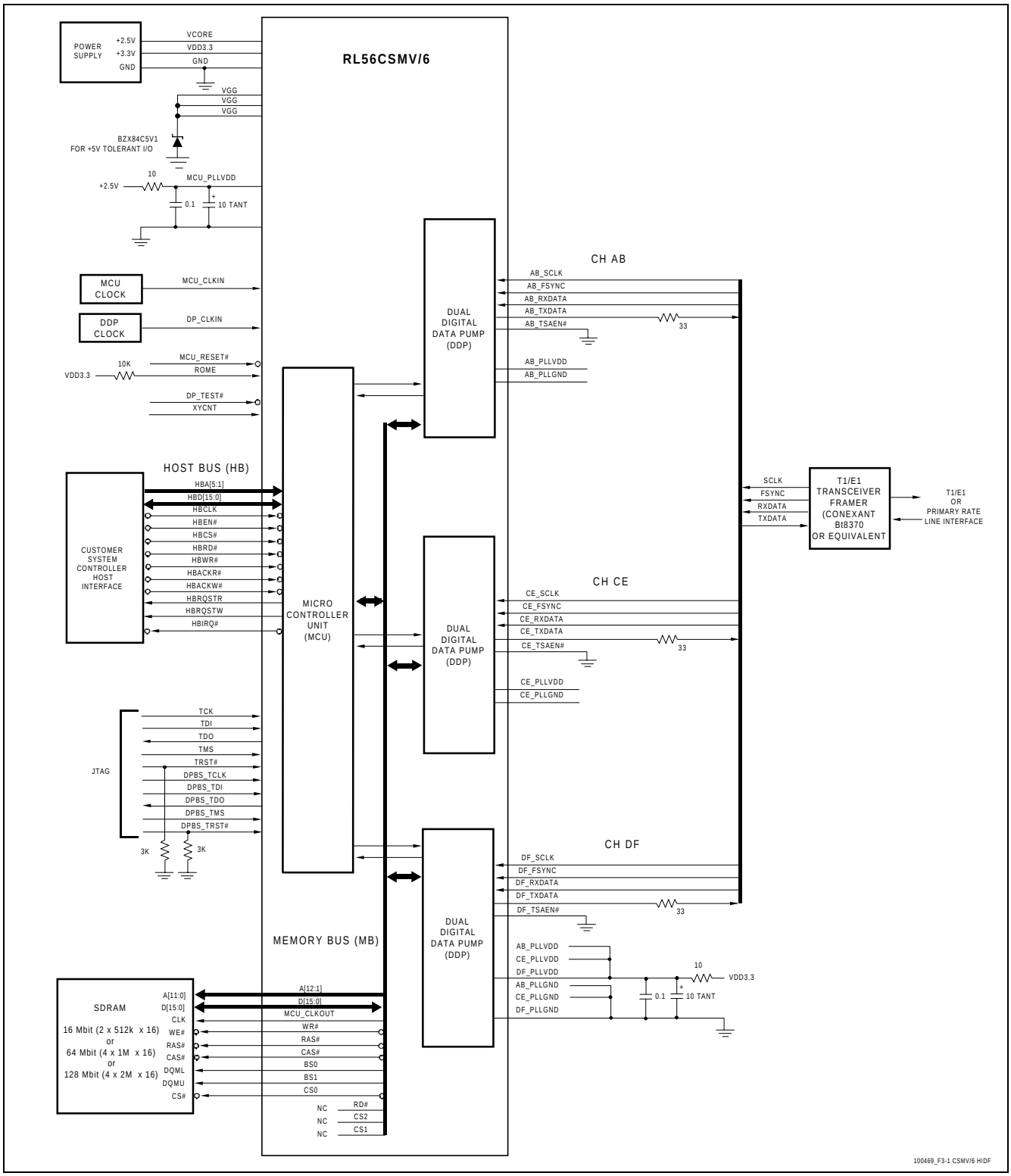


Figure 2. RL56CSMV/6 Hardware Interface Signals

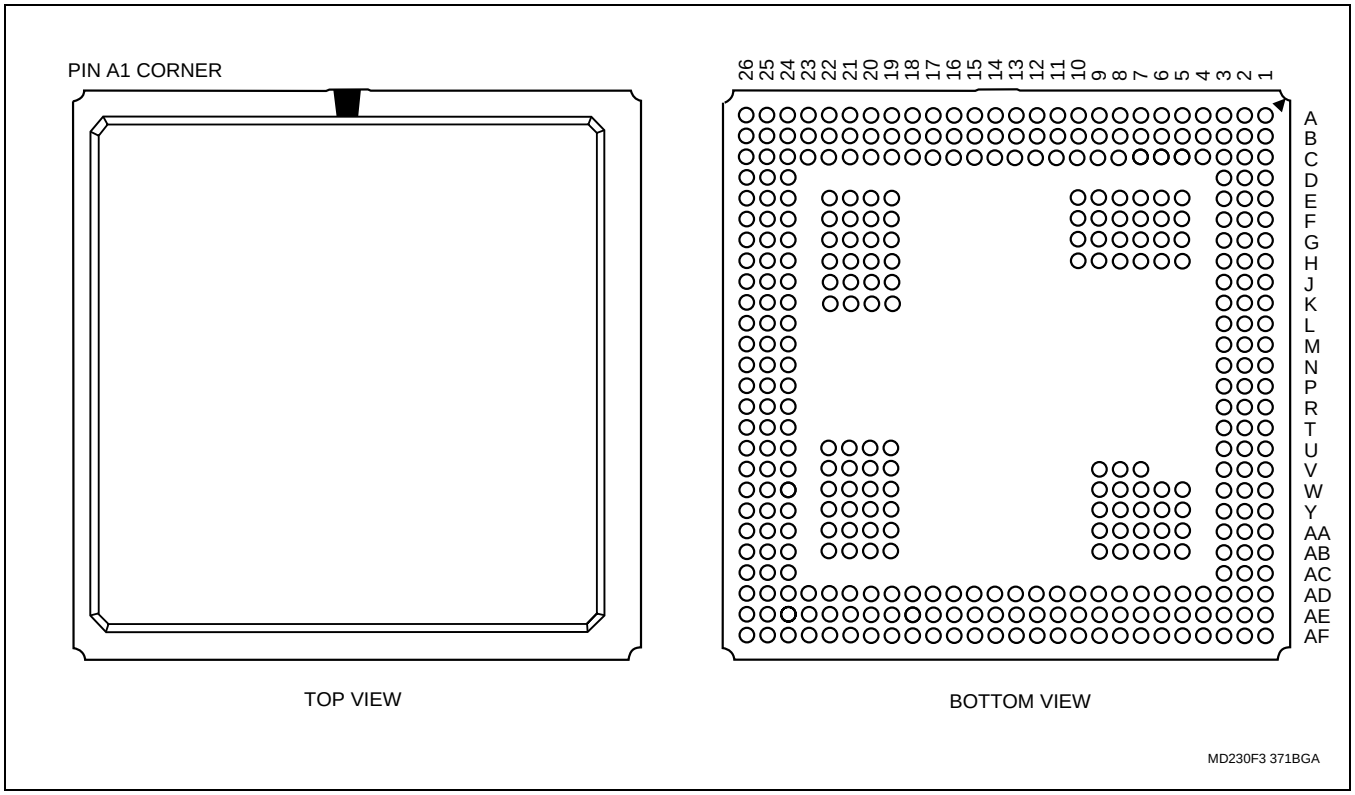


Figure 3. 371-Pin BGA Package

Table 2. RL56CSMV/6 Pin Signals by Pin Location

Ref Col.	1			2			3			4		
Ref Row	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F
1	A01	D_DPRST# (PD1)	TEST	B25	C_DPRXCLK (PC3)	TEST	F01	CE_SCLK	CH CE	J03	VDD3.3	3.3V
2	A02	B_DPRST# (PB1)	TEST	B26	A_DPCS#	TEST	F02	E_DSPRST#	TEST	J19	GND	GND
3	A03	C_DPRST# (PC1)	TEST	C01	CE_RXDATA	CH CE	F03	VCORE	2.5V	J20	GND	GND
4	A04	VGG	ZENER*	C02	C_DPSA2CLK	TEST	F05	C_DPCS#	TEST	J21	GND	GND
5	A05	CE_DSPCS#	TEST	C03	C_DPPF6#	TEST	F06	GND	GND	J22	GND	GND
6	A06	A4	MB	C04	F_DPCS#	TEST	F07	GND	GND	J24	D_DPPF6#	TEST
7	A07	A3	MB	C05	VCORE	2.5V	F08	GND	GND	J25	NC	NC
8	A08	A2	MB	C06	CE_YCLK	TEST	F09	GND	GND	J26	AB_IACLKIN	TEST
9	A09	A1	MB	C07	CE_XCLK	TEST	F10	GND	GND	K01	BS1	MB
10	A10	A0	MB	C08	C_DSPRST#	TEST	F19	GND	GND	K02	DPBS_TDO	JTAG
11	A11	D7	MB	C09	CE_PLLGND	GND	F20	GND	GND	K03	VDD3.3	3.3V
12	A12	D6	MB	C10	F_DSPRD#	TEST	F21	GND	GND	K19	GND	GND
13	A13	D5	MB	C11	DPBS_TRST#	JTAG	F22	B_DSPRD#	TEST	K20	GND	GND
14	A14	D0	MB	C12	VCORE	2.5V	F24	TEST#_DP	TEST	K21	GND	GND
15	A15	DP_CLKIN	SYS	C13	C_DPINT (PC4)	TEST	F25	B_DPSA2CLK	TEST	K22	GND	GND
16	A16	A_DPA4	TEST	C14	C_DPGP00	TEST	F26	B_EYESYNC	EYE	K24	B_DPRXCLK (PB3)	TEST
17	A17	B_DPINT (PB4)	TEST	C15	VDD3.3	3.3V	G01	C_EYESYNC	EYE	K25	B_DPTXCLK (PB7)	TEST
18	A18	B_EYEXY	EYE	C16	AB_PLLVDD	3.3V	G02	C_DPSR2IO	TEST	K26	AB_RXDATA	CH AB
19	A19	AB_DSPINT	TEST	C17	E_DSPRD#	TEST	G03	CE_PLLVDD	3.3V	L01	D9	MB
20	A20	AB_XCLK	TEST	C18	E_DSPWT#	TEST	G05	C_DPIA2CLK	TEST	L02	D8	MB
21	A21	AB_YCLK	TEST	C19	F_DSPWT#	TEST	G06	GND	GND	L03	C_EYEXY	EYE
22	A22	A_DSPRD#	TEST	C20	E_DPA4	TEST	G07	GND	GND	L24	XYCNT	TEST
23	A23	AB_TSAEN#	CH AB	C21	F_DPA4	TEST	G08	GND	GND	L25	B_DPPF6#	TEST
24	A24	A_DSPWT#	TEST	C22	E_EYEXY	EYE	G09	GND	GND	L26	AB_TXDATA	CH AB
25	A25	A_DPPF6#	TEST	C23	B_DPTXD (PB2)	TEST	G10	GND	GND	M01	D12	MB
26	A26	A_DSPRST#	TEST	C24	VDD3.3	3.3V	G19	GND	GND	M02	D11	MB
27	B01	CE_TXDATA	CH CE	C25	B_DPGP01	TEST	G20	GND	GND	M03	D10	MB
28	B02	A_DPRST# (PA1)	TEST	C26	NC	NC	G21	GND	GND	M24	VDD3.3	3.3V
29	B03	NC	NC	D01	CE_IACLKIN	TEST	G22	B_DPIA2CLK	TEST	M25	AB_DSPCS#	TEST
30	B04	F_DPRST# (PF1)	TEST	D02	E_DPCS#	TEST	G24	NC	NC	M26	B_DSPRST#	TEST
31	B05	TICACTV	TEST	D03	C_DPSR3IN	TEST	G25	F_DPSR2IO	TEST	N01	D15	MB
32	B06	TACK	TEST	D24	VDD3.3	3.3V	G26	AB_SCLK	CH AB	N02	D14	MB
33	B07	NC	NC	D25	PB5	NC	H01	C_EYECLK#	EYE	N03	D13	MB
34	B08	NC	NC	D26	B_CTLSIN	TEST	H02	NC	NC	N24	WR#	MB
35	B09	E_DPRST# (PE1)	TEST	E01	CE_FSYNC	CH CE	H03	CE_DSPINT	TEST	N25	AB_PLLGND	GND
36	B10	D4	MB	E02	E_DPPF6#	TEST	H05	C_DPA4	TEST	N26	DPBS_TCLK	JTAG
37	B11	D3	MB	E03	C_DPGP01	TEST	H06	GND	GND	P01	CAS#	MB
38	B12	D2	MB	E05	F_DPPF6#	TEST	H07	GND	GND	P02	RAS#	MB
39	B13	D1	MB	E06	C_DSPWT#	TEST	H08	GND	GND	P03	MCU_CLKIN	SYS
40	B14	D_DPRXD (PD6)	TEST	E07	C_DSPRD#	TEST	H09	GND	GND	P24	DF_DSPINT	TEST
41	B15	NC	NC	E08	GND	GND	H10	GND	GND	P25	RD#	MB
42	B16	B_DPGP00	TEST	E09	GND	GND	H19	GND	GND	P26	D_EYEXY	EYE
43	B17	NC	NC	E10	GND	GND	H20	GND	GND	R01	A_DPTXCLK (PA7)	TEST
44	B18	B_DPRXD (PB6)	TEST	E19	B_DPSR3IN	TEST	H21	GND	GND	R02	SRAMBIST2 (PD5)	TEST
45	B19	F_EYEXY	EYE	E20	B_DPA4	TEST	H22	GND	GND	R03	MCU_CLKOUT	MB
46	B20	A_EYEXY	EYE	E21	B_DSPWT#	TEST	H24	VDD3.3	3.3V	R24	D_DPTXCLK (PD7)	TEST
47	B21	A_DPSR2IO	TEST	E22	B_DPCS#	TEST	H25	E_DPSR2IO	TEST	R25	DF_YCLK	TEST
48	B22	C_DPRXD (PC6)	TEST	E24	F_DSPRST#	TEST	H26	AB_FSYNC	CH AB	R26	DF_XCLK	TEST
49	B23	C_DPTXD (PC2)	TEST	E25	B_DPSR2IO	TEST	J01	C_CTLSIN	TEST	T01	A_DPRXD (PA6)	TEST
50	B24	C_DPTXCLK (PC7)	TEST	E26	B_EYECLK#	EYE	J02	CE_TSAEN#	CH CE	T02	E_DPINT (PE4)	TEST

Notes:

Pin Signal NC = No internal connection; I/F NC = No external connection.

* Connect all VGG pins to GND through one +5.1V zener diode for +5V tolerant inputs; connect all VGG pins to VDD3.3 for +3.3V inputs.

Table 2. RL56CSMV/6 Pin Signals by Pin Location (Continued)

Ref Col.	1			2			3			4		
Ref Row	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F
1	T03	VCORE	2.5V	Y19	GND	GND	AD08	MCU_PLLVDD	2.5V	AF06	HBD0	HB
2	T24	D_DPINT (PD4)	TEST	Y20	GND	GND	AD09	VDD3.3	3.3V	AF07	HBD2	HB
3	T25	VCORE	2.5V	Y21	GND	GND	AD10	VDD3.3	3.3V	AF08	HBD3	HB
4	T26	VCORE	2.5V	Y22	D_DPA4	TEST	AD11	VCORE	2.5V	AF09	HBD10	HB
5	U01	A_DPINT (PA4)	TEST	Y24	D_EYECLK#	EYE	AD12	HBD14	HB	AF10	HBD8	HB
6	U02	PE0	NC	Y25	NC	NC	AD13	HBA2	HB	AF11	HBD5	HB
7	U03	VCORE	2.5V	Y26	WKRES#_DP	TEST	AD14	HBA5	HB	AF12	HBD13	HB
8	U19	GND	GND	AA01	SRAMBIST1 (PE5)	TEST	AD15	DPBS_TDI	JTAG	AF13	HBD11	HB
9	U20	GND	GND	AA02	E_DPTXCLK (PE7)	TEST	AD16	DF_PLLGND	GND	AF14	HBA3	HB
10	U21	GND	GND	AA03	VDD3.3	3.3V	AD17	D_DSPRST#	TEST	AF15	HBA4	HB
11	U22	GND	GND	AA05	TREQA	GND	AD18	A12	MB	AF16	HBRD#	HB
12	U24	VGG	ZENER*	AA06	GND	GND	AD19	DF_DSPCS#	TEST	AF17	D_DPSA2CLK	TEST
13	U25	DF_TSAEN#	CH DF	AA07	GND	GND	AD20	A11	MB	AF18	HBIRQ#	HB
14	U26	D_CTLSIN	TEST	AA08	GND	GND	AD21	A16	MB	AF19	A6	MB
15	V01	E_DPRXD (PE6)	TEST	AA09	GND	GND	AD22	A15	MB	AF20	DPBS_TMS	JTAG
16	V02	E_DPTXD (PE2)	TEST	AA19	GND	GND	AD23	PC0	NC	AF21	A8	MB
17	V03	NC	NC	AA20	GND	GND	AD24	WR#	MB	AF22	A10	MB
18	V07	GND	GND	AA21	GND	GND	AD25	DF_RXDATA	CH DF	AF23	A17	MB
19	V08	GND	GND	AA22	D_DPIA2CLK	TEST	AD26	CS1	MB	AF24	A19	MB
20	V09	GND	GND	AA24	VGG	ZENER*	AE01	PF5	NC	AF25	A18	MB
21	V19	GND	GND	AA25	D_EYESYNC	EYE	AE02	TDO	JTAG	AF26	PB0	NC
22	V20	GND	GND	AA26	CS2	MB	AE03	TCK	JTAG			
23	V21	GND	GND	AB01	PF0	NC	AE04	HBRQSTR	HB			
24	V22	GND	GND	AB02	PC5	NC	AE05	HBRQSTW	HB			
25	V24	D_DPRXCLK (PD3)	TEST	AB03	F_DPTXD (PF2)	TEST	AE06	HBD1	HB			
26	V25	D_DPTXD (PD2)	TEST	AB05	TREQB	GND	AE07	HBD9	HB			
27	V26	DF_PLLVDD	3.3V	AB06	TICCLK	GND	AE08	HBD4	HB			
28	W01	A_DPRXCLK (PA3)	TEST	AB07	SCANMODE	GND	AE09	HBD6	HB			
29	W02	A_DPTXD (PA2)	TEST	AB08	SCANEN	GND	AE10	HBD7	HB			
30	W03	VCORE	2.5V	AB09	GND	GND	AE11	HBD12	HB			
31	W05	GND	GND	AB19	D_DSPRD#	TEST	AE12	HBD15	HB			
32	W06	GND	GND	AB20	D_DSPWT#	TEST	AE13	HBA1	HB			
33	W07	GND	GND	AB21	D_DPGP00	TEST	AE14	HBCS#	HB			
34	W08	GND	GND	AB22	D_DPCS#	TEST	AE15	HBWR#	HB			
35	W09	GND	GND	AB24	DF_IACLKIN	TEST	AE16	HBCLK	HB			
36	W19	GND	GND	AB25	DF_FSYNC	CH DF	AE17	HBEN#	HB			
37	W20	GND	GND	AB26	D_DPSR2IO	TEST	AE18	A5	MB			
38	W21	GND	GND	AC01	TRST#	JTAG	AE19	A7	MB			
39	W22	D_DPGP01	TEST	AC02	F_DPRXCLK (PF3)	TEST	AE20	A9	MB			
40	W24	MCU_RESET#	SYS	AC03	VDD3.3	3.3V	AE21	A13	MB			
41	W25	ROME	SYS	AC24	CS0	MB	AE22	VDD3.3	3.3V			
42	W26	BS0	MB	AC25	DF_TXDATA	CH DF	AE23	D_DPSR3IN	TEST			
43	Y01	PD0	NC	AC26	DF_SCLK	CH DF	AE24	A14	MB			
44	Y02	E_DPRXCLK (PE3)	TEST	AD01	F_DPINT (PF4)	TEST	AE25	PA5	NC			
45	Y03	VDD3.3	3.3V	AD02	TMS	JTAG	AE26	PA0	NC			
46	Y05	GND	GND	AD03	VDD3.3	3.3V	AF01	F_DPRXD (PF6)	TEST			
47	Y06	GND	GND	AD04	VDD3.3	3.3V	AF02	F_DPTXCLK (PF7)	TEST			
48	Y07	GND	GND	AD05	VDD3.3	3.3V	AF03	TDI	JTAG			
49	Y08	GND	GND	AD06	VCORE	2.5V	AF04	HBACKR#	HB			
50	Y09	GND	GND	AD07	VCORE	2.5V	AF05	HBACKW#	HB			

Notes:

Pin Signal NC = No internal connection; I/F NC = No external connection.

* Connect all VGG pins to GND through one+5.1V zener diode for +5V tolerant inputs; connect all VGG pins to VDD3.3 for +3.3V inputs.

Table 3. RL56CSMV/6 Pin Signals by Interface

Ref Col.	1			2			3			4		
Ref Row	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F
1	AD08	MCU_PLLVDD	2.5V	E26	B_EYECLK#	EYE	J19	GND	GND	AE06	HBD1	HB
2	AD06	VCORE	2.5V	F26	B_EYESYNC	EYE	J20	GND	GND	AF09	HBD10	HB
3	AD07	VCORE	2.5V	A18	B_EYEXY	EYE	J21	GND	GND	AF13	HBD11	HB
4	AD11	VCORE	2.5V	H01	C_EYECLK#	EYE	J22	GND	GND	AE11	HBD12	HB
5	C05	VCORE	2.5V	G01	C_EYESYNC	EYE	K19	GND	GND	AF12	HBD13	HB
6	C12	VCORE	2.5V	L03	C_EYEXY	EYE	K20	GND	GND	AD12	HBD14	HB
7	F03	VCORE	2.5V	Y24	D_EYECLK#	EYE	K21	GND	GND	AE12	HBD15	HB
8	T03	VCORE	2.5V	AA25	D_EYESYNC	EYE	K22	GND	GND	AF07	HBD2	HB
9	T25	VCORE	2.5V	P26	D_EYEXY	EYE	U19	GND	GND	AF08	HBD3	HB
10	T26	VCORE	2.5V	C22	E_EYEXY	EYE	U20	GND	GND	AE08	HBD4	HB
11	U03	VCORE	2.5V	B19	F_EYEXY	EYE	U21	GND	GND	AF11	HBD5	HB
12	W03	VCORE	2.5V	N25	AB_PLLGND	GND	U22	GND	GND	AE09	HBD6	HB
13	C16	AB_PLLVDD	3.3V	C09	CE_PLLGND	GND	V07	GND	GND	AE10	HBD7	HB
14	G03	CE_PLLVDD	3.3V	AD16	DF_PLLGND	GND	V08	GND	GND	AF10	HBD8	HB
15	V26	DF_PLLVDD	3.3V	AA06	GND	GND	V09	GND	GND	AE07	HBD9	HB
16	AA03	VDD3.3	3.3V	AA07	GND	GND	V19	GND	GND	AE17	HBEN#	HB
17	AC03	VDD3.3	3.3V	AA08	GND	GND	V20	GND	GND	AF18	HBIRQ#	HB
18	AD03	VDD3.3	3.3V	AA09	GND	GND	V21	GND	GND	AF16	HBRD#	HB
19	AD04	VDD3.3	3.3V	AA19	GND	GND	V22	GND	GND	AE04	HBRQSTR	HB
20	AD05	VDD3.3	3.3V	AA20	GND	GND	W05	GND	GND	AE05	HBRQSTW	HB
21	AD09	VDD3.3	3.3V	AA21	GND	GND	W06	GND	GND	AE15	HBWR#	HB
22	AD10	VDD3.3	3.3V	AB09	GND	GND	W07	GND	GND	N26	DPBS_TCLK	JTAG
23	AE22	VDD3.3	3.3V	E08	GND	GND	W08	GND	GND	AD15	DPBS_TDI	JTAG
24	C15	VDD3.3	3.3V	E09	GND	GND	W09	GND	GND	K02	DPBS_TDO	JTAG
25	C24	VDD3.3	3.3V	E10	GND	GND	W19	GND	GND	AF20	DPBS_TMS	JTAG
26	D24	VDD3.3	3.3V	F06	GND	GND	W20	GND	GND	C11	DPBS_TRST#	JTAG
27	H24	VDD3.3	3.3V	F07	GND	GND	W21	GND	GND	AE03	TCK	JTAG
28	J03	VDD3.3	3.3V	F08	GND	GND	Y05	GND	GND	AF03	TDI	JTAG
29	K03	VDD3.3	3.3V	F09	GND	GND	Y06	GND	GND	AE02	TDO	JTAG
30	M24	VDD3.3	3.3V	F10	GND	GND	Y07	GND	GND	AD02	TMS	JTAG
31	Y03	VDD3.3	3.3V	F19	GND	GND	Y08	GND	GND	AC01	TRST#	JTAG
32	A04	VGG	ZENER*	F20	GND	GND	Y09	GND	GND	A10	A0	MB
33	AA24	VGG	ZENER*	F21	GND	GND	Y19	GND	GND	A09	A1	MB
34	U24	VGG	ZENER*	G06	GND	GND	Y20	GND	GND	AD20	A11	MB
35	H26	AB_FSYNC	CH AB	G07	GND	GND	Y21	GND	GND	AD18	A12	MB
36	K26	AB_RXDATA	CH AB	G08	GND	GND	AB08	SCANEN	GND	AE21	A13	MB
37	G26	AB_SCLK	CH AB	G09	GND	GND	AB07	SCANMODE	GND	AE24	A14	MB
38	A23	AB_TSAEN#	CH AB	G10	GND	GND	AB06	TICCLK	GND	AD22	A15	MB
39	L26	AB_TXDATA	CH AB	G19	GND	GND	AA05	TREQA	GND	AD21	A16	MB
40	E01	CE_FSYNC	CH CE	G20	GND	GND	AB05	TREQB	GND	AF23	A17	MB
41	C01	CE_RXDATA	CH CE	G21	GND	GND	AE13	HBA1	HB	AF25	A18	MB
42	F01	CE_SCLK	CH CE	H06	GND	GND	AD13	HBA2	HB	AF24	A19	MB
43	J02	CE_TSAEN#	CH CE	H07	GND	GND	AF14	HBA3	HB	A08	A2	MB
44	B01	CE_TXDATA	CH CE	H08	GND	GND	AF15	HBA4	HB	A07	A3	MB
45	AB25	DF_FSYNC	CH DF	H09	GND	GND	AD14	HBA5	HB	A06	A4	MB
46	AD25	DF_RXDATA	CH DF	H10	GND	GND	AF04	HBACKR#	HB	AE18	A5	MB
47	AC26	DF_SCLK	CH DF	H19	GND	GND	AF05	HBACKW#	HB	AF19	A6	MB
48	U25	DF_TSAEN#	CH DF	H20	GND	GND	AE16	HBCLK	HB	AE19	A7	MB
49	AC25	DF_TXDATA	CH DF	H21	GND	GND	AE14	HBCS#	HB	AF21	A8	MB
50	B20	A_EYEXY	EYE	H22	GND	GND	AF06	HBD0	HB	AE20	A9	MB

Notes:

Pin Signal NC = No internal connection; I/F NC = No external connection.

* Connect all VGG pins to GND through one+5.1V zener diode for +5V tolerant inputs; connect all VGG pins to VDD3.3 for +3.3V inputs.

Table 3. RL56CSMV/6 Pin Signals by Interface (Continued))

Ref Col.	1			2			3			4		
Ref Row	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F
1	AF22	A10	MB	P03	MCU_CLKIN	SYS	B22	C_DPRXD (PC6)	TEST	C18	E_DSPWT#	TEST
2	W26	BS0	MB	W24	MCU_RESET#	SYS	C02	C_DPSA2CLK	TEST	C21	F_DPA4	TEST
3	K01	BS1	MB	W25	ROME	SYS	G02	C_DPSR2IO	TEST	C04	F_DPCS#	TEST
4	P01	CAS#	MB	A16	A_DPA4	TEST	D03	C_DPSR3IN	TEST	AD01	F_DPINT (PF4)	TEST
5	AC24	CS0	MB	B26	A_DPCS#	TEST	B24	C_DPTXCLK (PC7)	TEST	E05	F_DPPF6#	TEST
6	AD26	CS1	MB	U01	A_DPINT (PA4)	TEST	B23	C_DPTXD (PC2)	TEST	B04	F_DPRST# (PF1)	TEST
7	AA26	CS2	MB	A25	A_DPPF6#	TEST	E07	C_DSPRD#	TEST	AC02	F_DPRXCLK (PF3)	TEST
8	A14	D0	MB	B02	A_DPRST# (PA1)	TEST	C08	C_DSPRST#	TEST	AF01	F_DPRXD (PF6)	TEST
9	B13	D1	MB	W01	A_DPRXCLK (PA3)	TEST	E06	C_DSPWT#	TEST	G25	F_DPSR2IO	TEST
10	M03	D10	MB	T01	A_DPRXD (PA6)	TEST	A05	CE_DSPCS#	TEST	AF02	F_DPTXCLK (PF7)	TEST
11	M02	D11	MB	B21	A_DPSR2IO	TEST	H03	CE_DSPINT	TEST	AB03	F_DPTXD (PF2)	TEST
12	M01	D12	MB	R01	A_DPTXCLK (PA7)	TEST	D01	CE_IACLKIN	TEST	C10	F_DSPRD#	TEST
13	N03	D13	MB	W02	A_DPTXD (PA2)	TEST	C07	CE_XCLK	TEST	E24	F_DSPRST#	TEST
14	N02	D14	MB	A22	A_DSPRD#	TEST	C06	CE_YCLK	TEST	C19	F_DSPWT#	TEST
15	N01	D15	MB	A26	A_DSPRST#	TEST	U26	D_CTLSIN	TEST	AA01	SRAMBIST1 (PE5)	TEST
16	B12	D2	MB	A24	A_DSPWT#	TEST	Y22	D_DPA4	TEST	R02	SRAMBIST2 (PD5)	TEST
17	B11	D3	MB	M25	AB_DSPCS#	TEST	AB22	D_DPCS#	TEST	B06	TACK	TEST
18	B10	D4	MB	A19	AB_DSPINT	TEST	AB21	D_DPGP00	TEST	F24	TEST#_DP	TEST
19	A13	D5	MB	J26	AB_IACLKIN	TEST	W22	D_DPGP01	TEST	B05	TICACTV	TEST
20	A12	D6	MB	A20	AB_XCLK	TEST	AA22	D_DPIA2CLK	TEST	Y26	WKRES#_DP	TEST
21	A11	D7	MB	A21	AB_YCLK	TEST	T24	D_DPINT (PD4)	TEST	L24	XYCNT	TEST
22	L02	D8	MB	D26	B_CTLSIN	TEST	J24	D_DPPF6#	TEST			
23	L01	D9	MB	E20	B_DPA4	TEST	A01	D_DPRST# (PD1)	TEST			
24	R03	MCU_CLKOUT	MB	E22	B_DPCS#	TEST	V24	D_DPRXCLK (PD3)	TEST			
25	P02	RAS#	MB	B16	B_DPGP00	TEST	B14	D_DPRXD (PD6)	TEST			
26	P25	RD#	MB	C25	B_DPGP01	TEST	AF17	D_DPSA2CLK	TEST			
27	AD24	WR#	MB	G22	B_DPIA2CLK	TEST	AB26	D_DPSR2IO	TEST			
28	N24	WR#	MB	A17	B_DPINT (PB4)	TEST	AE23	D_DPSR3IN	TEST			
29	B03	NC	NC	L25	B_DPPF6#	TEST	R24	D_DPTXCLK (PD7)	TEST			
30	B07	NC	NC	A02	B_DPRST# (PB1)	TEST	V25	D_DPTXD (PD2)	TEST			
31	B08	NC	NC	K24	B_DPRXCLK (PB3)	TEST	AB19	D_DSPRD#	TEST			
32	B15	NC	NC	B18	B_DPRXD (PB6)	TEST	AD17	D_DSPRST#	TEST			
33	B17	NC	NC	F25	B_DPSA2CLK	TEST	AB20	D_DSPWT#	TEST			
34	C26	NC	NC	E25	B_DPSR2IO	TEST	AD19	DF_DSPCS#	TEST			
35	G24	NC	NC	E19	B_DPSR3IN	TEST	P24	DF_DSPINT	TEST			
36	H02	NC	NC	K25	B_DPTXCLK (PB7)	TEST	AB24	DF_IACLKIN	TEST			
37	J25	NC	NC	C23	B_DPTXD (PB2)	TEST	R26	DF_XCLK	TEST			
38	V03	NC	NC	F22	B_DSPRD#	TEST	R25	DF_YCLK	TEST			
39	Y25	NC	NC	M26	B_DSPRST#	TEST	C20	E_DPA4	TEST			
40	AE26	PA0	NC	E21	B_DSPWT#	TEST	D02	E_DPCS#	TEST			
41	AE25	PA5	NC	J01	C_CTLSIN	TEST	T02	E_DPINT (PE4)	TEST			
42	AF26	PB0	NC	H05	C_DPA4	TEST	E02	E_DPPF6#	TEST			
43	D25	PB5	NC	F05	C_DPCS#	TEST	B09	E_DPRST# (PE1)	TEST			
44	AD23	PC0	NC	C14	C_DPGP00	TEST	Y02	E_DPRXCLK (PE3)	TEST			
45	AB02	PC5	NC	E03	C_DPGP01	TEST	V01	E_DPRXD (PE6)	TEST			
46	Y01	PD0	NC	G05	C_DPIA2CLK	TEST	H25	E_DPSR2IO	TEST			
47	U02	PE0	NC	C13	C_DPINT (PC4)	TEST	AA02	E_DPTXCLK (PE7)	TEST			
48	AB01	PF0	NC	C03	C_DPPF6#	TEST	V02	E_DPTXD (PE2)	TEST			
49	AE01	PF5	NC	A03	C_DPRST# (PC1)	TEST	C17	E_DSPRD#	TEST			
50	A15	DP_CLKIN	SYS	B25	C_DPRXCLK (PC3)	TEST	F02	E_DSPRST#	TEST			

Notes:
Pin Signal NC = No internal connection; I/F NC = No external connection.
* Connect all VGG pins to GND through one+5.1V zener diode for +5V tolerant inputs; connect all VGG pins to VDD3.3 for +3.3V inputs.

Table 4. RL56CSMV/6 Application Signals by Interface

Ref Col.	1			2			3			4		
Ref Row	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F	Loc.	Signal	I/F
1	H26	AB_FSYNC	CH AB	AE13	HBA1	HB	A10	A0	MB	A15	DP_CLKIN	SYS
2	K26	AB_RXDATA	CH AB	AD13	HBA2	HB	A09	A1	MB	P03	MCU_CLKIN	SYS
3	G26	AB_SCLK	CH AB	AF14	HBA3	HB	A08	A2	MB	W24	MCU_RESET#	SYS
4	A23	AB_TSAEN#	CH AB	AF15	HBA4	HB	A07	A3	MB	W25	ROME	SYS
5	L26	AB_TXDATA	CH AB	AD14	HBA5	HB	A06	A4	MB	N26	DPBS_TCLK	JTAG
6	E01	CE_FSYNC	CH CE	AF04	HBACKR#	HB	AE18	A5	MB	AD15	DPBS_TDI	JTAG
7	C01	CE_RXDATA	CH CE	AF05	HBACKW#	HB	AF19	A6	MB	K02	DPBS_TDO	JTAG
8	F01	CE_SCLK	CH CE	AE16	HBCLK	HB	AE19	A7	MB	AF20	DPBS_TMS	JTAG
9	J02	CE_TSAEN#	CH CE	AE14	HBCS#	HB	AF21	A8	MB	C11	DPBS_TRST#	JTAG
10	B01	CE_TXDATA	CH CE	AF06	HBD0	HB	AE20	A9	MB	AE03	TCK	JTAG
11	AB25	DF_FSYNC	CH DF	AE06	HBD1	HB	AF22	A10	MB	AF03	TDI	JTAG
12	AD25	DF_RXDATA	CH DF	AF09	HBD10	HB	AD20	A11	MB	AE02	TDO	JTAG
13	AC26	DF_SCLK	CH DF	AF13	HBD11	HB	AD18	A12	MB	AD02	TMS	JTAG
14	U25	DF_TSAEN#	CH DF	AE11	HBD12	HB	AE21	A13	MB	AC01	TRST#	JTAG
15	AC25	DF_TXDATA	CH DF	AF12	HBD13	HB	AE24	A14	MB			
16				AD12	HBD14	HB	AD22	A15	MB			
17				AE12	HBD15	HB	AD21	A16	MB			
18				AF07	HBD2	HB	AF23	A17	MB			
19				AF08	HBD3	HB	AF25	A18	MB			
20				AE08	HBD4	HB	AF24	A19	MB			
21				AF11	HBD5	HB	W26	BS0	MB			
22				AE09	HBD6	HB	K01	BS1	MB			
23				AE10	HBD7	HB	P01	CAS#	MB			
24				AF10	HBD8	HB	AC24	CS0	MB			
25				AE07	HBD9	HB	AD26	CS1	MB			
26				AE17	HBEN#	HB	AA26	CS2	MB			
27				AF18	HBIRQ#	HB	A14	D0	MB			
28				AF16	HBRD#	HB	B13	D1	MB			
29				AE04	HBRQSTR	HB	B12	D2	MB			
30				AE05	HBRQSTW	HB	B11	D3	MB			
31				AE15	HBWR#	HB	B10	D4	MB			
32							A13	D5	MB			
33							A12	D6	MB			
34							A11	D7	MB			
35							L02	D8	MB			
36							L01	D9	MB			
37							M03	D10	MB			
38							M02	D11	MB			
39							M01	D12	MB			
40							N03	D13	MB			
41							N02	D14	MB			
42							N01	D15	MB			
43							R03	MCU_CLKOUT	MB			
44							P02	RAS#	MB			
45							P25	RD#	MB			
46							AD24	WR#	MB			
47							N24	WR#	MB			
48												
49												
50												

ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

Operating Conditions and Absolute Maximum Ratings

Operating conditions are stated in Table 5.

The absolute maximum ratings are listed in Table 6.

Table 5. Operating Conditions

Parameter	Min.	Max.	Units
VDD3.3	+3.0	+3.6	VDC
VCORE	+2.375	+2.625	VDC
Junction Temperature (T_j)	0	110	°C

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
VCORE Supply Voltage (+2.5V nominal)	VCORE	-0.5 to +3.0	V
VDD3.3 Supply Voltage (+3.3V nominal)	VDD3.3	-0.5 to +4.0	V
Input Voltage	V_{IN}	-0.5 to (VGG + 0.5)	V
Storage Temperature Range	T_{STG}	-55 to +125	°C
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VGG + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±300	mA
Latch-up Current (125°C)	I_{TRIG}	±150	mA
Maximum Junction Temperature	T_j	125	°C

Current and Power Requirements

The current and power requirements are listed in Table 7.

Table 7. Current and Power Requirements

Mode	DDP Clock at 28.224 MHz				DDP Clock at 45 MHz			
	Typ. Current (mA)	Max. Current (mA)	Typ. Power (mW)	Max. Power (mW)	Typ. Current (mA)	Max. Current (mA)	Typ. Power (mW)	Max. Power (mW)
Normal mode (6 Channels Active, Note 1)								
+3.3V (VDD3.3)	50	55	165	182	50	55	165	182
+2.5V (VCORE)	343	377	858	944	493	542	1233	1356
Sleep mode (6 Channels in Sleep Mode)								
+3.3V (VDD3.3)	23	25	76	83	23	25	76	83
+2.5V (VCORE)	110	121	275	303	110	121	275	303

Notes:

1. Current and power values shown for six channels in active online connected state in a typical modem circuit.
2. Test Conditions: VCORE = +2.5 VDC for typical values; VCORE = +2.625 VDC for maximum values
   VDD3.3 = +3.3 VDC for typical values; VDD3.3 = +3.6 VDC for maximum values
   T_j = 0°C to 110°C
3. f = internal operating frequency: MCU = 66 MHz; DDP = 28.224 MHz (during non-G.728 modes) or 45 MHz (during G.728 mode).

Product Thermal Performance

For multi-die packages, an equivalent thermal resistance is used to represent thermal performance. This definition is used to evaluate thermal performance of the package directly in a system level situation. The defined equivalent thermal resistance is only valid at the stated power conditions.

Junction Temperature Calculation for Package Type: 35 mm BGA, Size = 35.0 mm * 35.0 mm * 2.27 mm

Maximum junction temperature can be calculated as:

$$T_j = P \times \theta_{ja} + T_a \quad (1)$$

Where:

θ_{ja} = Equivalent Package Thermal Resistance (°C/W)

T_j = Maximum Junction Temperature (°C)

T_a = Ambient Temperature (°C)

P = Package Total Power Dissipation Value (W)

For this product:

P = 1.54 (W)

θ_{ja} = 21.30 °C/W (natural convection)

θ_{ja} = 16.50 °C/W (1 m/s air flow)

From equation (1) and assuming maximum ambient temperature of 70 °C, maximum junction temperature for the natural convection case is calculated as:

$$T_j = 1.54 \times 21.30 + 70 = 102.80 \text{ °C}$$

Test Structure

Package thermal performance has been tested following JEDEC standards. The BGA package has been mounted at the center of a 100 mm x 100 mm 6-layer test board and has been tested under different air flow velocities. Figure 4 shows the system configuration.

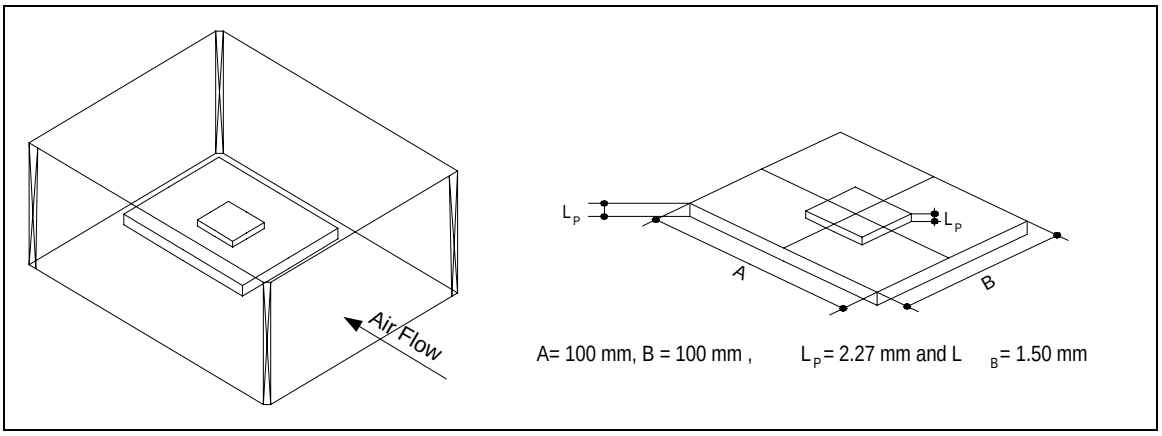
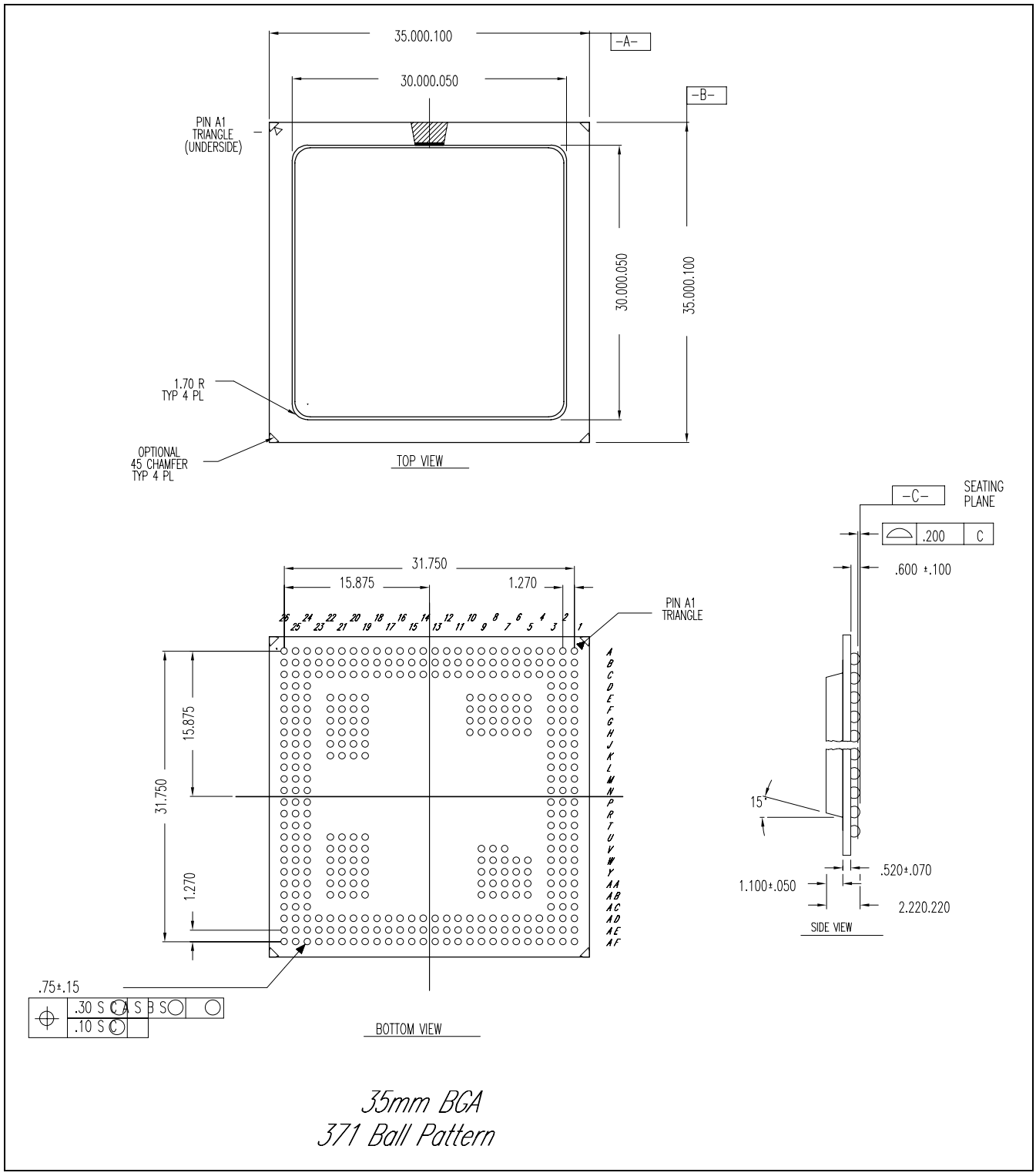


Figure 4. Test Performance Structure



Package Dimensions - 371-Pin BGA

REFERENCE

Table 8 identifies referenced specifications and recommendations.

Table 8. Referenced Specifications/Recommendations

Reference Number	Description
International Telecommunication Union (ITU) Recommendations	
G.168	Digital network echo cancellers
G.711	Pulse code modulation (PCM) of voice frequencies
G.723.1	Dual rate speech coder for multimedia communications transmitting at 5.3 and 6.3 kbit/s
G.723.1 Annex A	Silence compression scheme
G.723.1 Annex B	Alternative specification based on floating point arithmetic
G.726	40, 32, 24, 16 kbit/s adaptive differential pulse code modulation (ADPCM)
G.727	5-, 4-, 3- and 2-bits/sample embedded adaptive differential pulse code modulation (ADPCM)
G.728	Coding of speech at 16 kbit/s using low-delay code excited linear prediction
G.729	Coding of speech at 8 kbit/s using conjugate structure algebraic-code-excited linear-prediction (CS-ACELP)
G.729 Annex A	Reduced complexity 8 kbit/s CS-ACELP speech codec
G.729 Annex B	A silence compression scheme for G.729 optimized for terminals conforming to Recommendation V.70
Q.24	DTMF Detection
V.110	Support of data terminal equipments with V-series type interfaces by an integrated services digital network
V.120	Support by an ISDN of data terminal equipment with V-series type interfaces with provision for statistical multiplexing
V.17	A 2-wire modem for facsimile applications with rates up to 14 400 bit/s
V.21	300 bits per second duplex modem standardized for use in the general switched telephone network
V.22	1200 bits per second duplex modem standardized for use in the general switched telephone network and on point-to-point 2-wire leased telephone-type circuits
V.22 bis	2400 bits per second duplex modem using the frequency division technique standardized for use on the general switched telephone network and on point-to-point 2-wire leased telephone-type circuits
V.23	600/600-baud modem standardized for use in the general switched telephone network
V.27 ter	4800/2400 bits per second modem standardized for use in the general switched telephone network
V.29	9600 bits per second modem standardized for use on point-to-point 4-wire leased telephone-type circuits
V.32	A family of 2-wire, duplex modems operating at data signalling rates of up to 9600 bit/s for use on the general switched telephone network and on leased telephone-type circuits
V.32 bis	A duplex modem operating at data signalling rates of up to 14 400 bit/s for use on the general switched telephone network and on leased point-to-point 2-wire telephone-type circuits
V.33	14 400 bits per second modem standardized for use on point-to-point 4-wire leased telephone-type circuits
V.34	A modem operating at data signalling rates of up to 33 600 bit/s for use on the general switched telephone network and on leased point-to-point 2-wire telephone-type circuits
V.90	A digital modem and analogue modem pair for use on the public switched telephone network (PSTN) at data signalling rates of up to 56000 bits/sec downstream and up to 33600 bits/s upstream
European Telecommunications Standards Institute (ETSI)	
ETSI SMG GSM 06.10	Full Rate voice codec.
Internet Engineering Task Force (IETF)	
ietf-avt-rtp-new-00.txt IETF, December 5, 1997	RTP: A Transport Protocol for Real-Time Applications

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