ICs for Communications

Quad ISDN 4B3T Echocanceller Digital Front End DFE-T V2.1

PEF 24901 Version 2.1

Preliminary Data Sheet 06.99

DS 1

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Preface

This document describes the interfaces, functions and behavior of the QUAD ISDN 4B3T Echocanceller Digital Front End (DFE-T V2.1). The PEF 24901 is the digital part of a two-chip solution featuring four times ISDN basic rate access at 144kbit/s. DFE-T V2.1 supersedes the existing versions, DFE-T V1.1 and DFE-T V1.2.

The corresponding Analog Front End, the AFE V2.1 (PEF 24902) is described in detail in the Data Sheet V1.1, the Delta Sheet V1.2 and the Delta Sheet V2.1.

Organization of this Document

This Preliminary Data Sheet is divided into 9 chapters. It is organized as follows:

- Chapter 1, Introduction
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- Chapter 2, Pin Description
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- Chapter 3, Functional IC Description
  Gives a functional overview of the device, shows a block diagram, specifies the various interfaces and describes the provided U-transceiver functions.

- Chapter 4, Operational Description
  Describes the reset and power-down behavior, illustrates the activation and deactivation procedures, shows how the device is tested and how maintenance data can be retrieved.

- Chapter 5, Monitor Commands
  Lists all available Monitor Commands that can be applied.

- Chapter 6, Register Description
  Lists all register functions that are addressable by the new MON-12 protocol which behaves like a serial microprocessor interface.

- Chapter 7, Electrical Characteristics
  Denotes the operating conditions and gives the exact interface timing.

- Chapter 8, Package Outlines

- Chapter 9, Appendix A: Standards and Specifications

- Chapter 10, Glossary
- Chapter 11, Index

Related Documentation

- DFE-T V2.1 Product Overview 04.99
- DFE-T V2.1 Delta Sheet 03.98
- AFE V1.1 Data Sheet 05.96
- AFE V1.2 Delta Sheet 06.97
- AFE V2.1 Delta Sheet 09.98

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and in the body of your e-mail:
document type (Preliminary Data Sheet), issue date (06.99) and document revision number (DS 1).

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1 Introduction

The Quad ISDN 4B3T Echocanceller Digital Front End (DFE-T) is the digital part of an optimized two-chip solution featuring 4x ISDN basic rate access at 144kbit/s. The PEF 24901 is designed to provide in conjunction with the Quad ISDN Echocanceller Analog Front End (PEF 24902 V2.1) full duplex data transmission at the U-reference point according to FTZ Guideline 1TR 220, ETSI TS 102 080 and ITU-T I.430 standards.

The DFE-T 2nd generation has been completely reengineered to guarantee the availability of the well proved DFE-T/AFE solution over the year 2000. PEF 24901 V2.1 is downwards pin compatible and functionally equivalent to the DFE-T V1.x. Thus, line card manufacturers can make use of the most advanced process technology without the need to change their current design (besides the changeover to 3.3V power supply).

No software changes are required if the DFE-T V2.1 is deployed in existing DFE-T V1.x solutions. Some new features are provided such as transparent message exchange and enhanced monitoring and test functions. The data rate is programmable from 1Mbit/s to 4Mbit/s.

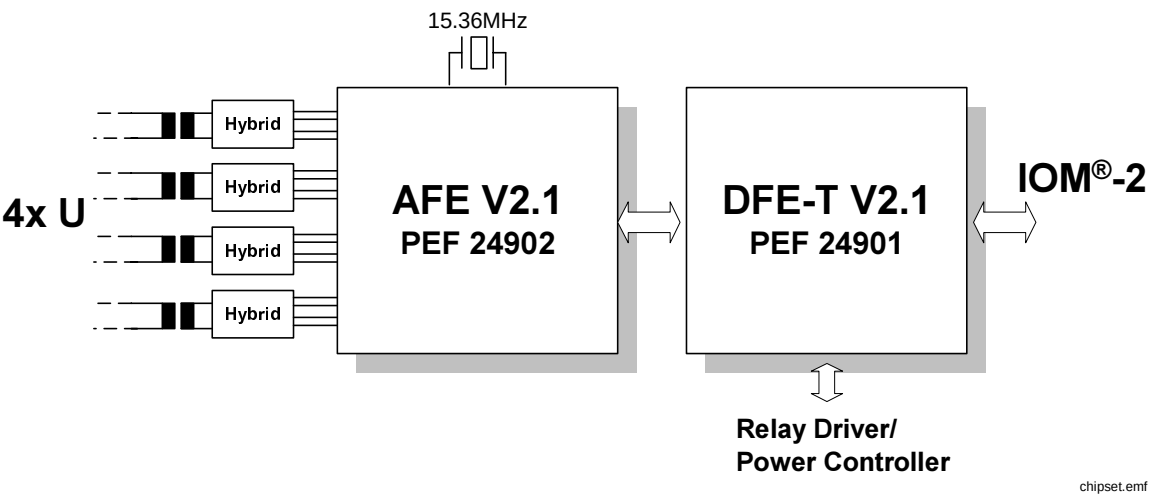


Figure 1-1 DFE-T/ AFE 2nd Generation Chip Set

The output and input pins are throughout 5V TTL compatible although the PEF 24901 is processed in advanced 3.3V CMOS technology. A power down state with very low power consumption is featured.

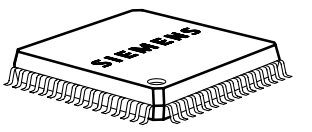
The PEF 24901 comes in a P-MQFP-64 package.

Quad ISDN 4B3T Echocanceller Digital Front End DFE-T V2.1

PEF 24901

Version 2.1 **CMOS**

1.1 Features



P-MQFP-64

U-Interface

- Digital part of a two-chip solution featuring full duplex data transmission and reception over two-wire metallic subscriber loops providing 4x ISDN basic rate access at 144 kbit/s
- Conforms to:
  - FTZ 1TR 220 (1991)
  - ETSI TS 102 080 V1.3.1 (1998)
  - ITU-T I.430 (1995)
- 4B3T-block code at 120-kHz symbol rate
- Subscriber loop length without repeater:
  - up to 4.2 km on 0.4 mm wire
  - up to 8.0 km on 0.6 mm wire
- LT mode
- 1 kbit/s maintenance channel for transmission of data loopback commands, detected transmission errors and transparent messages
- Activation/ deactivation controller
- Adaptive echo cancellation and equalization
- Automatic gain control and polarity adaption
- Clock recovery (frame and bit synchronization)
- Transmission error counters for line monitoring
- Remote and local control of test loops

System Interface

- IOM®-2 interface with programmable data rates (1 Mbit/s to 4 Mbit/s)
- 4 relay driver pins per port addressable by Monitor command
- 2 status pins per port accessible via Monitor channel

Type	Package
PEF 24901	P-MQFP-64

Other Features

- Software compatible to the PEF 24901 V1.2
- Inputs and outputs 5V TTL compatible
- DOUT (open drain) accepts pull-up to 3.3V or 5V
- Advanced low power CMOS technology
- (digital: 0.35µ process)
- Sophisticated power management for restricted power mode
- +3.3V ±0.3V Power Supply
- Extended temperature range (– 40...to 85°C) available
- Boundary-Scan, JTAG IEEE 1149.1

Add-On Features and Differences with Respect to DFE-T V1.2

- +3.3V instead of +5V power supply
- Exchange of transparent messages via Maintenance channel by use of MON-0 commands
- LT-RP mode is not supported
- DOUT configurable either as open drain or push-pull (tristate) output
- Monitor Time-Out (MTO) procedure
- Bit Error Rate measurement per port
- Additional digital local loops
- C/I codes ’LTD’ and ’HI’ are no more supported
- C/I code mnemonics adapted to 2B1Q notation for consistency reasons - coding has been retained unchanged
- State machine notation is aligned to that of 2B1Q for consistency reasons
- New MON-12 class features internal register access
- Coefficients retrievable by MON-12 commands instead of MON-8 commands
- The Boundary-Scan instructions ’CLAMP’ and HIGHZ are supported in version 2.1 (’SSP’ is omitted since for this function a dedicated pin is reserved)
- JTAG Boundary-Scan with dedicated reset line $\overline{\text{TRST}}$ (replaces power-on reset functionality)

1.2 Logic Symbol

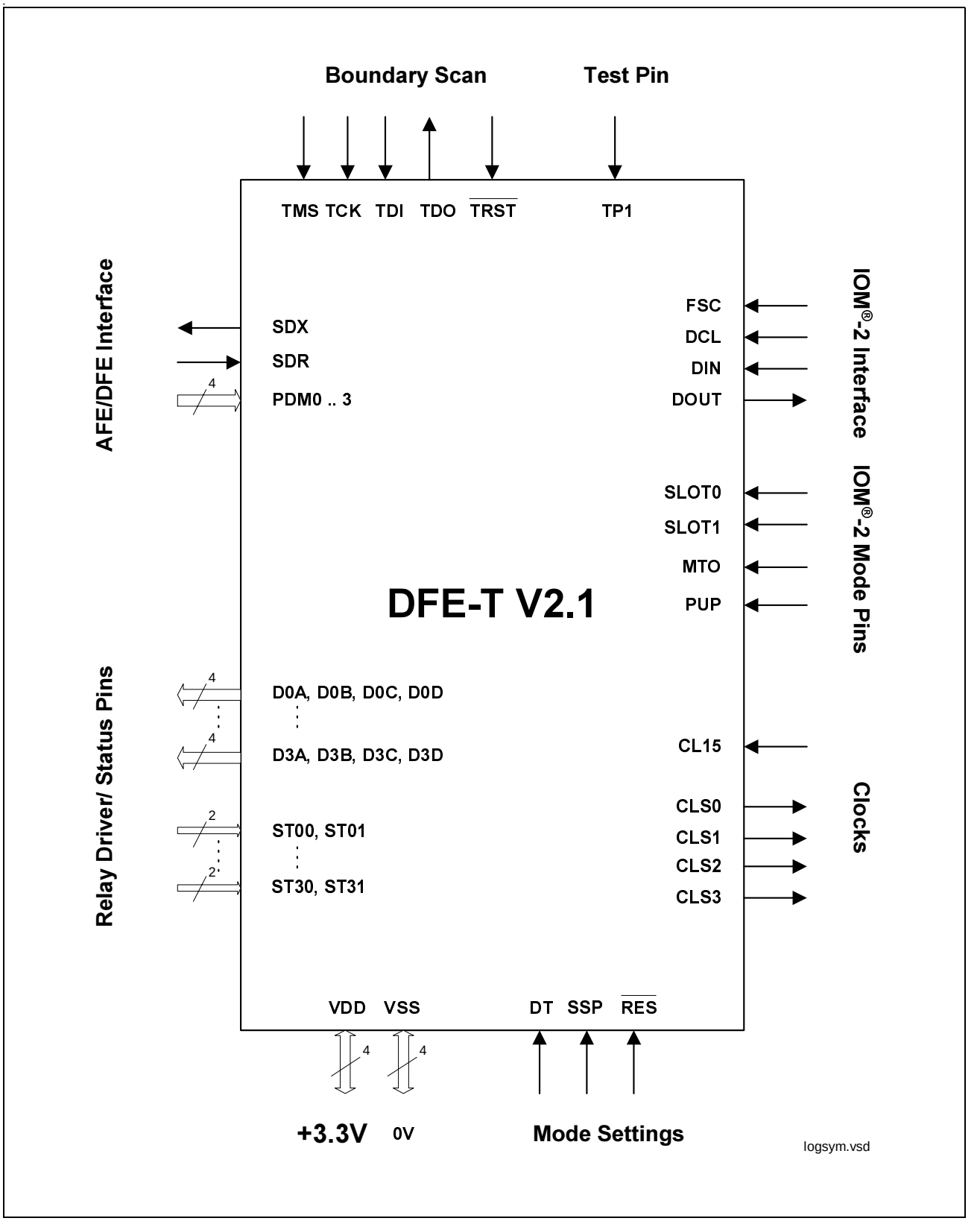


Figure 1-2 Logic Symbol

1.3 System Integration

This paragraph shows how the DFE-T V2.1 may be integrated in systems using other Infineon ISDN devices. The PEF 24901 V2.1 is optimized for use in the following applications:

- Digital Line Cards for Central Office
- Digital Line Cards for Access Networks (LT mode only)
- PBX applications (LT mode only)

Figure 1-3 and **Figure 1-4** illustrate line card solutions with various Infineon line card controllers. The DELPHI (PEB 20570) supersedes the ELIC® (PEB 20550) and will feature up to 32 HDLC controllers on-chip.

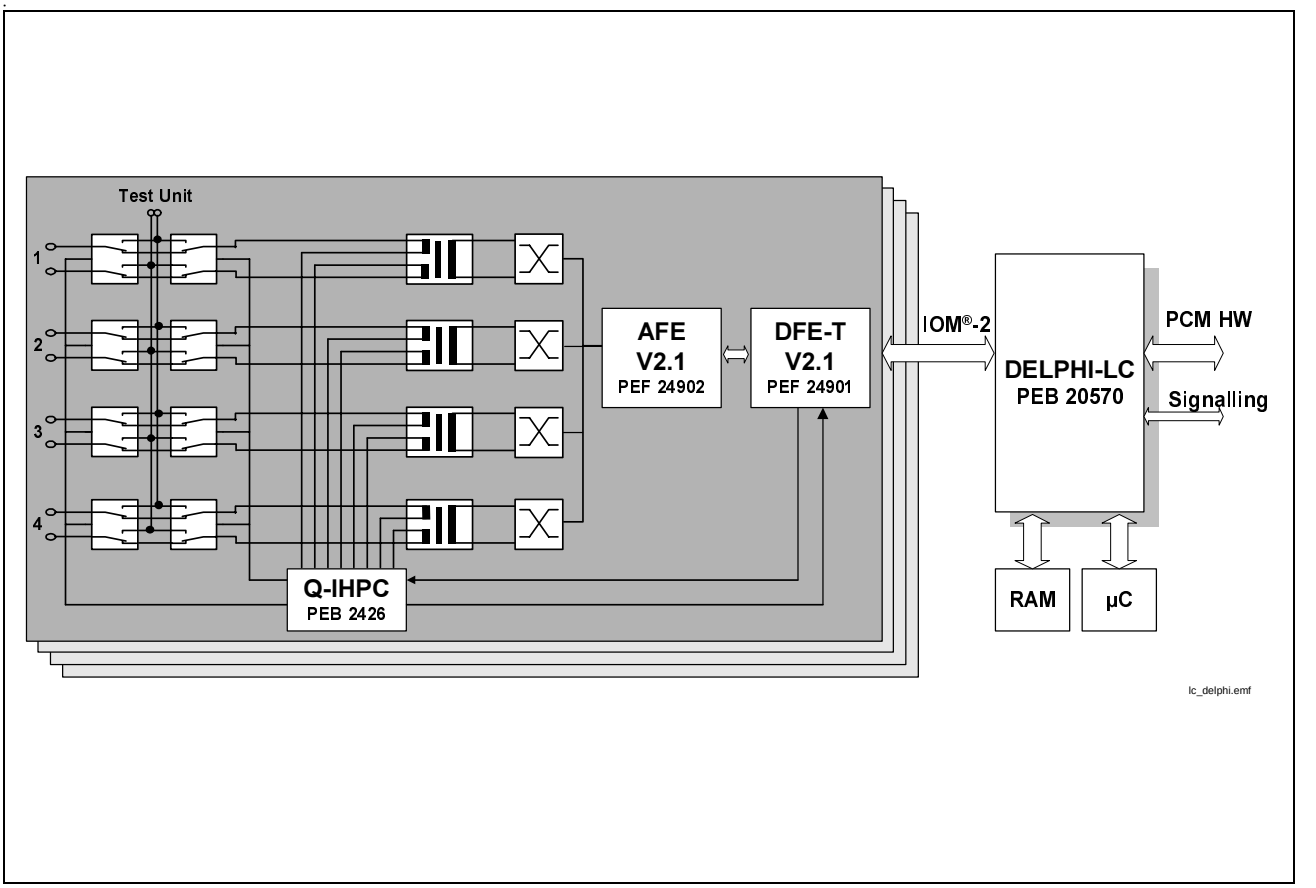


Figure 1-3 16-Line Card Application with DELPHI Solution

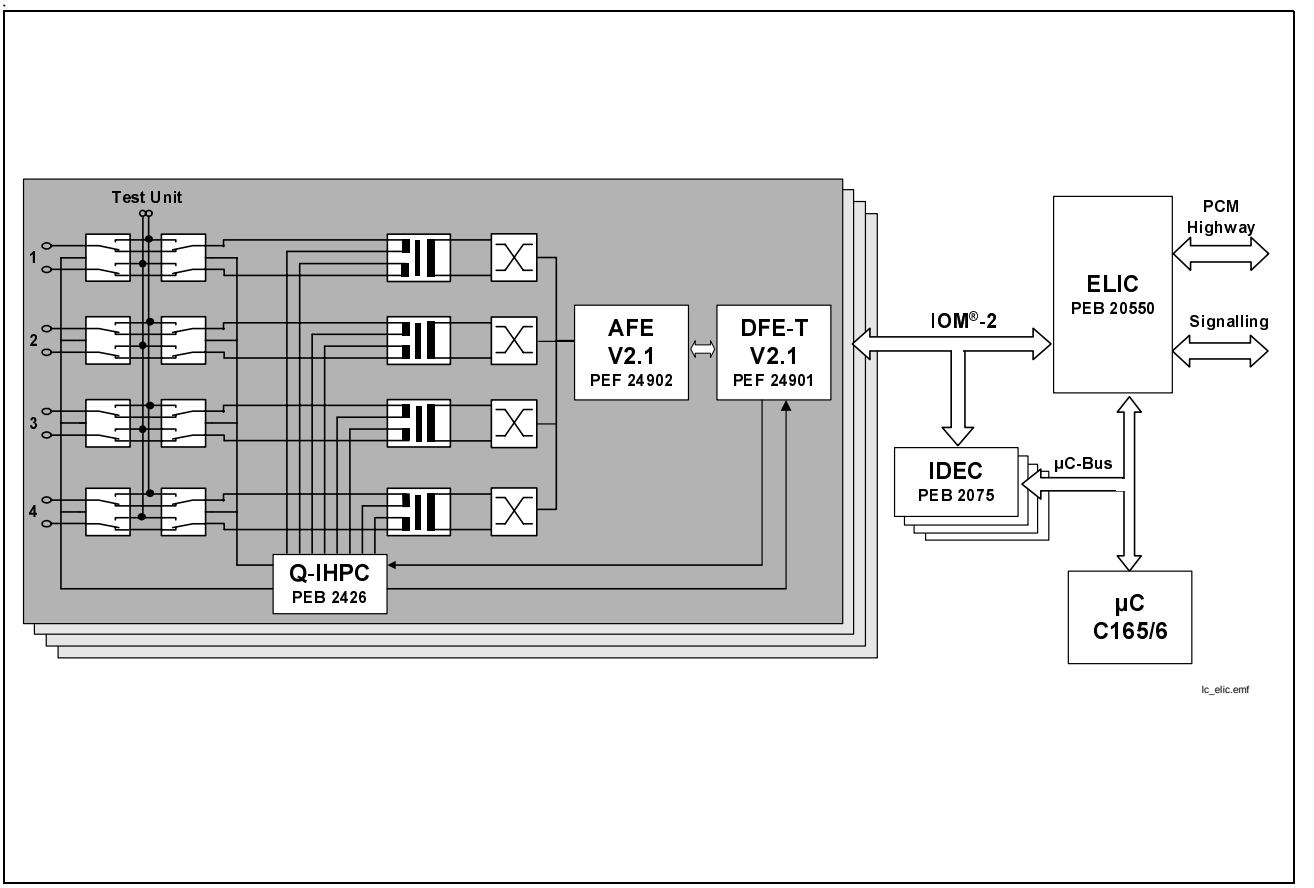


Figure 1-4 16-Line Card Application with ELIC®/ IDEC® Solution

Figure 1-5 shows how a 8 channel line card application is realized by use of two AFE/ DFE-T chip sets:

One AFE PLL generates the synchronized 15.36MHz clock and provides the master clock at pin CL15 for the other 3 devices. The internal PLL of the first AFE synchronizes the 15.36 MHz master clock onto a PTT reference clock of either 8 kHz or 2048 kHz.

The PLL of the second AFE is deactivated. The 15.36 MHz master clock is applied at pin CL15. CL15 is configured as input if XIN is clamped either to VDD or to VSS. Pin XOUT has to be left open and CLOCK shall be tied to GND.

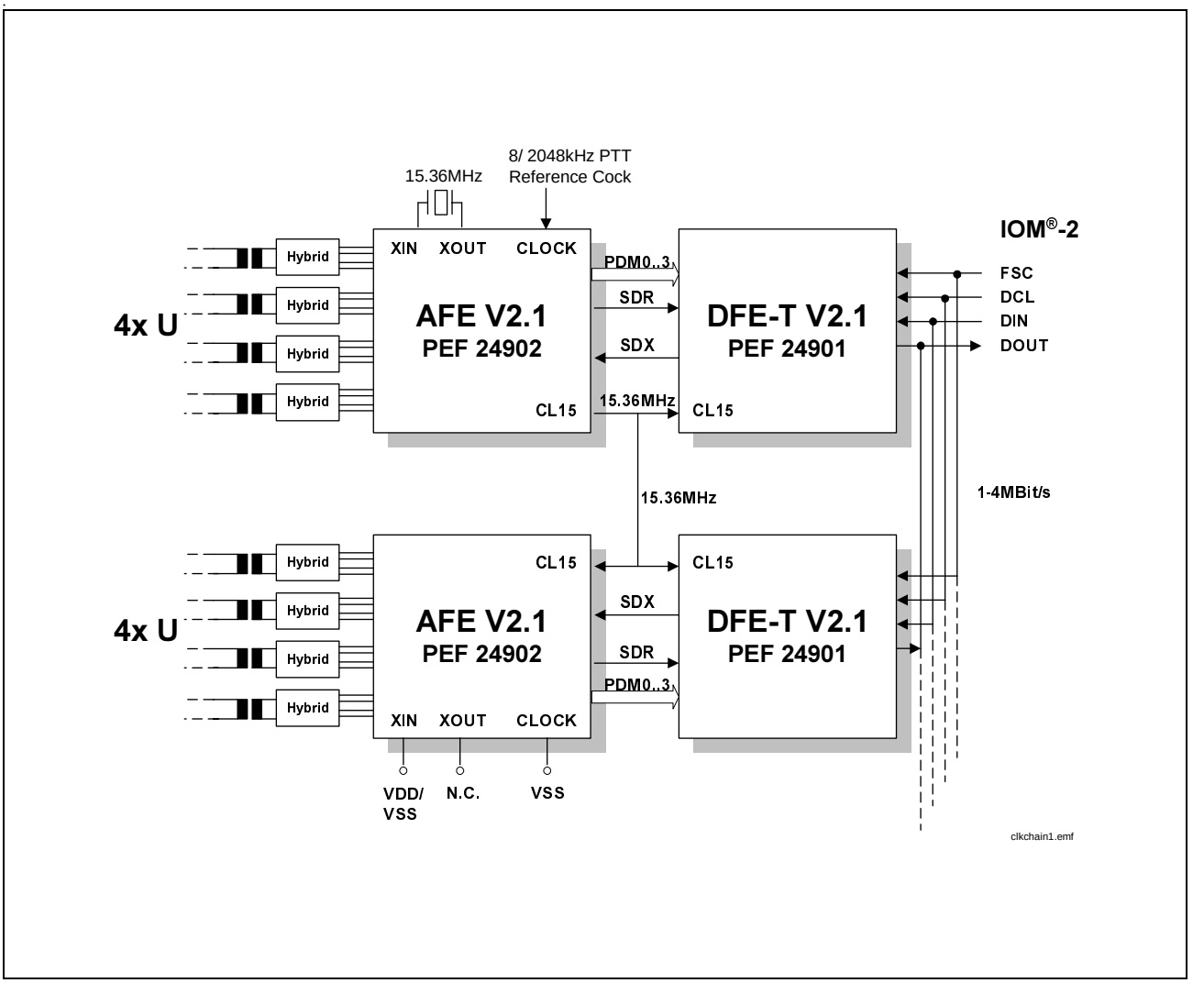


Figure 1-5 Connecting Two AFE/DFE-T Chip Sets

The DFE-T devices are supplied by the first AFE at pin CL15 with the synchronized 15.36MHz clock. The IOM®-2 channels the DFE-T devices are assigned to can be programmed by the two slot pins. Starting from channel no. 0/4/8/12 always four subsequent channels are occupied.

Alternatively the clocking scheme as shown in **Figure 1-6** may be applied if more than 3 devices are to be clocked (e.g. in a 16-channel line card application). Instead to supply the 2nd AFE with the master clock at pin CL15, here the 15.36MHz master clock is input at pin XIN. Thereby pin CL15 is configured as output and passes the 15.36MHz clock on to the attached DFE-T. If the clock chain is extended in the same way by another two AFE/DFE-T chip sets a 16-channel line card application can be realized with just one single crystal. Note that the 15.36MHz clock is inverted once by the AFE if it is input at XIN and output at CL15. This way the duty cycle is recovered again.

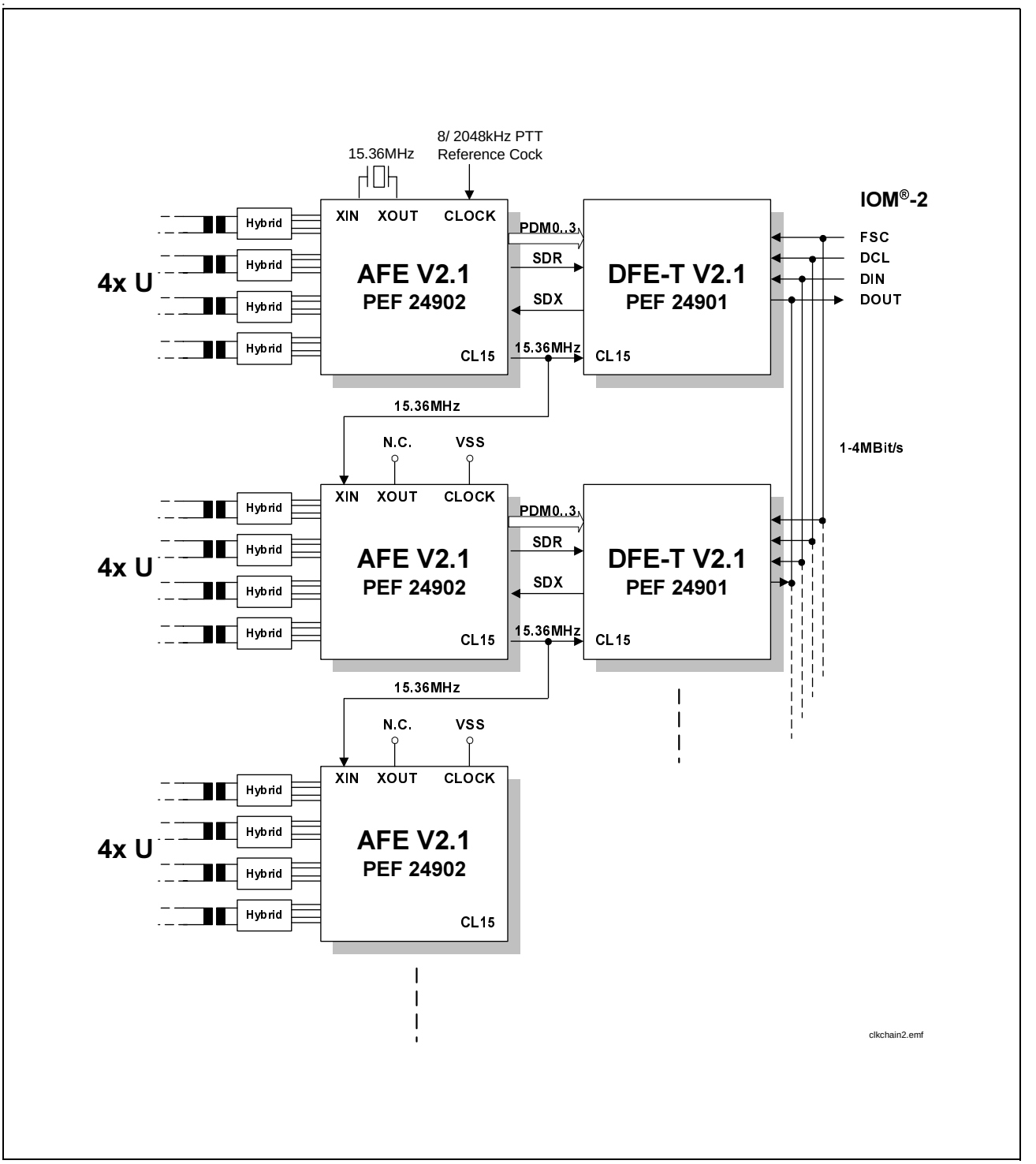


Figure 1-6 Recommended Clocking Scheme for More Than Two DFE-T/AFE Chip Sets

1.4 Operational Overview

The DFE-T V2.1 operates always in LT mode.

System Interface Configurations

The following parameters of the system interface are configurable:

- Open Drain/ Push-Pull Mode
  Configured as open drain the output pin DOUT is floating and a pull-up resistor is required. In push-pull mode the output pin is high impedance outside the active time slots.

- IOM®-2 Channel Assignment
  IOM®-2 channels are always assigned in blocks of four.

SLOT1	SLOT0	Assigned IOM®-2 Channels
0	0	0 .. 3
0	1	4 .. 7
1	0	8 .. 11
1	1	12 .. 15

- IOM®-2 Data Rates

DCL Frequency [kHz]	Data Rate [kBit/s]	IOM®-2 Channels	Remarks
2048	1024	4	
3072	1536	6	
4096	2048	8	LT Burst Mode
6144	3072	12	
8192	4096	16	

Send Single Pulses Test Mode

In test mode ’Send Single Pulses’ +1 pulses spaced by 1ms are transmitted on all U lines. The test mode is activated by pin SSP= set to ’1’. The SSP test function can be as well stimulated by C/I= SSP besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line.

Data Through Mode

In test mode ’Data Through’ the U-transceiver is forced to enter the ’Transparent’ state and to issue U4 independent of the wake-up protocol. The DT test mode is activated by pin DT= set to ’1’. The DT test function can be as well stimulated by C/I= DT besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line.

2 Pin Descriptions

2.1 Pin Diagram

(top view)

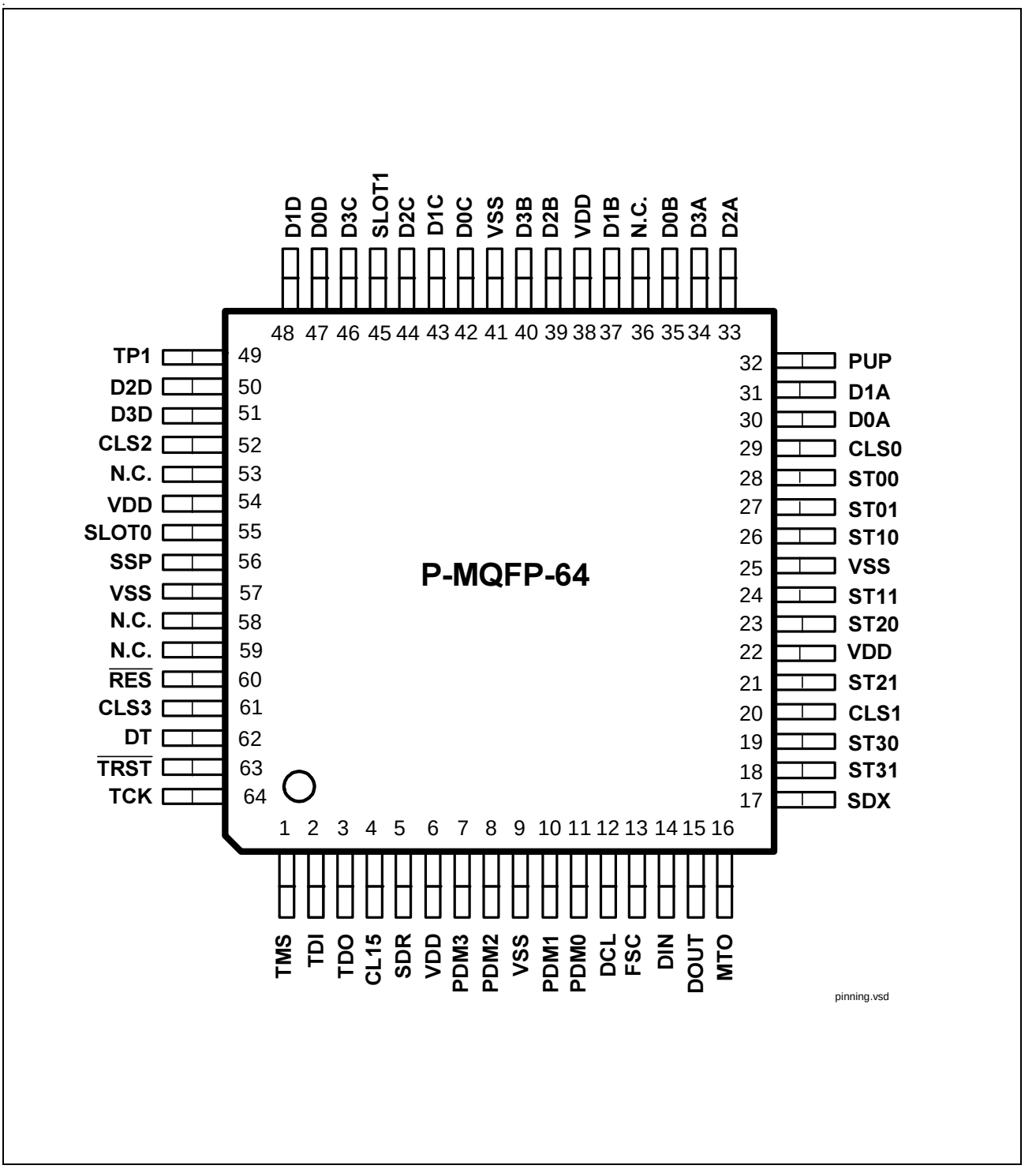


Figure 2-1 Pin Configuration (60 of 64 used)

2.2 Pin Definitions and Functions

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
IOM®-2 Interface			
13	FSC	I	**Frame Synchronization Clock (8kHz)** the start of the first B1-channel in time-slot 0 is marked, FSC is expected to be '1' for at least two DCL periods.
12	DCL	I	**Data Clock** clock rate ranges from 2048 to 8192kHz (1024 to 4096kBit/s)
14	DIN	I	**Data In** input of IOM®-2 data synchronous to DCL clock
15	DOUT	O (OD/ PuP)	**Data Out** output of IOM®-2 data synchronous to DCL clock
Mode Selection Pins			
60	$\overline{\text{RES}}$	I	**Reset** triggers asynchronous HW reset, Schmitt trigger input '1'= inactive '0'= active
55	SLOT0	I	**IOM®-2 Channel Slot Selection 0** assigns IOM®-2 channels in blocks of 4 SLOT1, 0: '00'= IOM®-2 channels 0 to 3 '01'= IOM®-2 channels 4 to 7 '10'= IOM®-2 channels 8 to 11 '11'= IOM®-2 channels 12 to 15
45	SLOT1	I (PD)	**IOM®-2 Channel Slot Selection 1** assigns IOM®-2 channels in blocks of 4, internal pulldown resistor (160kΩ)

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
16	MTO	I (PD)	**Monitor Channel Time-Out** if activated the Monitor channel is reset every 12ms, internal pulldown resistor (160kΩ) '1'= enables 12ms time-out '0'= disables the 12ms time-out
32	PUP	I (PD)	**Push Pull Mode** in push pull mode '0' and '1' is actively driven during an occupied time slot (as soon as 1.FSC was received after reset), outside the active time slots DOUT is high impedance (tristate), internal pulldown resistor (160kΩ) '1'= configures DOUT as push/pull output '0'= configures DOUT as open drain output
56	SSP	I	**Send Single Pulses (SSP) Test Mode** '1'= +1 pulses are issued at all line ports in 1ms intervals '0'= deactivated, clamp to GND if not used *Note: This pin function corresponds to the SW selection by C/I= SSP besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line*
62	DT	I	**Data Through (DT) Test Mode** enables/disables DT test mode '1'= DT test mode enabled, the U-transceiver is forced on all line ports to enter the 'Transparent' state '0'= DT test mode disabled *Note: This pin function corresponds to the SW selection by C/I= DT besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line*

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Interface to the Analog Front End			
4	CL15	I	**15.36MHz Master Clock Input**
11	PDM0	I	**Pulse Density Modulated Receive Data of Line Port 0** pulse density modulated bit stream from the PEB 24902 Quad AFE that is output from the second-order sigma-delta ADC
10	PDM1	I	**Pulse Density Modulated Receive Data of Line Port 1** pulse density modulated bit stream from the PEB 24902 Quad AFE that is output from the second-order sigma-delta ADC
8	PDM2	I	**Pulse Density Modulated Receive Data of Line Port 2** pulse density modulated bit stream from the PEB 24902 Quad AFE that is output from the second-order sigma-delta ADC
7	PDM3	I	**Pulse Density Modulated Receive Data of Line Port 3** pulse density modulated bit stream from the PEB 24902 Quad AFE that is output from the second-order sigma-delta ADC
5	SDR	I	**Serial Data Receive Line** interface signal from the PEB24902 Quad AFE that transports level detect information for the wake-up recognition of all 4 lines by use of TDM

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
17	SDX	O	**Serial Data Transmit Line** interface to the PEB24902 Quad AFE for the transmit and control data. Transmission is based on clock CL15 (15.36 Mbit/s). For each line port the following bits are exchanged: TD0, TD1: Transmit data RANGE: Range select LOOP: Analog loopback switch PDOW: Power down/power up Synchronization information
Relay Driver/ Status Pins			
30, 35, 42, 47	D0A D0B D0C D0D	O	**Relay Driver Pins of Line Port 0** addressable via MON-8 command in IOM®-2 channel 0/4/8/12. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.
31, 37, 43, 48	D1A D1B D1C D1D	O	**Relay Driver Pins of Line Port 1** addressable via MON-8 command in IOM®-2 channel 1/5/9/13. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.
33, 39, 44, 50	D2A D2B D2C D2D	O	**Relay Driver Pins of Line Port 2** addressable via MON-8 command in IOM®-2 channel 2/6/10/14. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
34, 40, 46, 51	D3A D3B D3C D3D	O	**Relay Driver Pins of Line Port 3** addressable via MON-8 command in IOM®-2 channel 3/7/11/15. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.
28, 27	ST00 ST01	I	**Status Pin of Line Port 0** change of status is passed to IOM®-2 channel 0/4/8/12 via the MON-8 message 'AST' at bit positions $S_{0,}$ S_1. Connect to either VDD or VSS if not used.
26, 24	ST10 ST11	I	**Status Pin of Line Port 1** change of status is passed to IOM®-2 channel 1/5/9/13 via the MON-8 message 'AST' at bit positions $S_{0,}$ S_1. Connect to either VDD or VSS if not used.
23, 21	ST20 ST21	I	**Status Pin of Line Port 2** change of status is passed to IOM®-2 channel 2/6/10/14 via the MON-8 message 'AST' at bit positions $S_{0,}$ S_1. Connect to either VDD or VSS if not used.
19, 18	ST30 ST31	I	**Status Pin of Line Port3** change of status is passed to IOM®-2 channel 3/7/11/15 via the MON-8 message 'AST' at bit positions $S_{0,}$ S_1. Connect to either VDD or VSS if not used.

Test Pins

29	CLS0	O	**120kHz Transmit Baud Clock of Port 0** can be used for monitoring and test purposes
20	CLS1	O	**120kHz Transmit Baud Clock of Port 1** can be used for monitoring and test purposes
52	CLS2	O	**120kHz Transmit Baud Clock of Port 2** can be used for monitoring and test purposes

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
61	CLS3	O	**120kHz Transmit Baud Clock of Port 3** can be used for monitoring and test purposes
49	TP1	I	**Test Pin 1** Not available to user. Connect to GND.
JTAG Boundary Scan			
64	TCK	I	**Test Clock**
1	TMS	I (PU)	**Test Mode Select** internal pullup resistor (160kΩ)
2	TDI	I (PU)	**Test Data Input** internal pullup resistor (160kΩ)
3	TDO	O	**Test Data Output**
63	$\overline{\text{TRST}}$	I (PU)	**JTAG Boundary Scan Disable** resets the TAP controller state machine (asynchronous reset), active low internal pullup (160kΩ) '1'= reset inactive '0'= reset active
Power Supply Pins			
6, 22, 38, 54	VDD		3.3V ±0.3V supply voltage
9, 25, 41, 57	VSS		0V ground

OD: Open Drain
PuP: Push Pull
PD: Internal Pull Down
PU: Internal Pull Up

2.3 Pinning Changes from DFE-T V1.2 to DFE-T V2.1

Table 2-2 Pinning Changes

Pin No.	V2.1	V1.2	Comment
16	MTO	N.C.	activates the Monitor Time-Out procedure as provided in IEC-Q
32	PUP	SLOT2	additional push-pull mode eases interface adaption, SLOT2 was not used in V1.2
49	TP1	TP3	renamed
53	N.C.	LT	as in V1.x LT-RP mode is neither supported in V2.1
56	SSP	TSP	dedicated pin for ’Send Single Pulses’ test mode
62	DT	TP	dedicated pin for ’Data Through’ test mode
63	$\overline{\text{TRST}}$	TP1	power-on-reset is replaced by a dedicated reset line

3 Functional Description

3.1 Functional Overview

A functional overview of the DFE-T V2.1 is given in **Figure 3-1**. Besides the signal processing and frame formatting blocks the PEF 24901 features an on-chip activation/ deactivation controller and programmable general purpose I/O pins for the control of test relays and power feeding circuits. An application specific DSP core services all four lines and cuts chip size to a minimum.

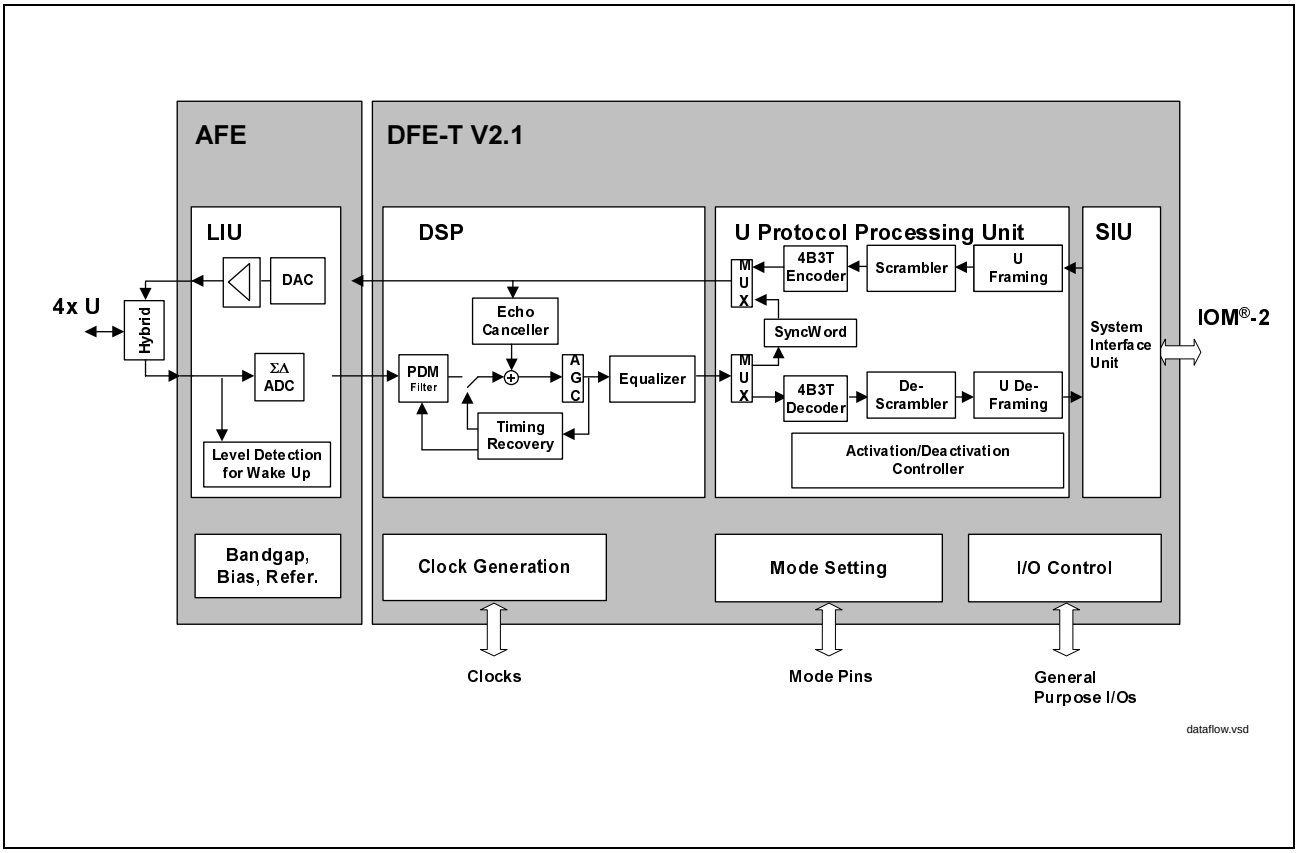


Figure 3-1 Data Flow Diagram (DFE-T V2.1 + AFE)

3.2 Block Diagram

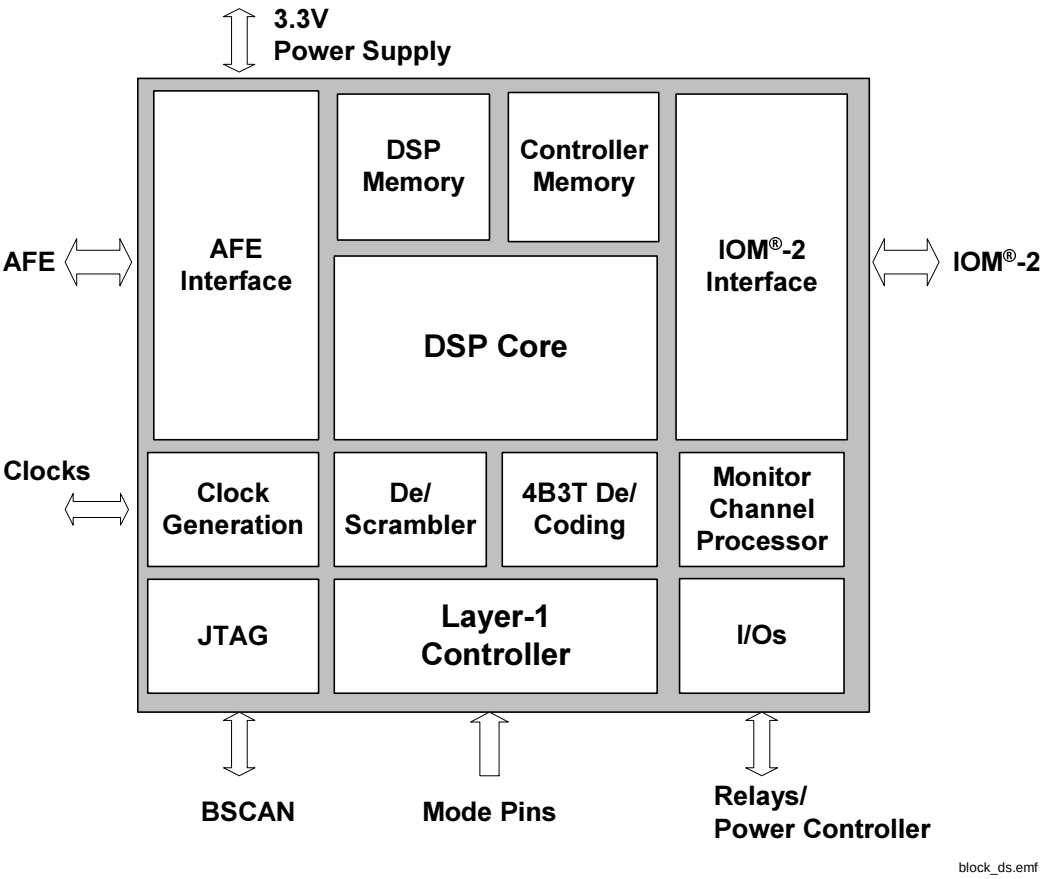


Figure 3-2 DFE-T V2.1 Block Diagram

3.3 IOM®-2 Interface

The IOM®-2 interface is a four-wire serial interface providing a symmetrical full-duplex communication link to layer-1 and layer-2 backplane devices. It transports user data, control/programming and status information via dedicated time multiplexed channels.

The structure used follows the 2B + 1 D-channel structure of ISDN. The ISDN-user data rate of 144 kbit/s (B1 + B2 + D) on the U-interface is transmitted transparently in both directions (U <=> IOM®) over the interface.

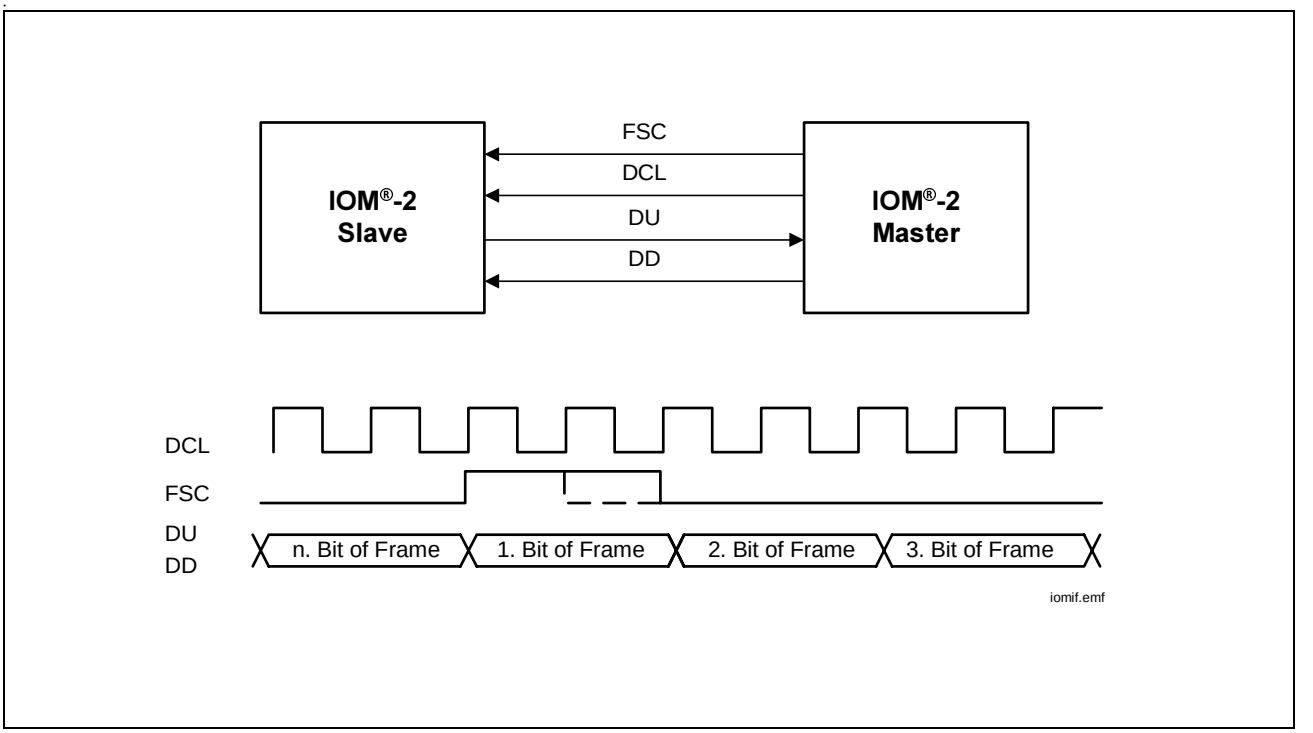


Figure 3-3 Clock Supply and Data Exchange between Master and Slave

The **Frame Sync Signal FSC** is a 8 kHz signal delimiting the frames. This signal is used to determine the start of a frame.

The data is clocked by a **Data Clock (DCL)** which operates at twice the data rate. The data clock is a square wave signal with a duty cycle ratio of typically 1:1. Incoming data is sampled on the falling edge of the DCL-clock.

Data is carried over **Data Upstream (DD)** and **Data Downstream (DU)** signals. The upstream and downstream directions are always defined with respect to the exchange: Downstream refers to information flowing from the exchange to the subscriber, upstream is defined vice versa.

The output line is operating either as open drain or push-pull output. Both modes are selected by signal “PUP”. In open drain mode an external pull-up resistor is required. The absence of a pull-up resistor is not automatically recognized (i.e. no push-pull detection).

Within one FSC-period, 128 to 512 bit are transmitted, corresponding to DCL-frequencies ranging from 2048 kHz up to 8192 kHz. The following table shows possible operating frequencies of the IOM®-2-interface.

Table 3-1 IOM®-2 Data Rates

DCL Frequency [kHz]	Data Rate [kBit/s]	IOM®-2 Channels	Remarks
2048	1024	4	
3072	1536	6	
4096	2048	8	LT Burst Mode
6144	3072	12	
8192	4096	16	

3.3.1 IOM®-2 Interface Frame Structure

The typical IOM®-2 line card application comprises a DCL-frequency of 4096 kHz with a nominal bit rate of 2048 kbit/s. Therefore eight channels are available, each consisting of the basic frame with a nominal data rate of 256 kbit/s. The downstream data (DD) is transferred on signal DIN, the upstream data (DU) on signal DOUT. The IOM®-2 channel assignment is programmable by pin strapping (SLOT1,0).

The basic IOM®-2 frame and clocking structure consists of:

channel bits	B1	B2	Monitor	D	Command / Indicate	MR	MX
	8	8	8	2	4	1	1

- Two 64-kbit/s channels B1 and B2
- The monitor channel for transferring maintenance information between layer-1 and layer-2 devices
- Two bits for the 16-kbit/s D-channel
- Four command / indication (C/I) bits for controlling of layer-1 functions (activation/ deactivation and additional control functions) by the layer-2 controller
- Two bits MR and MX for handling the monitor channel

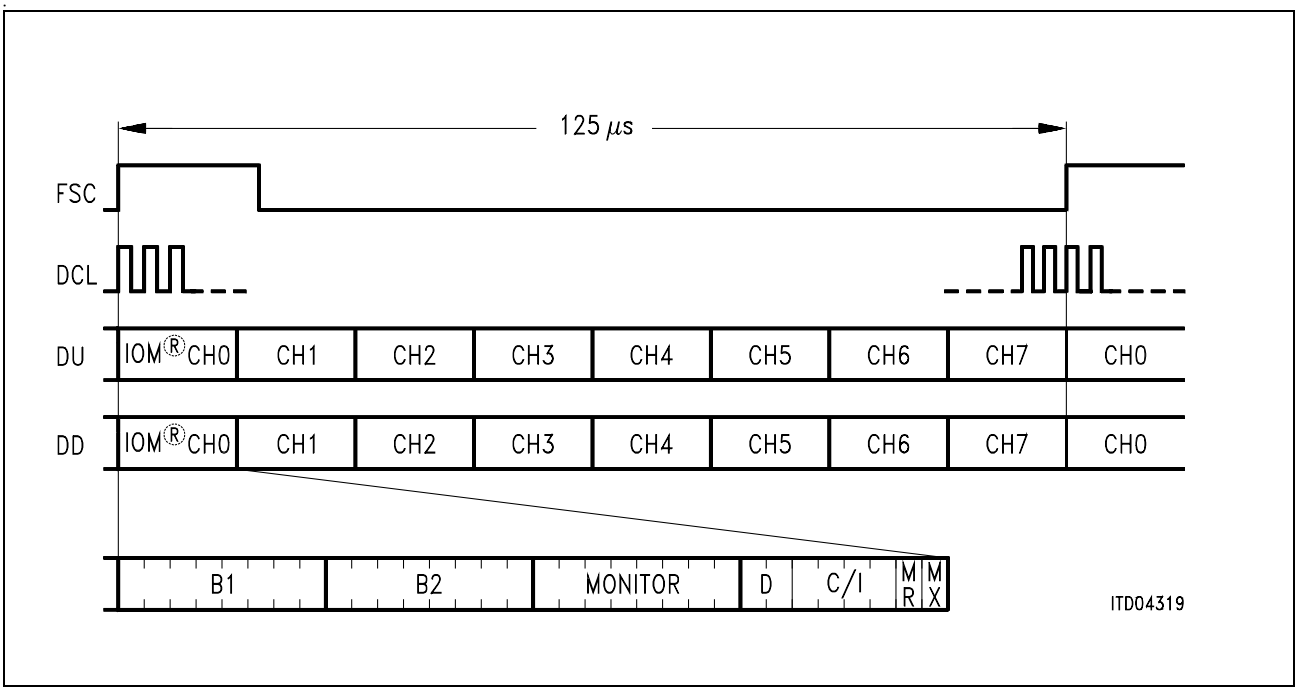


Figure 3-4 Multiplexed Frame Structure of the IOM®-2 Interface

3.3.2 IOM®-2 Command/ Indicate Channel

The Command/Indication (C/I) channel carries real-time control and status information between the DFE-T V2.1 and a layer-1 control device. A new C/I code must be detected in two consecutive IOM®-2 frames to be considered valid (double last look criterion). An indication is issued permanently by the DFE-T V2.1 on DOUT until a new indication needs to be forwarded.

The C/I code is 4 bit wide and located at bit positions 27–30 in each time-slot. A listing and explanation of the U-transceiver C/I codes can be found on page 3-32.

3.3.3 IOM®-2 Monitor Channel

The Monitor channel represents a second method of initiating and reading U-transceiver specific information. Features of the monitor channel are supplementary to the command/indicate channel. Unlike the command/indicate channel with an emphasis on status control, the monitor channel provides access to internal bits (maintenance, overhead) and test functions (local loop-backs, block error counter and self-test).

Besides the known MON-8 commands two new MON classes, MON-0 and MON-12 are introduced in the DFE-T V2.1:

- **New MON-0 Class**
  Like in the 2B1Q version MON-0 messages allow the user to transfer transparent

messages across the U-interface.

- **New MON-12 Class**
  By use of MON-12 commands the DFE-T V2.1 provides the ability to address parts of the device internal register map and thus to address functions that have been added with version 2.1. MON-12 commands are always prioritized and processed first if other Monitor commands are outstanding. See Chapter 3.3.4 for the details.

This means that Monitor commands are split into three categories. Each category derives its name from the first nibble (4 bits) of the two byte long message. These are:

- MON-12 (Internal Register Map)
- MON-0 (Transparent Channel)
- MON-8 (Local Functions)

The order of the list above corresponds to the priority attributed to each category. MON-12 commands are always processed first. MON-0 messages will be transmitted before MON-8 messages in case several messages are initiated simultaneously. The various MON-0 and MON-8-commands are discussed in detail in chapter "Monitor Commands" on page 5-1.

Structure

The structure of the Monitor channel is 8 bit wide, located at bit position 17 – 24 in every time-slot. Monitor commands/messages sent to/from the U-transceiver are always 2 bytes long.

Transmission of multiple monitor bytes is specified by IOM®-2 (see next section “Handshake Procedure” for details). For handshake control in multiple byte transfers, bit 31, monitor read “MR”, and bit 32, monitor transmit “MX”, of every time-slot are used.

Verification

A double last-look criterion is implemented for the monitor channel. If the monitor message that was received consecutively after a change has been detected is not identical to the message that was received before the message will be aborted.

Handshake Procedure

IOM®-2 provides a sophisticated handshake procedure for the transfer of monitor messages. For handshake control two bits, MX and MR, are assigned to each IOM®-2 frame (on DIN and DOUT). The monitor transmit bit (MX) indicates when a new byte has been issued in the monitor channel (active low). The transmitter postpones transmitting the next information until the correct reception has been confirmed. A correct reception will be confirmed by setting the monitor read bit (MR) to low.

The monitor channel is full duplex and operates on a pseudo-asynchronous base, i.e. while data transfer on the bus takes place synchronized to frame synchronization, the flow of monitor data is controlled by the MR- and MX-bits. Monitor data will be transmitted repeatedly until its reception is acknowledged.

Figure 3-5 illustrates a monitor transfer at maximum speed. The transmission of a 2-byte monitor command followed by a 2-byte response requires a minimum of 15 IOM®-2 frames (reception 7 frames + transmission 8 frames = 1.875 ms). In case the controller is able to confirm the receipt of first response byte in the frame immediately following the MX-transition on DOUT from high to low (i.e. in frame No. 9), 1 byte may be saved (7 frames + 7 frames).

Transmission and reception of monitor messages can be performed simultaneously by the U-transceiver. In the procedure depicted in **Figure 3-5** it would be possible for the U-transceiver to transmit monitor data in frames 1–5 (excluding EOM-indication) and receive monitor data from frame 8 onwards.

M 1/2: Monitor message 1. and 2. byte
R 1/2: Monitor response 1. and 2. byte

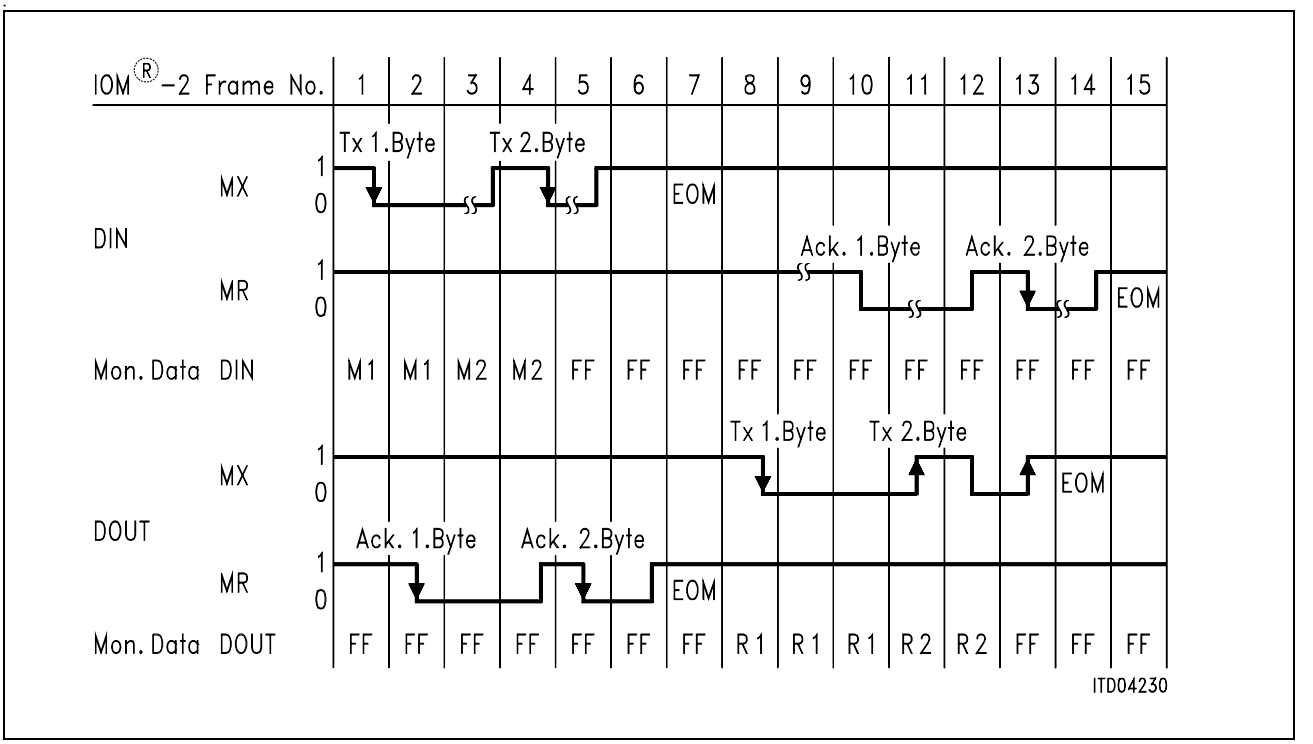


Figure 3-5 Handshake Protocol with a 2-Byte Monitor Message/Response

Idle State

After the bits MR and MX have been held inactive (i.e. high) for two or more successive IOM®-frames, the channel is considered idle in this direction.

Standard Transmission Procedure

1. The first byte of monitor data is placed by the external controller on the DIN line of the DFE-T V2.1 and MX is activated (low; frame No. 1).
2. The DFE-T V2.1 reads the data of the monitor channel and acknowledges by setting the MR-bit of DOUT active if the transmitted bytes are identical in two received frames (frame No. 2 because data are already read and compared while the MX-bit is not activated).
3. The second byte of monitor data is placed by the controller on DIN and the MX-bit is set inactive for one single IOM®-frame. This is performed at a time convenient to the controller.
4. The DFE-T V2.1 reads the new data byte in the monitor channel after the rising edge of MX has been detected. In the frame immediately following the MX-transition active-to-inactive, the MR-bit of DOUT is set inactive. The MR-transition inactive-to-active exactly one IOM®-frame later is regarded as acknowledgment by the external controller (frame No. 4–5).
   The acknowledgment by the DFE-T V2.1 will always be sent two IOM®-frames after the activation of a new data byte.
5. After both monitor data bytes have been transferred to the DFE-T V2.1, the controller transmits “End Of Message” (EOM) by setting the MX-bit inactive for two or more IOM®-frames (frame No. 5–6).
6. In the frame following the transition of the MX-bit from active to inactive, the DFE-T V2.1 sets the MR-bit inactive (as was the case in step 4). As it detects EOM, it keeps the MR-bit inactive (frame No. 6). The transmission of the monitor command by the controller is complete.
7. If the DFE-T V2.1 is requested to return an answer it will commence with the response as soon as possible. In case the “monitor time out” function is enabled it may have to postpone the answer until after the internal reset (see section Monitor Procedure Time-out for details). **Figure 3-5** illustrates the case where the response can be sent immediately.
   The procedure for the response is similar to that described in points 1 – 6 except for the transmission direction. It is assumed that the controller does not latch monitor data. For this reason one additional frame will be required for acknowledgment.
   Transmission of the 2nd monitor byte will be started by the DFE-T V2.1 in the frame immediately following the acknowledgment of the first byte. The U-transceiver does not delay the monitor transfer.

Transmission Abortion

If no EOM is detected after the first two monitor bytes, or received bytes are not identical in the first two received frames, transmission will be aborted through receiver by setting the MR-bit inactive for two or more IOM®-2-frames. The controller reacts with EOM. This situation is illustrated in **Figure 3-6**.

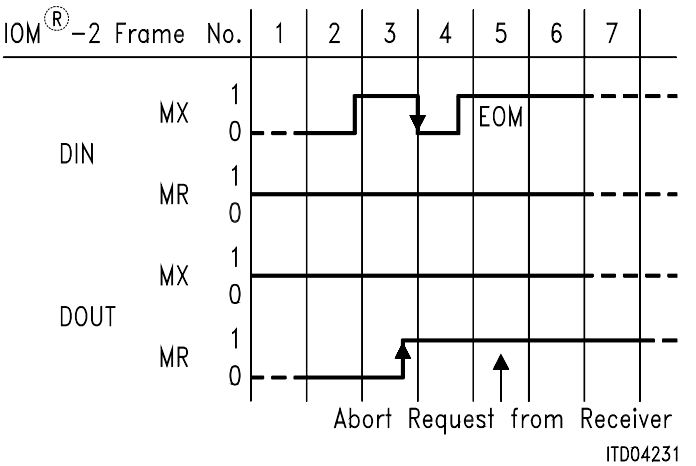


Figure 3-6 Abortion of Monitor Channel Transmission

MONITOR Procedure Time-Out (MTO)

The DFE-T V2.1 offers an internal reset (monitor procedure “Time-out”) for the monitor routine. This reset function transfers the monitor channel into the idle state (MR and MX set to high) thereby resolving possible lock-up situations. It therefore is to be used in all systems where no microprocessor is capable of detecting and solving hang-up situations in the monitor procedure.

The reset procedure is started in 12 ms intervals. In order to avoid the loss of transmitted or received data the DFE-T V2.1 commences a monitor transfer only when enough time is available before the next reset will be initiated. If this is not the case transmission is postponed until after the reset.

Once a message has been issued on IOM®-2, its transfer needs to be completed before the next reset. If this is not accomplished, the message can be lost without notice. For this reason the control software should be able to transfer monitor messages as quickly as possible.

Signal “MTO” set to ’1’ enables the MTO-function, signal “MTO” set to ’0’ disables it.

With the MTO-function enabled, the monitor routine is reset every 12ms. Every reset sets both handshake bits of DOUT to the idle state (MR and MX set to high) thereby preventing lock-up situations. The MX and MR are reset synchronously.

With the MTO-function disabled no internal resets are performed. In this case an external controller must prevent lock-up situations in the monitor channel.

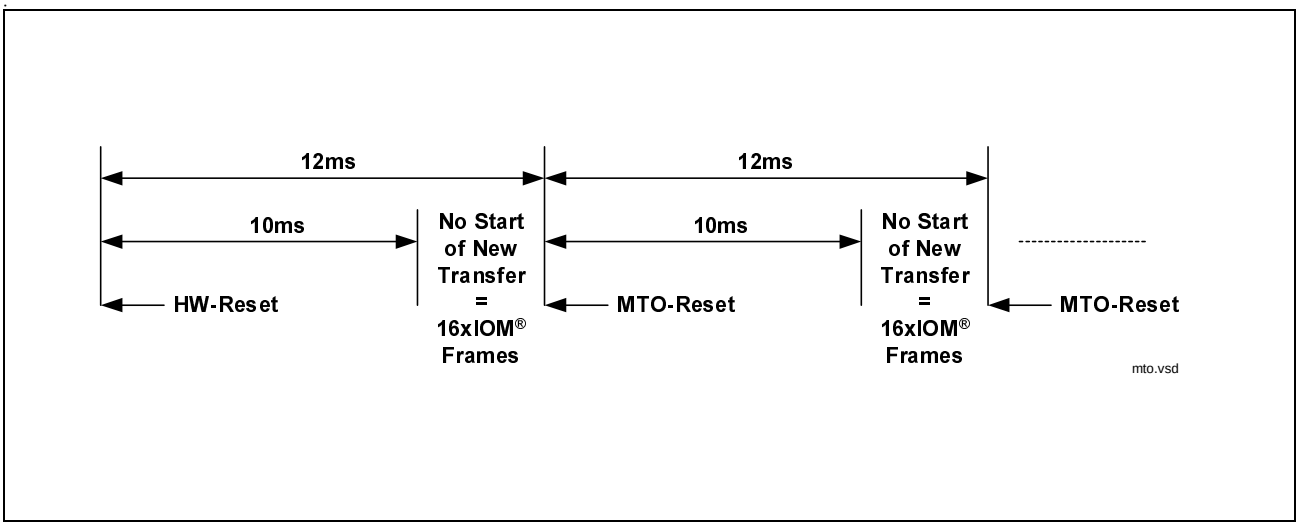


Figure 3-7 Monitor Access with MTO Enabled

Note that there is no relationship of the reset timing to the U-frame, since no superframe exists as for the 2B1Q line code.

DFE-T V2.1 operates as Transmitter with MTO Enabled

The transmitter is reset in 12ms intervals as shown in the figure above. In case the transmission of a monitor message has not been completed before the transmitter is reset, the complete message will be lost. A message that has been lost due to the interruption of a monitor reset will not be retransmitted.

To prevent this loss of monitor messages, the DFE-T V2.1 will only commence a monitor transmission if more than 16 IOM®-2 frames will be available for transmission before the next reset occurs. To ensure correct transmission the receiver must not delay the receive procedure for more than the following value:

2-byte transmission: max. speed = 8 frames => max. controller (receive) delay = 8 frames

DFE-T V2.1 operates as Receiver with MTO Enabled

The receiver is reset in 12ms intervals as shown in the figure above. In case the reception of a monitor message has not been completed before the receiver is reset, the complete message can be lost because the generation of an abort request can not be guaranteed.

To prevent this loss of monitor messages the DFE-T V2.1 will only commence a monitor reception (i.e. acknowledge the 1st received byte) if more than 16 IOM®-2 frames will be available for reception before the next reset occurs. Reception thus does not start if there is less than 2ms (=16x IOM®-2 frames) time left. To ensure correct reception, the transmitter must not delay the receive procedure for more than the following value:

2-byte reception: max. speed = 7 frames => max. controller (transmit) delay = 9 frames

3.3.4 MON-12 Protocol

MON-12 commands feature direct access to the device internal register map via the Monitor channel. This means that although the DFE-T V2.1 features no microcontroller interface internal register functions can be directly addressed by use of MON-12 commands.

A MON-12 read request command must be first acknowledged by the DFE-T V2.1 before a subsequent read request can be triggered. In case of a failure condition the DFE-T V2.1 repeats the last outstanding MON-12 answer. MON-12 commands are prioritized over the other MON classes.

If U-interface functions are addressed then the value of register LP_SEL determines the register bank of the channel that is referred to. As a result the desired line port number must be programmed first in register LP_SEL before any U-interface register can be accessed. For this reason MON-12 commands may not be issued simultaneously on different IOM®-2 channels, but must be issued consecutively if they address U-interface functions.

For registers that are addressable by MON-12 commands please refer to the register map in Chapter 6.2 on page 6-4.

MON-12 commands are of the following format:

- A MON-12 **write command** comprises 3 bytes, the first byte contains the MON-12 header, the second byte the register address, the third byte the register value.

1. Byte		2. Byte		3. Byte	
1100	w=1 0 0 0	A A A A	A A A A	D D D D	D D D D
MON-12		Register Address		Register Value	

- A MON-12 **read request command** comprises 2 bytes, the first byte contains the MON-12 header, the second byte the register address of the data that is requested.

1. Byte		2. Byte	
1100	r=0 0 0 0	A A A A	A A A A
MON-12		Register Address	

- After a read request the DFE-T V2.1 reacts with a 3-byte message. A MON-12 **read answer** comprises 3 bytes, the first byte contains the MON-12 header, the second byte the register address, the third byte the register value.

1. Byte		2. Byte		3. Byte	
1100	r=0 0 0 0	A A A A	A A A A	D D D D	D D D D
MON-12		Register Address		Register Value	

3.4 Interface to the Analog Front End

The interface to the PEF 24902 AFE V2.1 is a 6-wire interface (see **Figure 3-8**). On SDX and SDR transmit and receive data is exchanged as well as control information for the start-up procedure by means of time division multiplexing.

On **SDX** transmit data, power-up/down information, range function and analog loopback requests are transferred.

On **SDR** level status information is received for all line ports.

On **PDM0..PDM3** the ADC output data from the AFE is transferred to the DFE-T V2.1. The timing of all signals is based on the 15.36MHz master clock which is provided by the AFE.

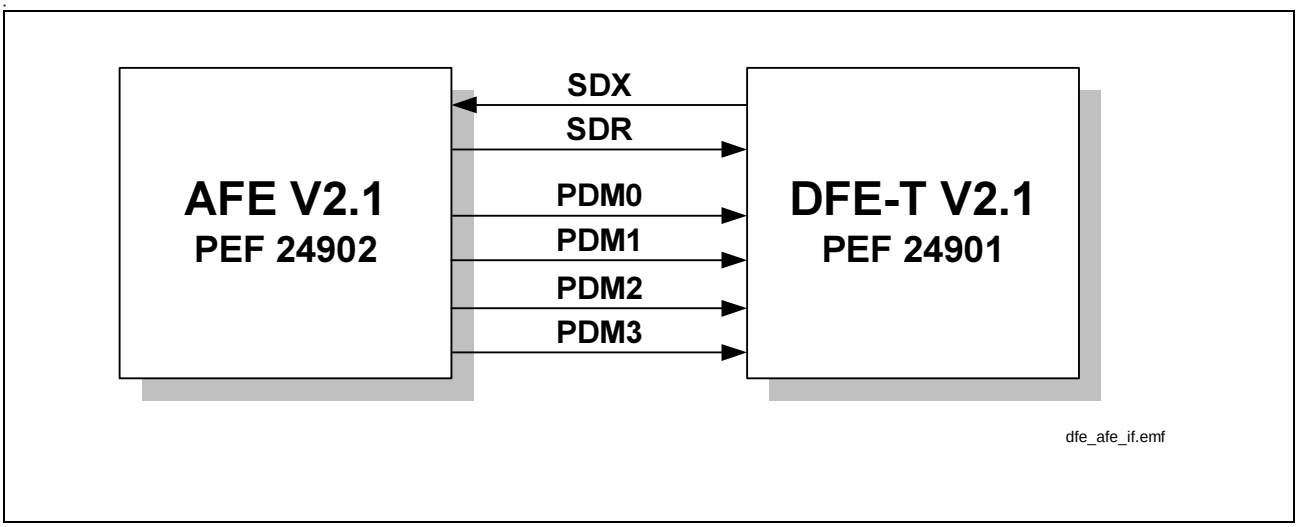


Figure 3-8 Interface to the Analog Front End

The 128 available bits (related to the 15.36 MHz clock) on SDR/SDX during a 120 kHz period are divided into 9 time-slots. 8 time-slots are 13 bits long and are reserved for data transmission, 1 time-slot is 24 bits long and used for synchronization purposes. The DFE-T V2.1 uses four of them, time-slots no. 1, 3, 5 and 7. **Table 3-2** shows the assignment of the IOM®-2 channels to the time-slots on SDX/SDR and the assignment of the time-slots to the line ports.

Table 3-2 Assignments of IOM® Channels to Time-Slots No. on SDX/SDR and Line Ports No.

IOM®-2 Channel No.	Time-Slot No.	Line Port No.
0/4/8/12	1	0
1/5/9/13	3	1
2/6/10/14	5	2
3/7/11/15	7	3

The status on SDR is synchronized to SDX. Each time-slot on SDR carries the corresponding LD bit during the last 12 bits of the slot.

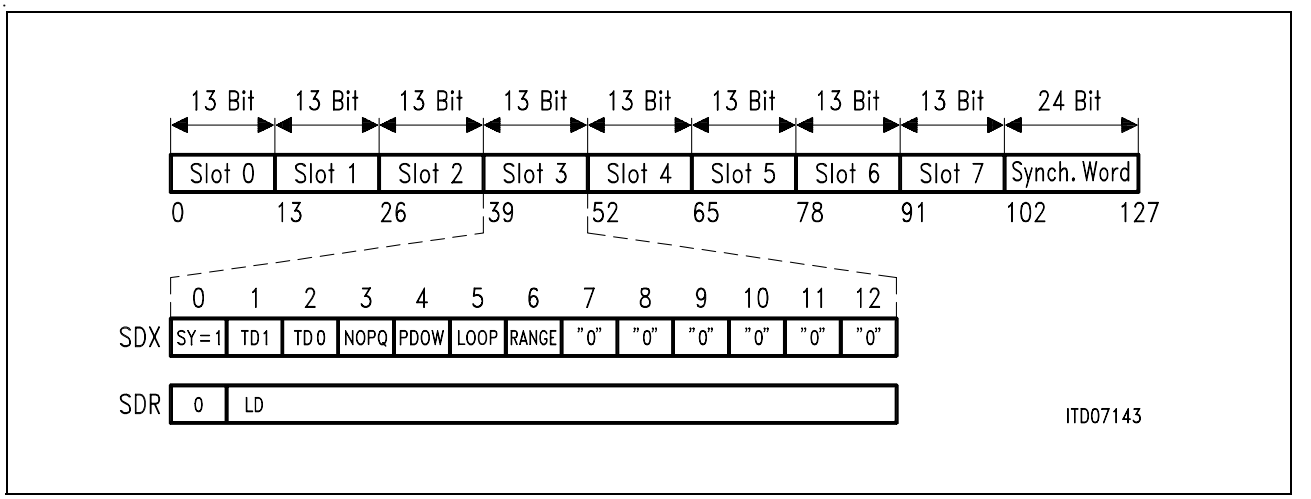


Figure 3-9 Frame Structure on SDX/SDR

The data on **SDX** is interpreted as follows:

$\overline{\text{NOP}}$: The no-operation-bit is set to ’0’ if none of the control bits (PDOW, RANGE and LOOP) shall be changed. The values of the control bits of the assigned line port is latched. The states of the control bits on SDX are ignored, they should be set to ’0’ to reduce any digital cross-talk to the analog signals.

The NOPQ bit is set to ’1’ if at least one of the control bits shall be changed. In this case all control bits are transmitted with their current values.

PDOW: If the PDOW bit is set to ’1’, the assigned line port is switched to power-down. Otherwise it is switched to power-up.

RANGE: RANGE = ’1’ activates the range function, otherwise the range function is deactivated. "Range function activated" refers to high input levels.

LOOP: LOOP = ’1’ activates the loop function, i.e. the loop is closed. Otherwise the line port is in normal operation.

SY: First bit of the time-slots with transmission data. For synchronization and bit allocation on SDX, SY is set to ’1’ on SDX and ’0’ on SDR.

"0": Reserved bit. Reserved bits are currently not defined and shall be set to ’0’. Some of these bits may be used for test purposes or can be assigned a function in later versions.

The 4B3T data is coded with the bits TD1, TD0:

Table 3-3 Coding of the 4B3T Data Pulse (AOUT/BOUT)

4B3T Data Pulse	TD1	TD0
0	0	0
+ 1	1	0
– 1	1	1

The data on **SDR** is interpreted as follows:

LD: The level detect information is communicated to the DFE-T V2.1 on SDR. If the signal amplitude reaches the wake-up level, the LD bit toggles with the signal frequency. If the input signal at the U-interface is below the wake-up level, the LD bit is tied to either low or high.

SY: First bit of the time-slots with transmission data. For synchronization and bit allocation on SDX, SY is set to ’1’ on SDX and ’0’ on SDR.

3.5 General Purpose I/Os

The DFE-T V2.1 features 6 general purpose I/O pins per line port. This way transparent control of test relays and power feeding circuits is possible via the IOM®-2 Monitor channel. Four of the six pins are outputs, two are inputs.

Setting Relay Driver Pins

Four relay driver output pins Dij (where i = 0, 1, 2, 3 denotes the line port no. and j = A, B, C, D specifies the pin) are available per line port. The logic state of the four relay driver outputs which are assigned to the same line port can be set by a single MON-8 command, called 'SETD'. The value is latched as long as no other SETD command with different relay driver settings is received.

The state of the relay driver pins is not affected by any software reset (C/I= RES). The state of all relay driver pins after hardware reset is „low".

Reading Status Pins

Each line port owns two status pins ST_{ij} (where i = 0,1, 2, 3 denotes the line port no. and j = 0, 1 specifies the pin) whose logical value is reported in the associated Monitor channel. Any signal change at one of the status pins ST1..4 causes automatically the issue of a two-byte MON-8 message 'AST' whose two least significant bits reflect the status of pin STij.

However, this automatic mechanism is only enabled again, if the previous status pin message has been transferred and acknowledged correctly according to the Monitor channel handshake protocol. It takes The DFE-Q V1.2 at least 8x IOM®-2 frames (1ms) to transmit the 2-byte MON-8 message. Thus, repeated changes within periods shorter than 8x IOM®-2 frames will overwrite the status pin register information. For this reason only the value of the last recent status change will be reported. Note that the MON-8 transfer time depends also on the reaction time (acknowledge by MR-bit) of the DFE-Q counterpart.

Besides this automatic report the DFE-T V2.1 will issue the status pin Monitor message 'AST' upon the MON-8 request 'RST' .

The ST_{ij} pins have to be tied to either VDD or GND, if they are not used.

3.6 U-Transceiver Functions

The 4B3T U-interface performs full duplex data transmission and reception at the U-reference point according to ETSI ETR 080 and FTZ 1TR 220. It applies the 4B3T block code together with adaptive echo cancelling and equalization. Transmission performance shall be such that it meets all ETSI and FTZ test loops with margin.

The U-interface is designed for data transmission on twisted pair wires in local telephone loops with ISDN basic rate access and a user bit rate of 144 kbit/s.

The following information is transmitted over the twisted pair:

- Bidirectional:
  - B1, B2, D data channels
  - 120 kHz Symbol clock, 160 kbit/s Transmission rate
  - 1 kHz Frame and 40 kHz block clock
  - Activation
- From LT to NT side:
  - Power feeding
  - Deactivation
  - Remote control of test loops
- From NT to LT side:
  - Indication of monitored code violations

On the U-interface transmission ranges 4.2 km on wires of 0.4 mm diameter and 8 km on 0.6 mm wires are achieved without additional signal regeneration in the loop. The transmission ranges can be doubled by inserting a repeater for signal regeneration.

3.6.1 4B3T Frame Structure

1 ms frames are transmitted across the U-interface, each consisting of:

- 108 symbols: 144 bit scrambled and coded B1 + B2 + D data
- 11 symbols: Barker code for both symbol and frame synchronization (not scrambled)
- 1 symbol: Ternary maintenance symbol (not scrambled)

The 108 user data symbols are split into four equally structured groups. Each group (27 ternary symbols, resp. 36 bits) contains the user data of two IOM®-2 frames in the same order (8B + 8B + 2D + 8B + 8B + 2D).

Different syncwords are used for each direction:

- Downstream from LT to NT+ + + – – – + – – + –
- Upstream from NT to LT– + – – + – – – + + +

On the NT side the transmitted Barker code begins 60 symbols after the received Barker code and vice versa.

After successful synchronization, resynchronization will occur if the syncword is not detected at the expected position in 64 consecutive frames.

The U-transceiver is synchronized, if it detects the syncword four times consecutively within a period of 1 ms.

Table 3-4 Frame Structure for Downstream Transmission LT to NT

1 D_1	2 D_1	3 D_1	4 D_1	5 D_1	6 D_1	7 D_1	8 D_1	9 D_1	10 D_1	11 D_1	12 D_1
13 $D_{1/2}$	14 $D_{1/2}$	15 $D_{1/2}$	16 D_2	17 D_2	18 D_2	19 D_2	20 D_2	21 D_2	22 D_2	23 D_2	24 D_2
25 D_2	26 D_2	27 D_2	28 D_3	29 D_3	30 D_3	31 D_3	32 D_3	33 D_3	34 D_3	35 D_3	36 D_3
37 D_3	38 D_3	39 D_3	40 $D_{3/4}$	41 $D_{3/4}$	42 $D_{3/4}$	43 D_4	44 D_4	45 D_4	46 D_4	47 D_4	48 D_4
49 D_4	50 D_4	51 D_4	52 D_4	53 D_4	54 D_4	55 D_5	56 D_5	57 D_5	58 D_5	59 D_5	60 D_5
61 D_5	62 D_5	63 D_5	64 D_5	65 D_5	66 D_5	67 $D_{5/6}$	68 $D_{5/6}$	69 $D_{5/6}$	70 D_6	71 D_6	72 D_6
73 D_6	74 D_6	75 D_6	76 D_6	77 D_6	78 D_6	79 D_6	80 D_6	81 D_6	82 D_7	83 D_7	84 D_7
85 **M**	86 D_7	87 D_7	88 D_7	89 D_7	90 D_7	91 D_7	92 D_7	93 D_7	94 D_7	95 $D_{7/8}$	96 $D_{7/8}$
97 $D_{7/8}$	98 D_8	99 D_8	100 D_8	101 D_8	102 D_8	103 D_8	104 D_8	105 D_8	106 D_8	107 D_8	108 D_8
109 D_8	110 **+**	111 **+**	112 **+**	113 **–**	114 **–**	115 **–**	116 **+**	117 **–**	118 **–**	119 **+**	120 **–**

D_1 ... D_8 Ternary 2B + D data of IOM-2 frames 1 ... 8
M Maintenance symbol
+, – Syncword

Table 3-5 Frame Structure for Upstream Transmission NT to LT

1 U_1	2 U_1	3 U_1	4 U_1	5 U_1	6 U_1	7 U_1	8 U_1	9 U_1	10 U_1	11 U_1	12 U_1
13 $U_{1/2}$	14 $U_{1/2}$	15 $U_{1/2}$	16 U_2	17 U_2	18 U_2	19 U_2	20 U_2	21 U_2	22 U_2	23 U_2	24 U_2
25 **M**	26 U_2	27 U_2	28 U_2	29 U_3	30 U_3	31 U_3	32 U_3	33 U_3	34 U_3	35 U_3	36 U_3
37 U_3	38 U_3	39 U_3	40 U_3	41 $U_{3/4}$	42 $U_{3/4}$	43 $U_{3/4}$	44 U_4	45 U_4	46 U_4	47 U_4	48 U_4
49 U_4	50 **–**	51 **+**	52 **–**	53 **–**	54 **+**	55 **–**	56 **–**	57 **–**	58 **+**	59 **+**	60 **+**
61 U_4	62 U_4	63 U_4	64 U_4	65 U_4	66 U_4	67 U_5	68 U_5	69 U_5	70 U_5	71 U_5	72 U_5
73 U_5	74 U_5	75 U_5	76 U_5	77 U_5	78 U_5	79 $U_{5/6}$	80 $U_{5/6}$	81 $U_{5/6}$	82 U_6	83 U_6	84 U_6
85 U_6	86 U_6	87 U_6	88 U_6	89 U_6	90 U_6	91 U_6	92 U_6	93 U_6	94 U_7	95 U_7	96 U_7
97 U_7	98 U_7	99 U_7	100 U_7	101 U_7	102 U_7	103 U_7	104 U_7	105 U_7	106 $U_{7/8}$	107 $U_{7/8}$	108 $U_{7/8}$
109 U_8	110 U_8	111 U_8	112 U_8	113 U_8	114 U_8	115 U_8	116 U_8	117 U_8	118 U_8	119 U_8	120 U_8

U_1 ... U_8 Ternary 2B + D data of IOM-2 frames 1... 8

M Maintenance symbol

+, - Syncword

3.6.2 Maintenance Channel

The 4B3T frame structure provides a 1kbit/s M(aintenance)-channel for the transfer of remote loopback commands, error indications and transparent messages.

Loopback Commands

The LT station uses the M-channel to request remote loopbacks. Loopback commands are coded with a series of ’0’ and ’+’ symbols.

- A continuous series of ’+0’ requests for loopback 1A activation in the repeater
- A continuous series of ’+’ requests for loopback 2 activation in the NT
- A continuous series of ’0’ requests for deactivation of any loopback

The NT station reacts as soon as the pattern has been detected in 8 consecutive symbols.

Error Indications

The NT U-transceiver reports line code violations via the M-channel to the exchange by setting one M-Bit to ’+’ polarity.

Transparent Messages

In either direction it is possible to transmit transparent messages via the M-channel. Transparent messages have priority and may override loopback commands and line code violations. So the user has to make sure that during an activation the NT is able to recognize a loopback command and that there is no conflict by simultaneous use of the transparent channel. ’-’ polarity represents a logic ’0’, ’+’ and ’0’ polarity represents a logic ’1’.

The interpretation of the M-Bit symbols depending on the direction (up-, downstream) is summarized below:

LT -> NT

Loopback Commands

the symbol sequence given below shall be received at least 8 times before the loopback command is approved valid

’+0..’= loopback 1A activation (in regenerator)
’++..’= loopback 2 activation (in NT)
’00..’= loopback deactivation

Transparent Channel Messages

’0’= logic ’1’ and no loop request
’+’= logic ’1’ and loop request
’-’= logic ’0’

NT -> LT

Transmission Error Detection and Report

’+’= code violation detected by the NT
’0’= idle code

Transparent Channel Message

’0’= logic ’1’ and no code violation
’+’= logic ’1’ and a detected code violation
’-’= logic ’0’

3.6.3 Exchanging Transparent Messages

The 4B3T U-transceiver provides via its register pair MRD and MWR direct access to the transparent channel. Access to the MRD and MWR registers is provided in turn via the Monitor channel of the IOM®-2 interface. Therefore two MON-0 messages were defined, MON-0 ’MRD’ and MON-0 ’MWR’.

Register MRD contains the last eight received M-bits, register MWR stores the M-bit data that is serialized and sent with the next eight outgoing U-frames (see **Figure 3-10**).

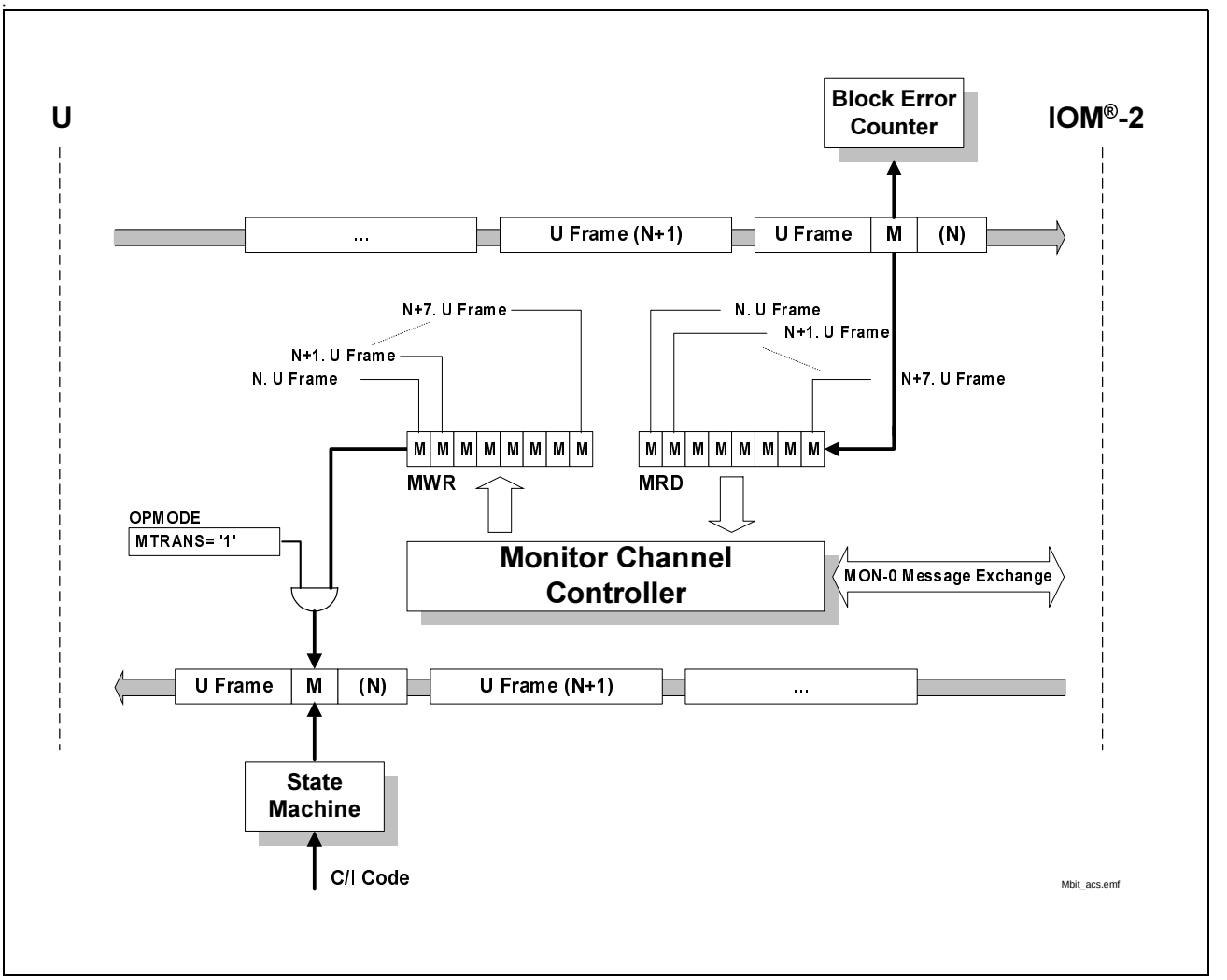


Figure 3-10 M-Bit Access via MRD, MWR Register Pair

Transparent channel mode is enabled by bit MTRANS set to ’1’ in the OPMODE register using the MON-12 protocol. As soon as OPMODE.MTRANS has been set to ’1’ the U-transceiver starts with the next incoming U-frame to shift M-bit data into the MRD register. Simultaneously - starting with the MSB value- the content of the MWR register is inserted at the M-bit positions of the next outgoing U-frame.

In case the MWR register was not preloaded before, zero or plus polarity is sent by default. The same applies if the MWR register is not reloaded in time again.

Once eight M-bits have been stacked by MRD (every 8ms) or the content of MWR has been shifted out, a MON-0 message is sent. That is every 8ms an autonomous MON-0 message will be issued which contains the last eight received M-bit data.

The periodic transmission of MON-0 messages allows to align MON-0 write commands in the transmit direction. See **Figure 3-11** for the access timing (MON TX= Monitor channel transmit register, MON RX= Monitor channel receive register).

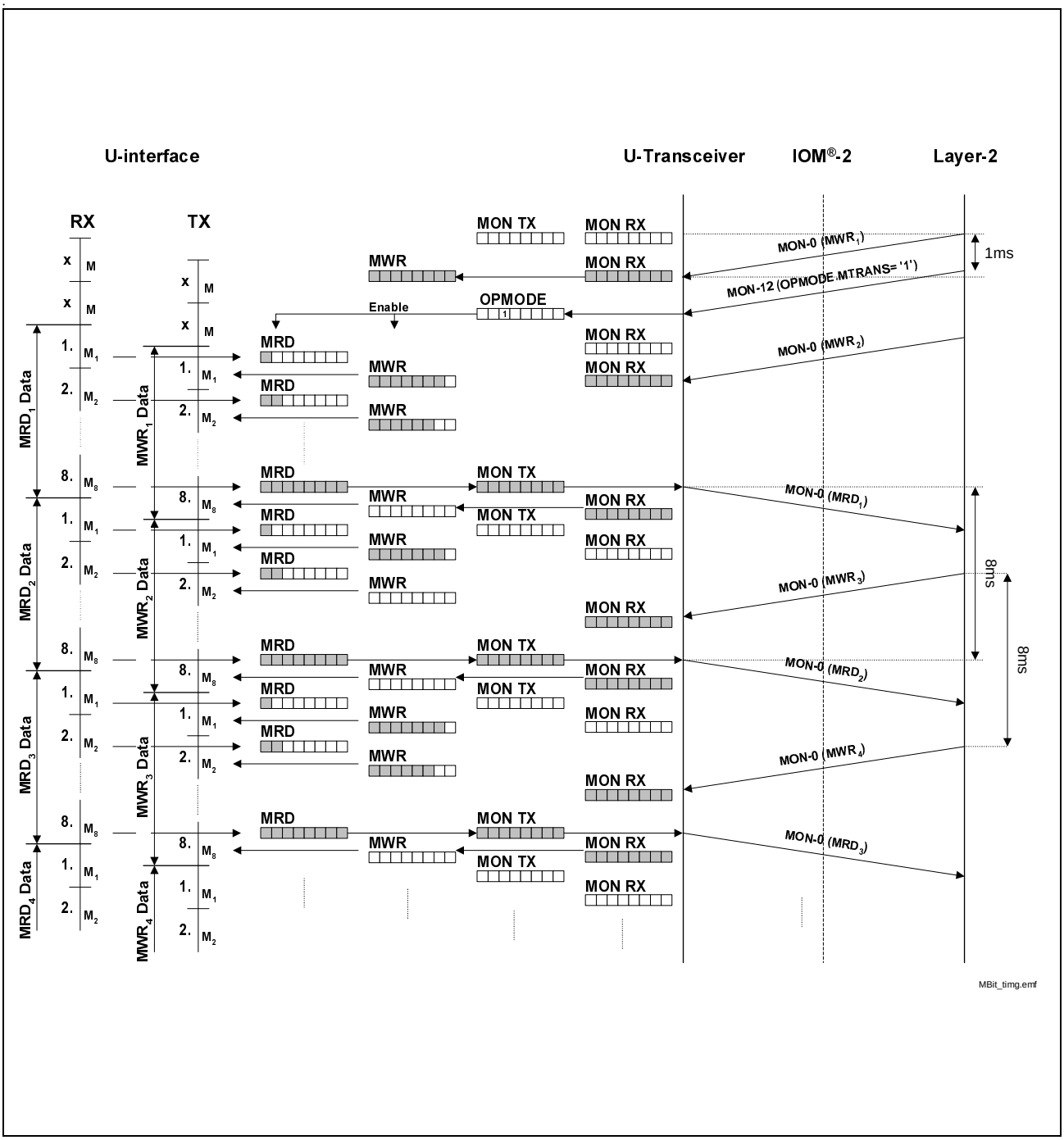


Figure 3-11 M-Bit Access Timing

3.6.4 Coding from Binary to Ternary Data

Each 4 bit block of binary data is encoded into 3 ternary symbols using the MMS 43 block code according to **Table 3-6**.

The number of the next column to be used, is given at the right hand side of each block. The left hand signal elements in the table (both ternary and binary) are transmitted first.

Table 3-6 MMS 43 Coding Table

				S1				S2				S3				S4			
t →				t →				t →				t →				t →			
0	0	0	1	0	–	+	1	0	–	+	2	0	–	+	3	0	–	+	4
0	1	1	1	–	0	+	1	–	0	+	2	–	0	+	3	–	0	+	4
0	1	0	0	–	+	0	1	–	+	0	2	–	+	0	3	–	+	0	4
0	0	1	0	+	–	0	1	+	–	0	2	+	–	0	3	+	–	0	4
1	0	1	1	+	0	–	1	+	0	–	2	+	0	–	3	+	0	–	4
1	1	1	0	0	+	–	1	0	+	–	2	0	+	–	3	0	+	–	4
1	0	0	1	+	–	+	2	+	–	+	3	+	–	+	4	–	–	–	1
0	0	1	1	0	0	+	2	0	0	+	3	0	0	+	4	–	–	0	2
1	1	0	1	0	+	0	2	0	+	0	3	0	+	0	4	–	0	–	2
1	0	0	0	+	0	0	2	+	0	0	3	+	0	0	4	0	–	–	2
0	1	1	0	–	+	+	2	–	+	+	3	–	–	+	2	–	–	+	3
1	0	1	0	+	+	–	2	+	+	–	3	+	–	–	2	+	–	–	3
1	1	1	1	+	+	0	3	0	0	–	1	0	0	–	2	0	0	–	3
0	0	0	0	+	0	+	3	0	–	0	1	0	–	0	2	0	–	0	3
0	1	0	1	0	+	+	3	–	0	0	1	–	0	0	2	–	0	0	3
1	1	0	0	+	+	+	4	–	+	–	1	–	+	–	2	–	+	–	3

3.6.5 Decoding from Ternary to Binary Data

Decoding is done in the reverse manner of coding. The received blocks of 3 ternary symbols are converted into blocks of 4 bits. The decoding algorithm is given in **Table 3-7**.

As in the encoding table the left hand symbol of each block (both binary and ternary) is the first bit and the right hand is the last. If a ternary block "0 0 0" is received, it is decoded to binary "0 0 0 0". This pattern usually occurs only during deactivation.

Table 3-7 4B3T Decoding Table

Ternary Block	Binary Block
0 0 0, + 0 +, 0 – 0	0 0 0 0
0 – +	0 0 0 1
+ – 0	0 0 1 0
0 0 +, – – 0	0 0 1 1
– + 0	0 1 0 0
0 + +, – 0 0	0 1 0 1
– + +, – – +	0 1 1 0
– 0 +	0 1 1 1
+ 0 0, 0 – –	1 0 0 0
+ – +, – – –	1 0 0 1
+ + –, + – –	1 0 1 0
+ 0 –	1 0 1 1
+ + +, – + –	1 1 0 0
0 + 0, – 0 –	1 1 0 1
0 + –	1 1 1 0
+ + 0, 0 0 –	1 1 1 1

3.6.6 Monitoring of Code Violations

The running digital sum monitor (RDSM) computes the running digital sum from the received ternary symbols by adding the polarity of the received user data (+ 1, 0, –1). At the end of each block, the running digital sum is supposed to reflect the number of the next column in **Table 3-6 "MMS 43 Coding Table" on page 3-24.**

A code violation has occurred if the running digital sum is less than one or more than four at the end of a ternary block, or if the ternary block 0 0 0 (three user symbols with zero polarity) is found in the received data.

If at the end of a ternary block no error was found, the running digital sum retains its current value. If the counter value is greater than 4, it is set to 3 at the beginning of the next ternary block, if its value is 0 or less, it is set to one. So after a code violation has been detected, the RDSM synchronizes itself within a period depending on the received data pattern. Note there are some transmission errors which do not cause a code violation.

3.6.7 Scrambler / Descrambler

Scrambler

The binary transmit data from the IOM®-2 interface is scrambled with a polynomial of 23 bits, before it is sent to the 4B3T coder. The scrambling algorithm ensures that no sequences of permanent binary 0s or 1s are transmitted.

– The scrambler polynomial in **LT mode** and **NT mode with the analog loop closed** is:

$$z^{-23} + z^{-5} + 1$$

– The scrambler polynomial in **NT mode with open analog loop** is:

$$z^{-23} + z^{-18} + 1$$

Descrambler

The received data (after decoding from ternary to binary) is multiplied with a polynomial of 23 bits in order to recover the original data before it is forwarded to the IOM®-2 interface. The descrambler itself is synchronized after 23 symbols.

– The descrambler polynomial in **LT mode with open analog loop** is:

$$z^{-23} + z^{-18} + 1$$

– The descrambler polynomial in **NT mode** or in **LT with the analog loop closed** is:

$$z^{-23} + z^{-5} + 1$$

3.6.8 4B3T Signal Elements

For control and monitoring purposes of the activation/deactivation progress the following signal elements are defined by TS 102 080 and FTZ 1 TR 220.

Encoding Scheme

The table below describes the characteristics of the defined 4B3T signal elements.

Table 3-8 Coding of the 4B3T Signal Elements

Upstream from NT to LT	Downstream from LT to NT
U1W: 16 times ternary + + + + + + + + – – – – – – – – – A tone of: Frequency: 7.5 kHz Period: 2.13 ms	U2W 16 times ternary + + + + + + + + – – – – – – – – – A tone of: Frequency: 7.5 kHz Period: 2.13 ms
U1A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code	U2A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code
U1: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)	U2: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)
U3: Binary continuous "1" before scrambling. Frame (Transmitting Barker code)	U4H: Binary continuous "1" before scrambling with duration of 1 ms. Frame (Transmitting Barker code)
U5: Binary data from the digital interface. Frame (Transmitting Barker code)	U4: Binary data from the digital interface. Frame (Transmitting Barker code)
U0: Ternary continuous "0" No frame, no signal level	U0: Ternary continuous "0" No frame, no signal level

Detection of U0, U1, U2, U3 and U4H

- The DFE-T V2.1 detects an **U1 or U3** signal element if the continuous binary data is found on the descrambler output after 8 subsequent U-frames. Thus these signal elements are detected valid after 8 to 9 ms.
- **U4H** is recognized if the NT finds 16 subsequent binary 1s in the data stream.
- **U0** is recognized if the LT finds one complete frame with continuous zero level. The significance of the U0 signal element is given in **Table 3-9**.

Significance of the 4B3T Signal Elements

Table 3-9 lists the defined 4B3T signal elements that are exchanged across the U-reference point in the course of an activation or deactivation process.

Table 3-9 4B3T Signal Elements

U0	No signal or deactivation signal that is used in both directions. Downstream, it requests the NT to deactivate. Upstream, the NT acknowledges by U0 that it is deactivated.
U1W	Awake or awake acknowledge signal **upstream** (7.5kHz) used in the awake procedure of the U-interface.
U2W	Awake or awake acknowledge signal **downstream** (7.5kHz) used in the awake procedure of the U-interface.
U2	The LT sends U2 to enable the own echo canceller to adapt the coefficients. By the Barker code the NT at the other end is enabled to synchronize. The detection of U2 is used by the NT as a criterion for synchronization. The M-channel on U may be used to transfer loop commands.
U1A	U1A is similar to U1 but without framing information. While the NT synchronizes on the received signal, it sends out U1A to enable its echo canceller to adapt its coefficients, but sends no Barker code to prevent the LT from synchronizing on the still asynchronous signal. Due to proceeding synchronization, the U-frame may jump from time to time. U1A can not be detected by the far-end LT.

Table 3-9 4B3T Signal Elements

U1	When synchronized, the NT sends the Barker code and the LT may synchronize itself. U1 indicates additionally that a terminal equipment has not yet activated. Upon receiving U1 the LT indicates the synchronized state by C/I 'UAI' to layer-2. Usually during activation, no U1 signal is detected in the LT because the TE is activated first and U1 changes to U3 before being detected. The M-channel on U may be used to transfer code error indications and 1 kbit/s transparent data.
U3	U3 indicates that the whole link to the TE is synchronous in both directions. On detecting U3 the LT requests the NT by U4H to establish a fully transparent connection. The M-channel on U may be used to transfer code error indications and 1 kbit/s transparent data.
U4H	U4H requires the NT to go to the 'Transparent' state. On detecting U4H the NT stops sending signal U3 and informs the S-transceiver or a layer-2 device via the IOM®-2 interface. The M-channel on U may be used to transfer loop commands and 1 kbit/s transparent data.
U4	U4 transports operational data on B and D channels. The M-channel on U may be used to transfer loop commands and 1 kbit/s transparent data.
U5	U4 transports operational data on B and D channels. The M-channel on U may be used to transfer code error indications and 1 kbit/s transparent data.
SP	The DFE-T V2.1 sends periodically single pulses spaced by 1 ms on the U-interface. The test mode can be used for pulse mask measurements.

3.6.9 Awake Protocol

For the awake process two signals are defined ’U1W’ and ’U2W’. Depending on the call direction (up-, downstream) U1W and U2W are interpreted as awake or acknowledge signals (see figures below).

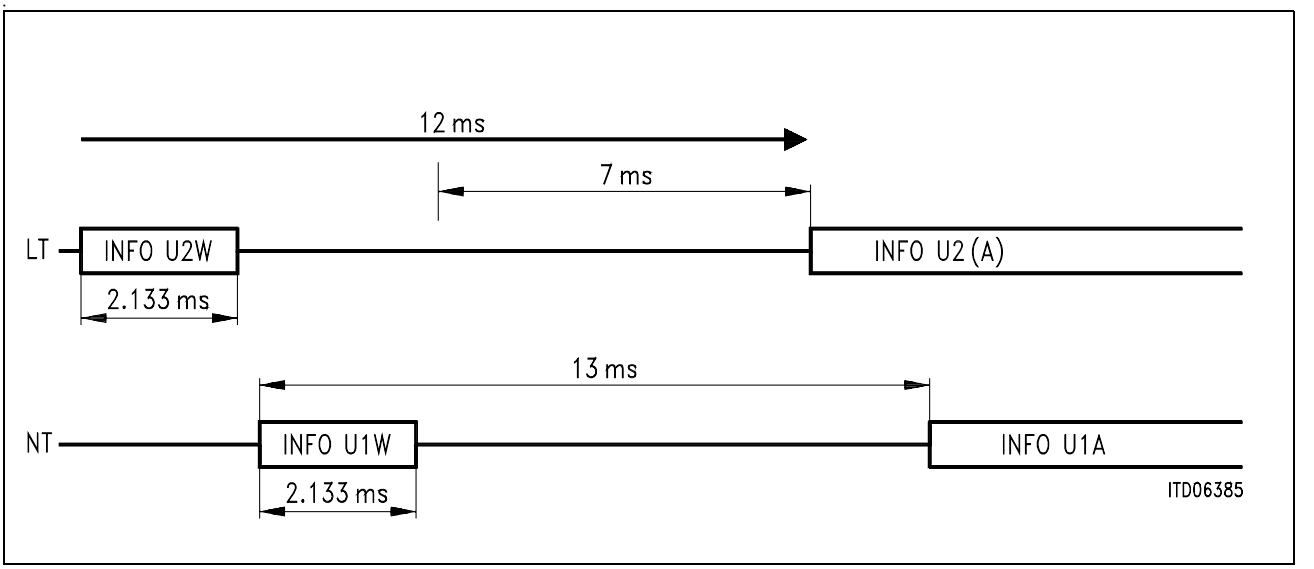


Figure 3-12 Awake Procedure initiated by the LT

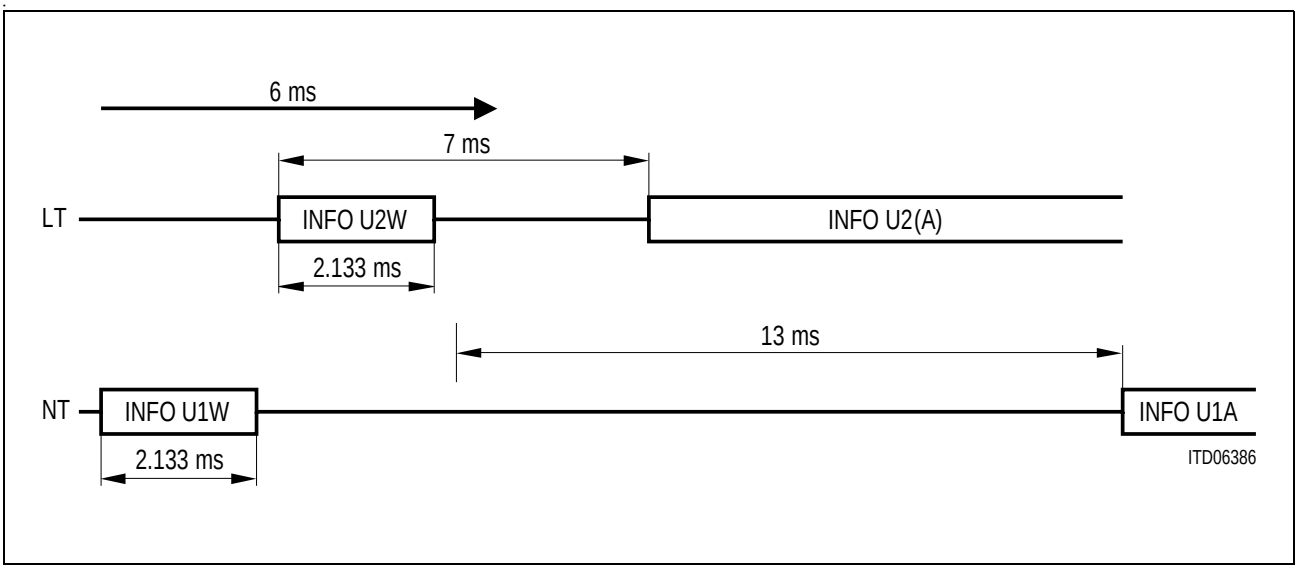


Figure 3-13 Awake Procedure initiated by the NT

Acting as Calling Station

After sending the awake signal, the awaking device waits for the acknowledge. After 12 ms the awake signal is repeated, if no acknowledge has been recognized. If an acknowledge signal has been recognized, the DFE-T V2.1 waits for its possible repetition (in case of previous coincidence of two awake signals).

If no repetition was detected, the DFE-T V2.1 starts transmitting U2 with a delay of 7 ms. If such a repetition is detected, the DFE-T V2.1 interprets it as an awake signal and behaves like a device awoken by the far-end.

Acknowledging a Wake-Up Call

If the DFE-T V2.1 detects an awake signal on U, an acknowledge signal is sent out. Afterwards the DFE-T V2.1 waits for a possible repetition of the awake signal (in case the acknowledge signal has not been recognized).

If no repetition is found, the awoken DFE-T V2.1 starts sending U2 after 7 ms from detecting the awake signal. If a repeated awake signal is found, the procedure in the awoken DFE-T V2.1 starts again.

3.6.10 C/I Codes

The Control/Indicate (C/I) channel is used to control the operational status of the DFE-T V2.1 and to issue corresponding indications. **Table 3-10** presents all defined C/I codes (former C/I code names of the DFE-T V1.2 are given in brackets).

A new command or indication will be recognized valid after it has been detected in two successive IOM® frames (double last-look criterion). Indications are strictly state orientated. Refer to the state diagram in the following section for commands and indications applicable in various states.

Table 3-10 Command / Indicate Codes

Code	LT-Mode	
	DIN	**DOUT**
0000	**DR**	–
0001	–	**DEAC**(DA)
0010	–	–
0011	– (LTD)	– (HI)
0100	–	**RSY** (RSYU)
0101	**SSP**	–
0110	**DT**(TEST)	–
0111	–	**UAI**(RDS)
1000	**AR**(ARN)	**AR**(ARU)
1001	**ARL**	–
1010	**ARL2**(AR2)	–
1011	**ARL1A**(AR4)	–
1100	–	**AI(**AIU)
1101	**RES**	–
1110	–	–
1111	**DC**(DID)	**DI**(DIU)

AI	Activation Indication	DI	Deactivation Indication.
AR	Activation Request	DR	Deactivation Request
ARL	Activation Request Local Loop	RES	Reset
ARL2	Activation Request Loop 2	RSY	Resynchronization Indication
ARL1A	Activation Request Loop 1A	SSP	Send-Single-Pulses

DC	Deactivation Confirmation	DT	Data Through Mode
DEAC	Deactivation Accepted	UAI	U Activation Indication

3.6.11 State Machine Notation

The following state diagram describes all the actions/reactions resulting from any command or detected signal and resulting from the various operating modes.

The states with its inputs and outputs are interpreted as shown below:

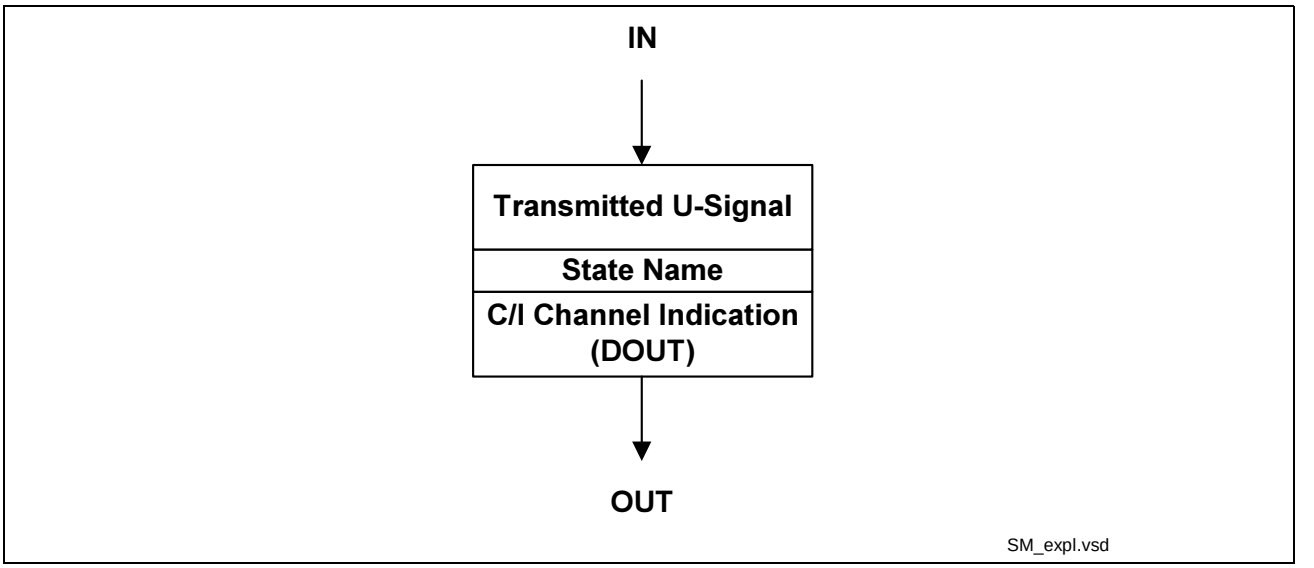


Figure 3-14 State Diagram Example

Each state has one or more transitions to other states. These transitions depend on certain conditions which are noted next to the transition lines. These conditions are the only possibility to leave a state. If more conditions have to be fulfilled together, they are put into parentheses with an AND operator (&). If more than one condition leads to the same transition, they are put into parentheses with an OR operator (|). The meaning of a condition may be inverted by the NOT operator (/). Only the described states and transitions exist.

At some transitions, an internal timer is started. The start of a timer is indicated by TxS ('x' is the timer number). Transitions that are caused if a timer has expired are labelled by TxE.

Some conditions lead to the same target state. To reduce the number of lines and the complexity of the figures, a state named "ANY STATE" acts on behalf of all state.

The state machine is designed to cope with all ISDN devices with IOM®-2 standard interfaces. Undefined situations are excluded. In any case the involved devices will enter defined conditions as soon as the line is deactivated.

3.6.12 LT Mode State Diagram

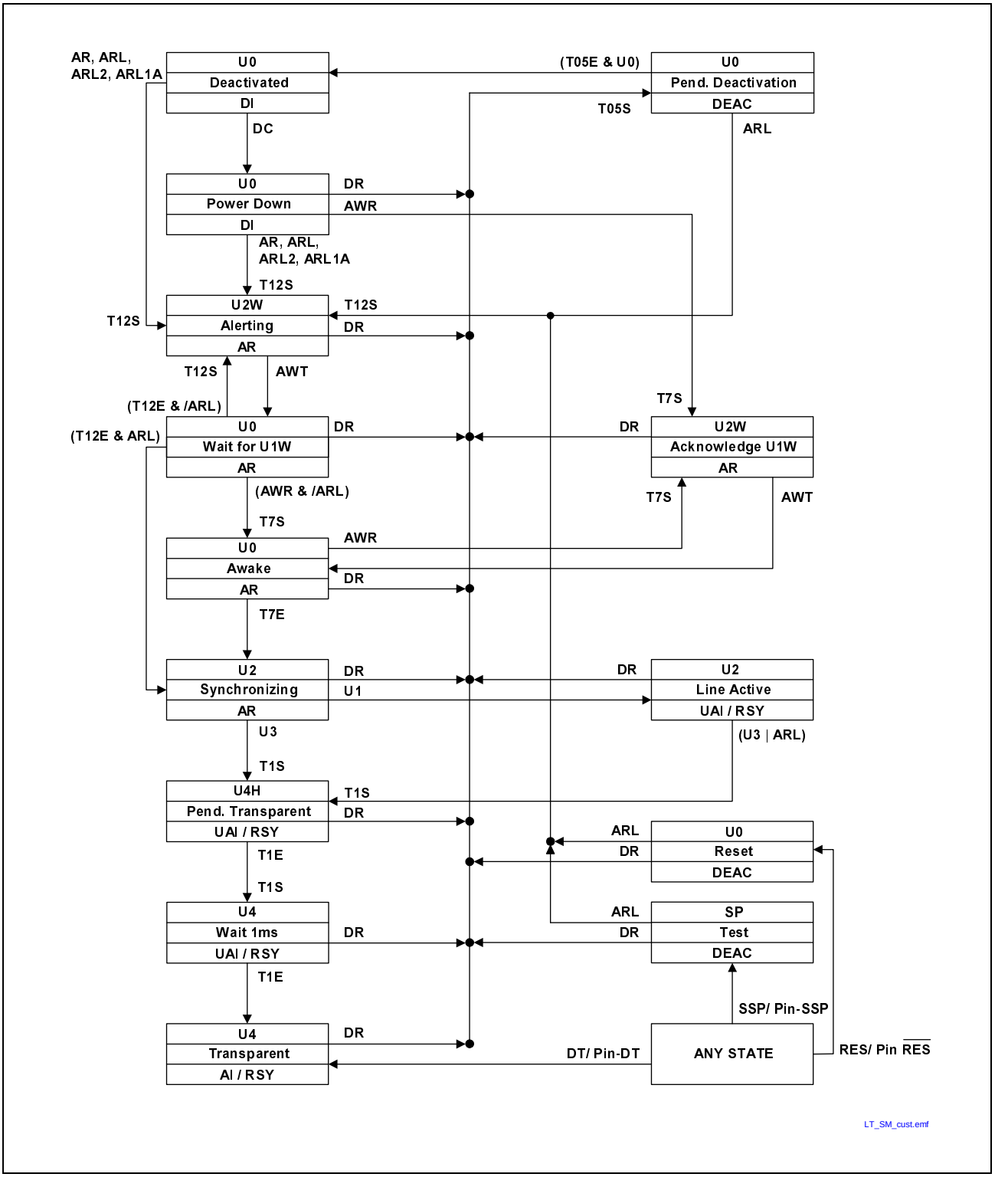


Figure 3-15 LT State Diagram

Table 3-11 Differences to LT-SM of DFE-T V1.2

No.	V1.2 State/ Signal	Change in V2.1	Comment
1.	’Maintenance’ State	split into two states - Reset State - Test State	simplifies SM implementation
2.	State ’Deactivating’	renamed to state ’Pending Deactivation’	for consistency reasons to 2B1Q and to TS 102 080
3.	State ’Deac. Acknowledge’	renamed to state ’Deactivated’	
4.	State ’Start Awak. U’	renamed to state ’Alerting’	
5.	State ’Awake Signal Sent’	renamed to state ’Wait for U1W’	
6.	State ’Sending Awake Ack.’	renamed to state ’Acknowledge U1W’	
7.	State ’Ack. Sent/ Received’	renamed to state ’Awake’	
8.	State ’U Synch. no TE?’	renamed to state ’Line Active’	
9.	State ’Link to TE Synch.’	renamed to state ’Pend. Transparent’	
10.	State ’Data Transmission’	renamed to state ’Transparent’	
11.	Any State	transition condition PFOFF& /ARL or LTD doesn’t exist any more	no support of the IEC type power controller interface

Table 3-11 Differences to LT-SM of DFE-T V1.2

No.	V1.2 State/ Signal	Change in V2.1	Comment
12.	Renamed C/I codes	**old -> new** ARN -> AR AR2 -> ARL2 AR4 -> ARL1A AIU -> AI DA -> DEAC DID -> DC DIU -> DI RSYU -> RSY TEST -> DT	consistency to 2B1Q coding
13.	C/I codes LTD and HI	C/I codes 'LTD' and 'HI' were omitted and are no more available	function corresponds to that of C/I 'RES'
14.	Timer variables introduced	**Name Duration** T05 0.5ms T1 1.0ms T7 7.0ms T12 12.0ms	

3.6.12.1 State Machine Inputs

C/I-Commands

AR Activation Request
The U-transceiver is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal U2W.

ARL Activation Request Local Loop-back
The U-Transceiver gets reset and is requested to operate an analog loop-back. An activation procedure is started. Any other C/I-channel input, low on pin $\overline{\text{RES}}$ or high on pin SSP causes the analog loop to be opened and the M-symbol to be set to zero.

ARL2 Activation Request Loop 2 in the NT
The U-Transceiver is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal U2W. The loop 2 request is signalled via the Maintenance channel by a continuous plus polarity in the M-symbol.

ARL1A Activation Request Loop 1A in the Repeater
The U-Transceiver is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal U2W. The loop 1A request is signalled via the Maintenance channel by a series of alternating plus and zero polarity in the M-symbol.

DR Deactivation Request
The U-transceiver is requested to start a deactivation procedure.

DC Deactivation Confirmation
DC informs the U-transceiver that the upstream unit is also deactivated. The U-transceiver is now ready to receive awake signals. Upon DC the U-transceiver enters power-down mode.

RES Reset
Unconditional command which resets any stored settings of the U-transceiver; no line signal will be sent out.

SSP Send Single Pulses
Unconditional command which requests the transmission of single pulses with a period of 1ms.

DT Data Through Test Mode
Unconditional command which causes the U-transceiver to transit to the transparent state and to issue U4 independent of the wake-up protocol. A far-end transceiver needs not to be connected. In case a far-end transceiver is present it is assumed to be in the same condition.

Pins

RES — Pin-Reset
Corresponds to C/I code 'RES' besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line. C/I-message DEAC will be issued.

SSP — Pin-Send Single Pulses
Corresponds to C/I code 'SSP' besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line. C/I-message DEAC will be issued.

U-Interface Events

U0 — U0 detected
U0 is recognized after one complete frame with continuous zero level.

U1 — U1 detected
The U-transceiver detects U1 if continuous binary data is found on the descrambler output after 8 subsequent U-frames. U1 is detected after 8 to 9 ms.

U3 — U3 detected
See description of U1.

AWR — Awake signal (U1W) detected

AWT — Awake signal (U2W) has been sent out

TxE — Timer ended, the started timer has expired

Timers

The start of timers is indicated by TxS, the expiry by TxE. The following table shows which timers are used.

Table 3-12 Timers

Timer	Duration (ms)	Function	State
T05	0.5	C/I code recognition	Deactivated
T1	1.0	Defines duration of U4H	Pend. Transparent
T7	7.0	Supervises U1W repetition	Awake
T12	12.0	Supervises U2W repetition	Alerting, Wait for U1W

3.6.12.2 State Machine Outputs

Below the signals and indications are summarized that are issued on IOM®-2 (C/I-indications) and on the U-interface (predefined U-signals).

C/I Indications

AR Activation Request
The AR code indicates that an awake signal has been received and that a start-up procedure is in progress.

UAI U-Activation Indication
The U-transceiver has detected U1 or U3 indicating that the transmission line between the two U-interface stations is now synchronized. At this point of time the block error counter (RDS) is enabled.

AI Activation Indication
As soon as U3 has been detected the U-transceiver issues ’AI’ and transits to the ’Transparent’ state. ’AI’ indicates that the whole transmission line is now synchronized from the LT to the TE.

DEAC Deactivation Accepted
DEAC is issued in response to a DR-code and informs the upstream unit that the U-transceiver is deactivating the transmission line downstream.

DI Deactivation Indication
DI informs the upstream unit that the U-transmission line is deactivated. On receiving ’DC’ the U-transceiver enters the power-down state. The transmitter is disabled, but awake signals may be detected.

RSY Resynchronization Indication
RSY informs that the U-transceiver is not synchronous. RSY is issued if the U-transceiver was in the fully activated state and has lost synchronization afterwards (transmission of U4 will not be interrupted).

Signals on U-Interface

The signals U0, U2W, U2A, U2, U4H, U4 are transmitted on the U-interface in the course of an activation/ deactivation. They are defined in detail in Table 3-9 "4B3T Signal Elements" on page 3-28.

SP Single Pulses
The U-transceiver sends periodically single pulses spaced by 1 ms e.g. for pulse mask measurements.

3.6.12.3 State Description

In this section each LT state is described with its inputs, outputs and its function.

The C/I-channel output and the transmitted signal elements on U are already specified by the state diagram. Below they are only referred to, if within a state there are more than one of them specified. In this case, the C/I-channel output and the transmitted signal element depend on the given inputs.

Acknowledge U1W

On the receipt of the awake signal U1W the U-transceiver responds with the transmission of U2W. The user data (2B + D) on pin DOUT is clamped to high.

Alerting

On the receipt of AR, ARL, ARL2 or ARL1A in the C/I-channel the U-transceiver has powered up and is sending the awake signal U2W. The user data (2B + D) on pin DOUT is clamped to high.

Awake

If awaking the U-transceiver has received the acknowledge signal. If being awoken the U-transceiver has sent the acknowledge. In both cases the U-transceiver waits for a possible repetition or time-out. The user data (2B + D) on pin DOUT is clamped to high to prevent that wrong data is transmit in the D-channel during activation.

Deactivated

In the Deactivated state no signal is transmitted on the U-interface. The U-transceiver is ready to enter the power-down state. The user data (B + B + D) on pin DOUT is clamped to high.

Line Active

After the recognition of U1 the U-interface is synchronized in both directions. That is 1.152 subsequent bits have been transferred and received without any bit error. The U-transceiver transits to the ’Transparent’ state as soon as a TE signals its presence by signal U3. In case of an analog loop the U-transceiver leaves this state again immediately.

If in 64 subsequent U-frames the Barker-code can not be detected at the expected position, the U-transceiver issues RSY on the C/I-channel until it has resynchronized. The criteria for resynchronization is that the Barker-code has been detected at the same position in 4 subsequent frames.

The block error counter (RDS) and the coefficient adaptation are enabled until deactivation is performed.

Pending Deactivation

The U-transceiver deactivates the U-interface sending U0 and waits in turn for signal U0 to enter the 'Deactivated' state. Timer T05 ensures that the C/I code DEAC is recognized by the exchange.

The user data (2B + D) on pin DOUT is clamped to high.

Pending Transparent

The whole transmission system from the LT to the TE is now synchronized in both directions of transmission. Signal U4H is sent until the expiry of timer T1. U4H requires the NT to establish a transparent link to the TE.

If synchronization has been lost the U-transceiver issues RSY on the C/I-channel until it has resynchronized again.

Power Down

On the receipt of 'DC' in the C/I channel the U-transceiver enters the power-down state. In power-down mode all power consuming parts of the device which are not required for the wake-up detection are switched off.
The U-transceiver waits either for an activation request (AR, ARL, ARL2, ARL1A) from the exchange or for a wake-up signal U1W from the NT.

Reset

The Reset state is entered by the unconditional command RES or pin-$\overline{\text{RES}}$. All stored coefficients are erased. The U-transceiver leaves the Reset state if pin-$\overline{\text{RES}}$ is set inactive ('1') and the C/I code DR or ARL is applied. The U-transceiver does not react on the receipt of a wake-up signal.

The user data (B + B + D) on pin DOUT is clamped to high.

Synchronizing

After successful awake procedure, the U-transceiver looks for the signals U1 or U3 to synchronize its receiver.

The user data (2B + D) on pin DOUT is clamped to high.

Test

Test mode is entered by the unconditional command SSP or pin-SSP. The Test state is left if pin SSP is set inactive ('0') and the C/I code DR or ARL is applied. Single pulses spaced by 1ms are sent on the U-line.

The U-transceiver does not react on the receipt of a wake-up signal. The user data (B + B + D) on pin DOUT is clamped to high.

Transparent

The transmission line is fully activated. User data can be exchanged by U4/U5. Transparent state may also be entered in the case of a loop-back 2. The exchange is informed by C/I code AI that the transparent state has been reached.

The block error counter (RDS) and the adaptation of the receiver coefficients are enabled even if RSY is sent. If synchronization has been lost the U-transceiver issues RSY on the C/I-channel until it has resynchronized again.

Wait 1ms

If the transparent state has been reached, the U-Transceiver in the exchange waits 1ms to ensure that the whole link is already transparent before it is indicated by C/I code AI to the exchange.

If synchronization has been lost the U-transceiver issues RSY on the C/I-channel until it has resynchronized again. The user data (B + B + D) on pin DOUT is clamped to high.

Wait for U1W

The U-transceiver is awaking the U-interface and waits for the acknowledge by the NT or for the time-out (12ms) after sending the awake signal.

The user data (2B + D) on pin DOUT is clamped to high.

3.7 Clock Generation

The 15.36MHz master clock is generated by a crystal oscillator connected to the AFE V2.1. In case FSC differs from the 8kHz PTT reference clock an integrated crystal based phase locked loop (PLL) is provided in the AFE to retain system synchronization. The AFE-PLL accepts either a 8kHz or 2048kHz system clock. The AFE supplies the DFE-T V2.1 with the synchronized 15.36MHz clock at pin CL15. Below the clock characteristics are summarized:

Master clock nominal frequency:	15.36 MHz
Max. Difference of phase deviations of Master clock and FSC:	± 25 µs
Max. low freq. phase wander within 1 period:	± 0.85 ps
Jitter (peak-to-peak):	see **Figure 3-16**

Jitter on the 15.36 MHz master clock is passed to the U-interface without change. Hence, **Figure 3-16** reflects the maximum tolerable input jitter as given by FTZ 1 TR 220.

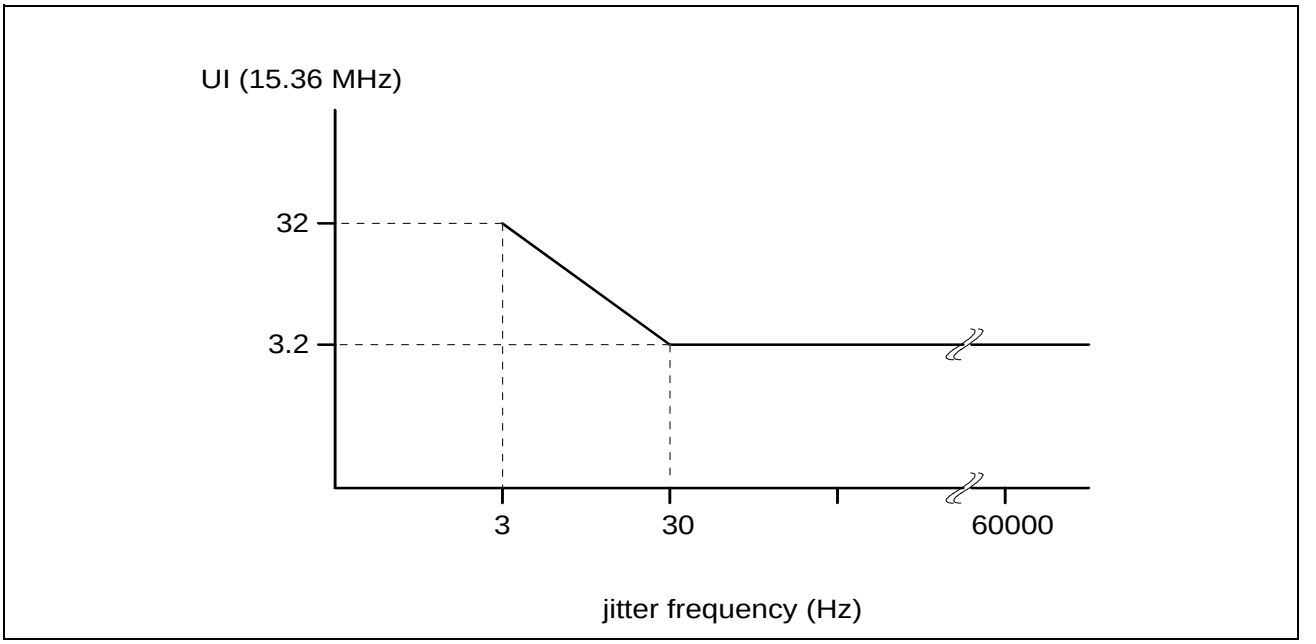


Figure 3-16 Maximum Tolerable Input Jitter of the 15.36MHz Clock

4 Operational Description

The scope of this section is to describe how the DFE-T V2.1 works and behaves in the system environment. Activation/ deactivation control procedures are exemplary given for SW programmers reference.

4.1 Reset

There are two different ways to apply a reset,

- either as a hardware reset by setting pin $\overline{\text{RES}}$ to low
- or as a software reset by applying 'C/I= RES'

Hardware Reset

A hardware reset affects all design components and takes effect immediately (asynchronous reset style). No clock signal other than the master clock shall be required for reset execution.

Software Reset

A software reset triggered by 'C/I= RES' has only effect on the addressed line port. The remaining line ports, the system interface, the relay driver/ status pins and any global functions are not affected. A clock signal must be provided for the C/I code processing.

C/I 'RES' resets the receiver and the activation/deactivation state machine. Transmission on U is stopped. It is an unconditional command and is therefore applicable in any state.

4.2 Power Down

Each building block of the DFE-T V2.1 is optimized with respect to power consumption and support a power down mode. See chapter 7.6.2 page 7-8 for the specified max. power consumption.

The DFE-T V2.1 goes in power down mode

- if the U-transceiver is in state 'Power Down'

There are two events that awake the DFE-T V2.1 again from power down mode,

- when a wake up tone (U1W) has been detected on U
- when any of the C/I codes AR, ARL, ARL2 or ARL1A is applied at DIN

Regarding the **DFE-T V2.1** power down mode means that

- the DSP clock is turned off
- all other digital circuits (excluding the IOM®-2 interface) go in power down mode

- no timing signals are delivered (CLS0, ... , CLS3)

Regarding a connected **AFE** power down mode means that

- no signal is sent on the U-interface
- only functions that are necessary to detect the wake up conditions are kept active
- transmit path, receive path and auxiliary functions of the analog line port are switched to a low power consuming mode when the power down function is activated. This implies the following:
- the ADC, the relevant output is tied to GND.
- the DAC and the output buffer; the outputs AOUTx/ BOUTx are tied to GND.
- the internal DC voltage reference is switched off.
- the range and the loop functions are deactivated.

4.3 Layer 1 Activation/ Deactivation Procedures

This chapter illustrates the interactions during activation and deactivation between the LT and NT station. An activation can be initiated by either of the two stations involved. A deactivation procedure can be initiated only by the exchange. The status of a transmission line is classified by one of the seven activation/deactivation states (also referred to by number in the activation/ deactivation procedures on the following sides):

1. **Activation** States:
   - 1.1 **Line awake**
     Each individual line is being awoken, but is not yet synchronized, data transmission is not yet possible
   - 1.2 **Synchronization downstream**
     Synchronization is always done downstream first, the whole line has to synchronize on the exchange
   - 1.3 **Synchronization upstream**
     Because the delay differs from line to line, bit synchronization is necessary in the LT
   - 1.4 **Synchronized**
     All layer-1 units of the link are told by the exchange that synchronization has been finished

2. **Transparent** State:
   In the activated state, the user data is transmitted from exchange to TE and vice versa.

3. **Deactivation** States:
   Deactivation is done in two steps on each individual line separately.
   - 3.1 Deactivation request downstream
   - 3.2 Deactivation acknowledge upstream

   The transmission link is totally deactivated thereafter.

The exchange of control information is partially state oriented on the U-interface. Some signal elements are given as long as no other information has to be transferred, other signal elements have distinct durations.

4.3.1 Complete Activation Initiated by Exchange

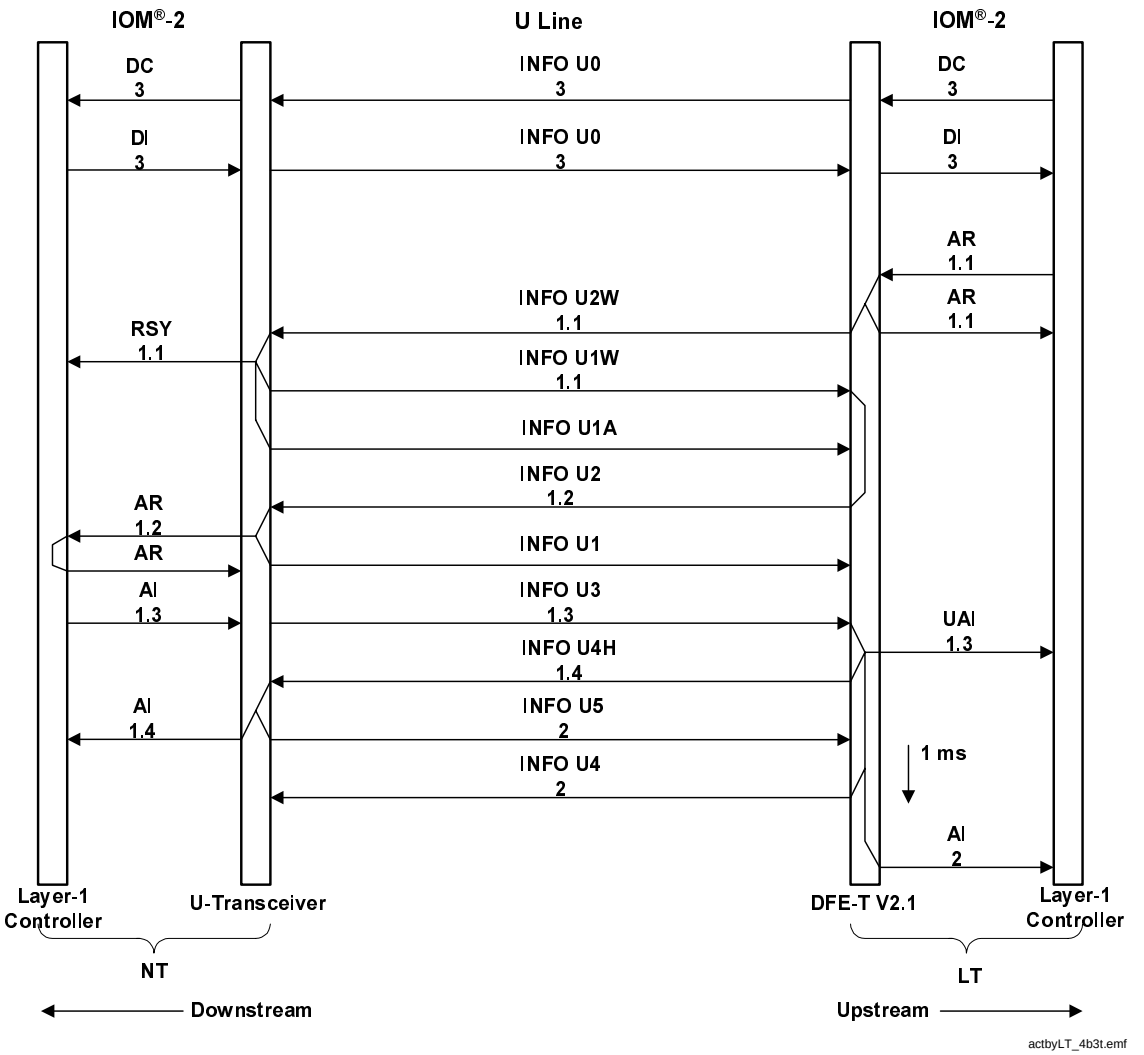


Figure 4-1 Activation Initiated by Exchange

4.3.2 Complete Activation Initiated by TE

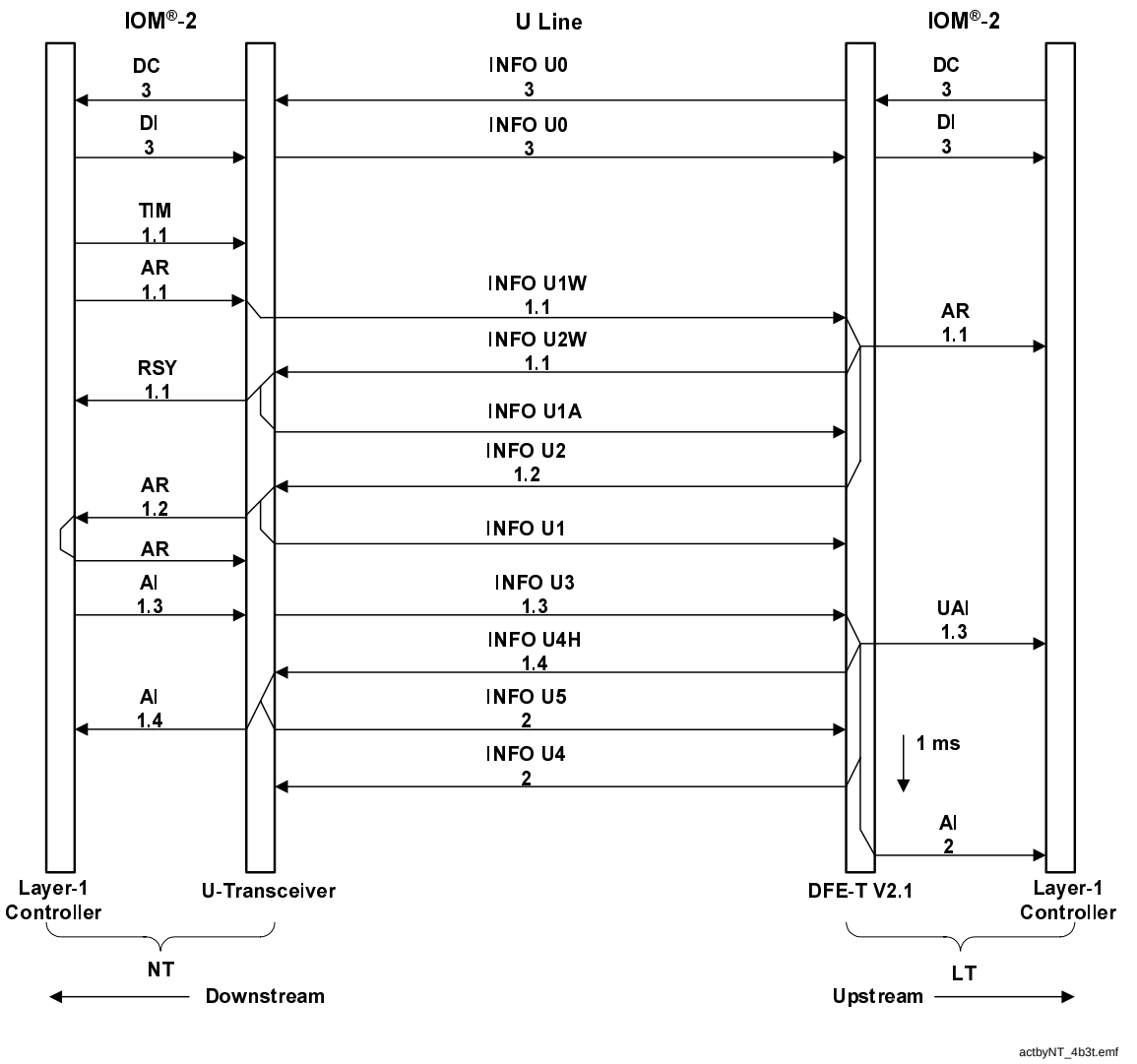


Figure 4-2 Activation Initiated by TE

4.3.3 Complete Activation Initiated by Exchange with Repeater

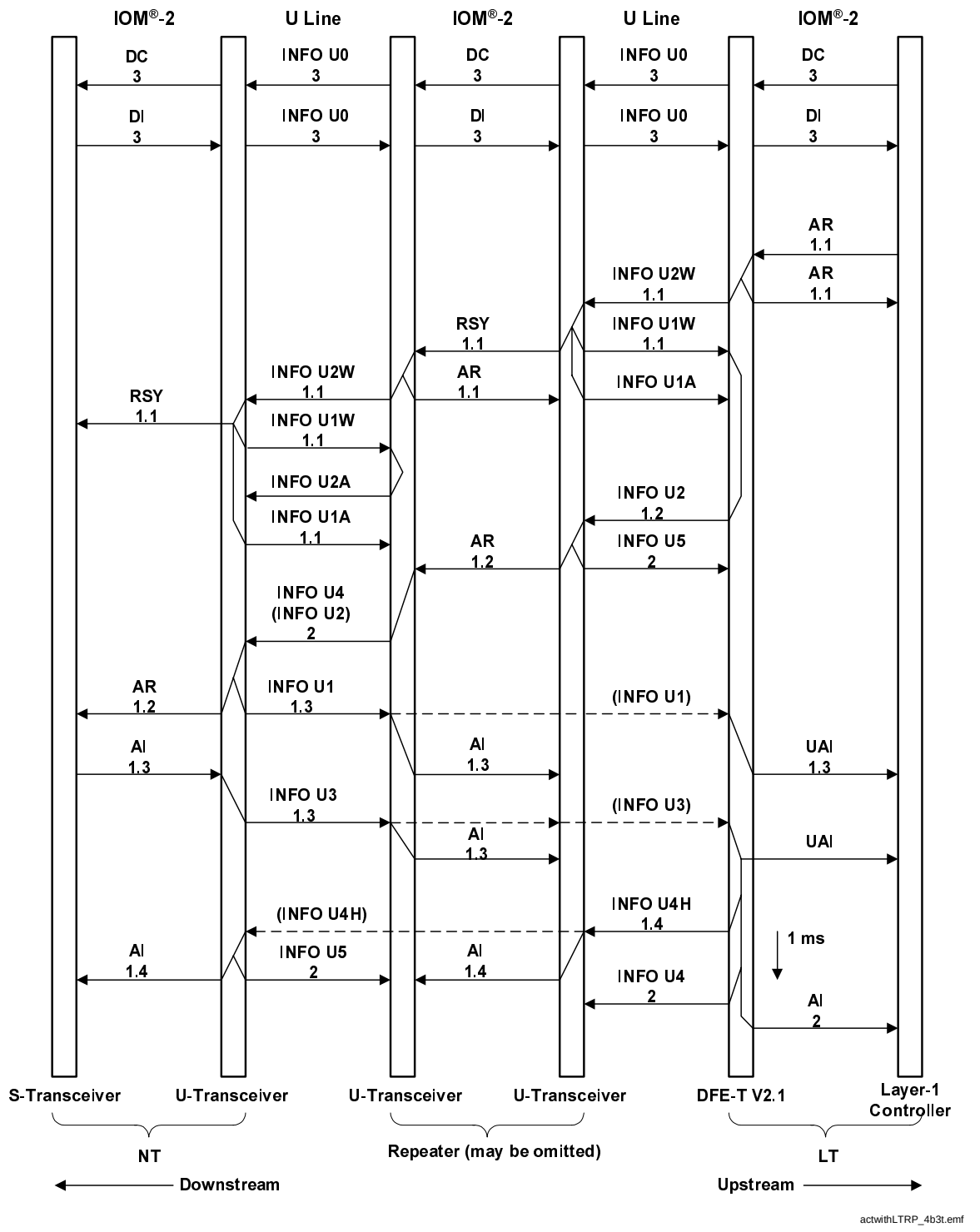


Figure 4-3 Activation with Repeater Initiated by LT

4.3.4 Complete Activation Initiated by Terminal with Repeater

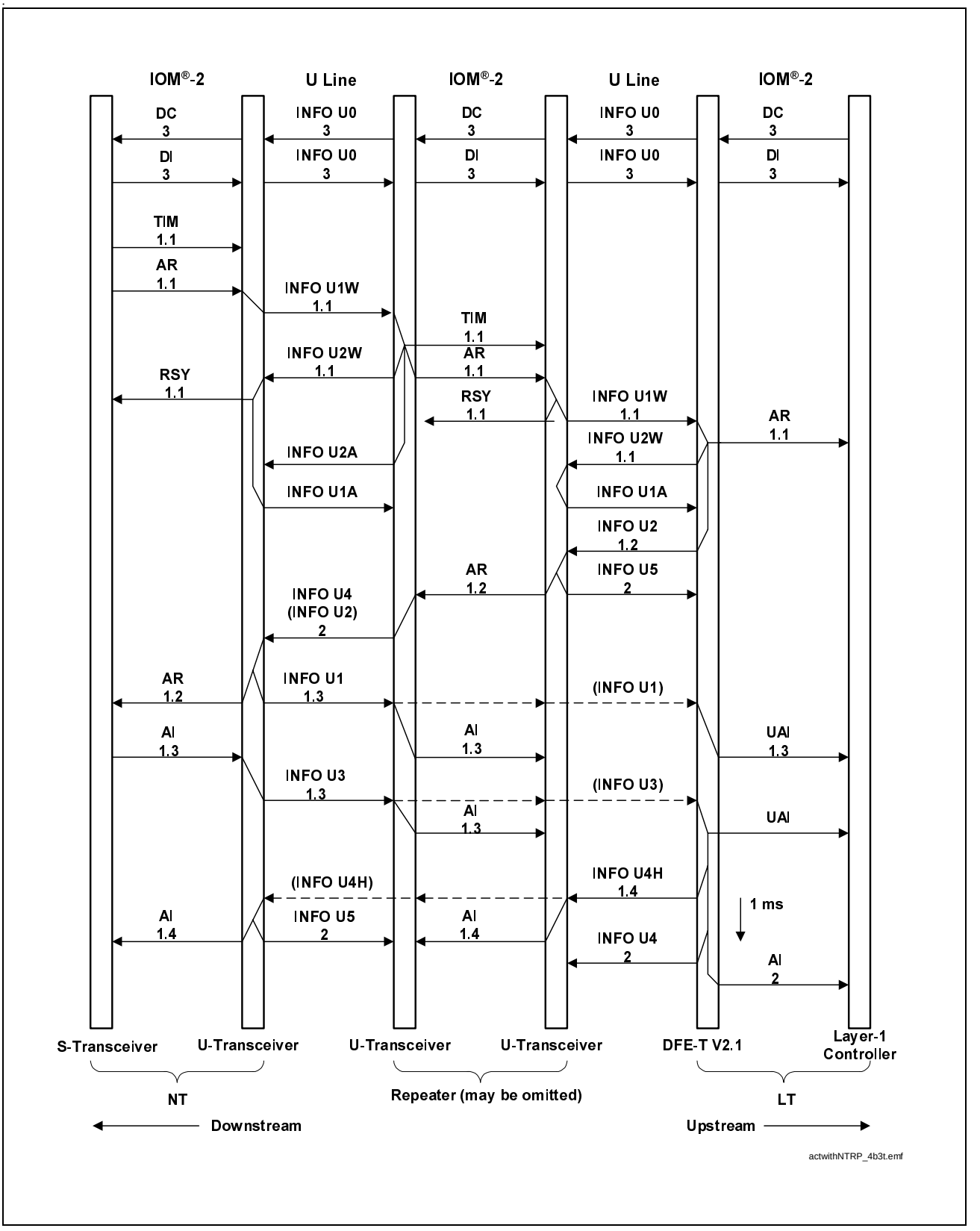


Figure 4-4 Activation with Repeater Initiated by TE

4.3.5 Deactivation

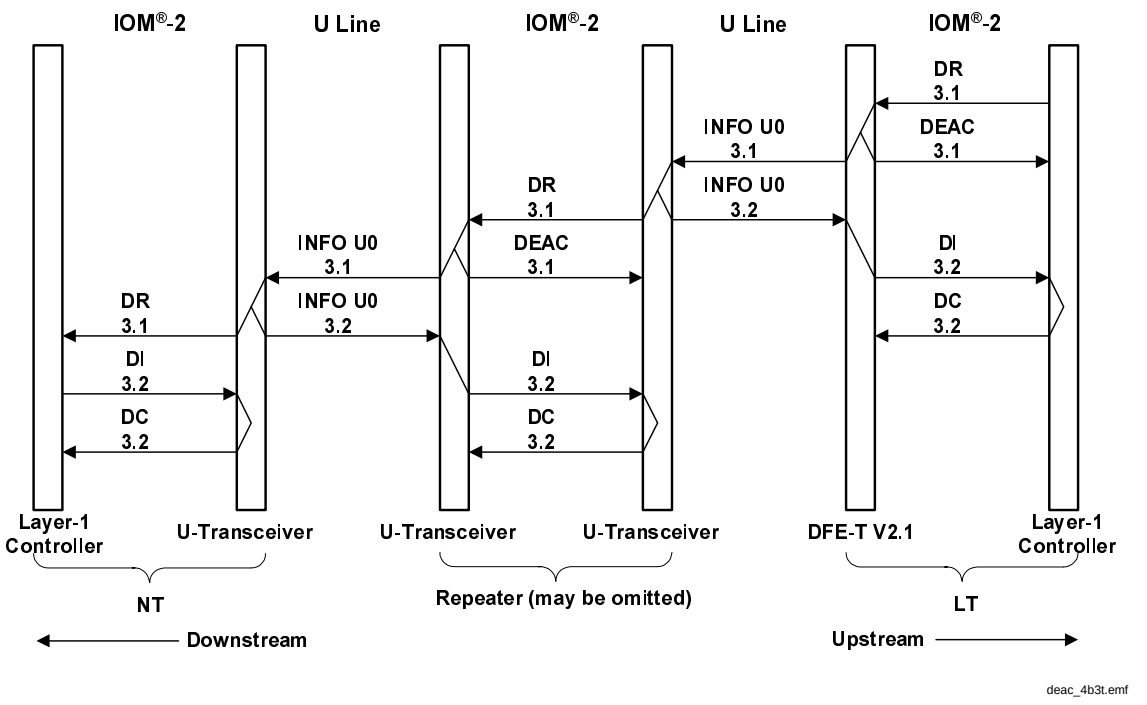


Figure 4-5 Deactivation (Always Initiated by the Exchange)

4.3.6 Activation of Loop#1

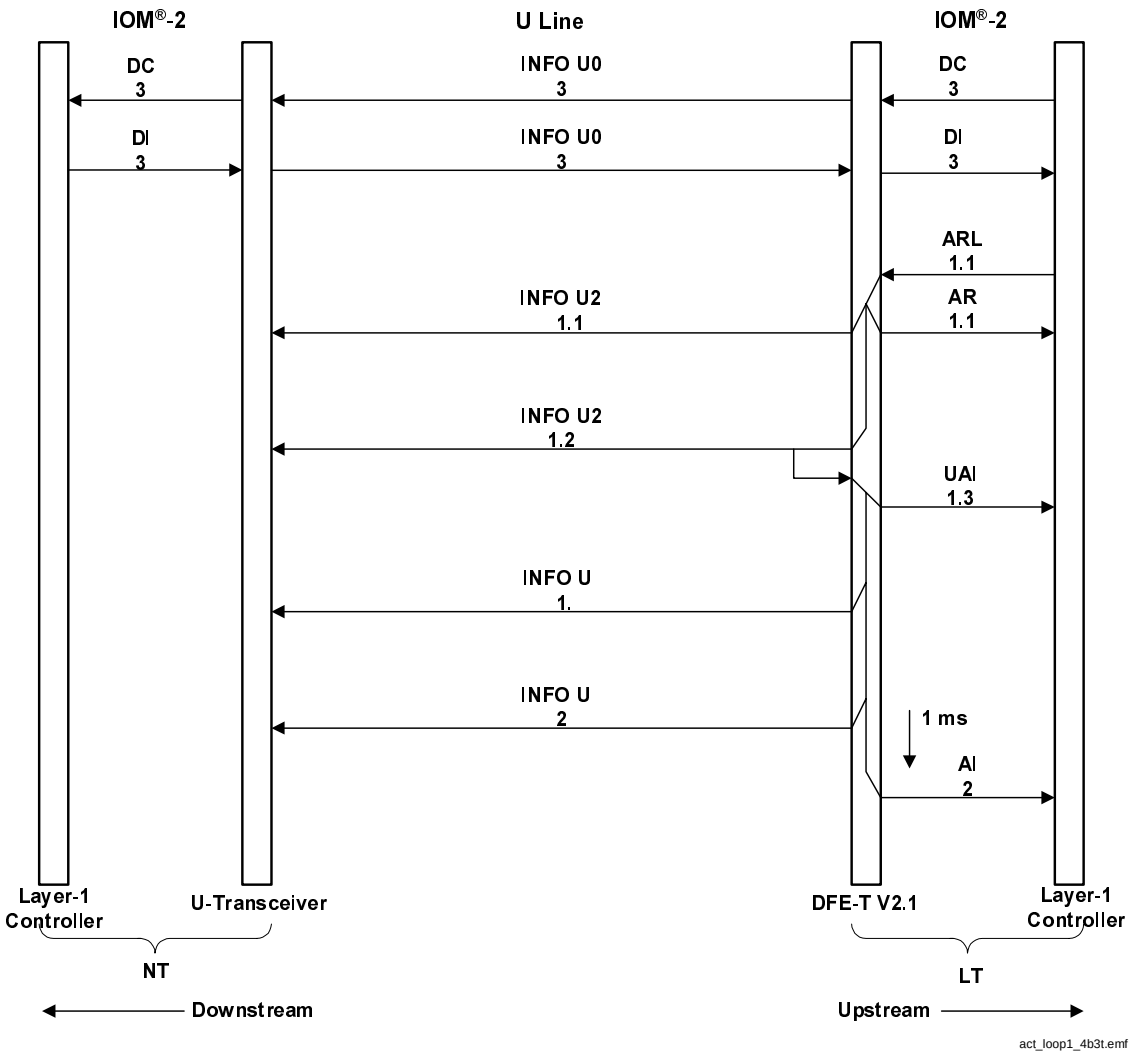


Figure 4-6 Activation of Loop#1

4.3.7 Activation of Loop#1A

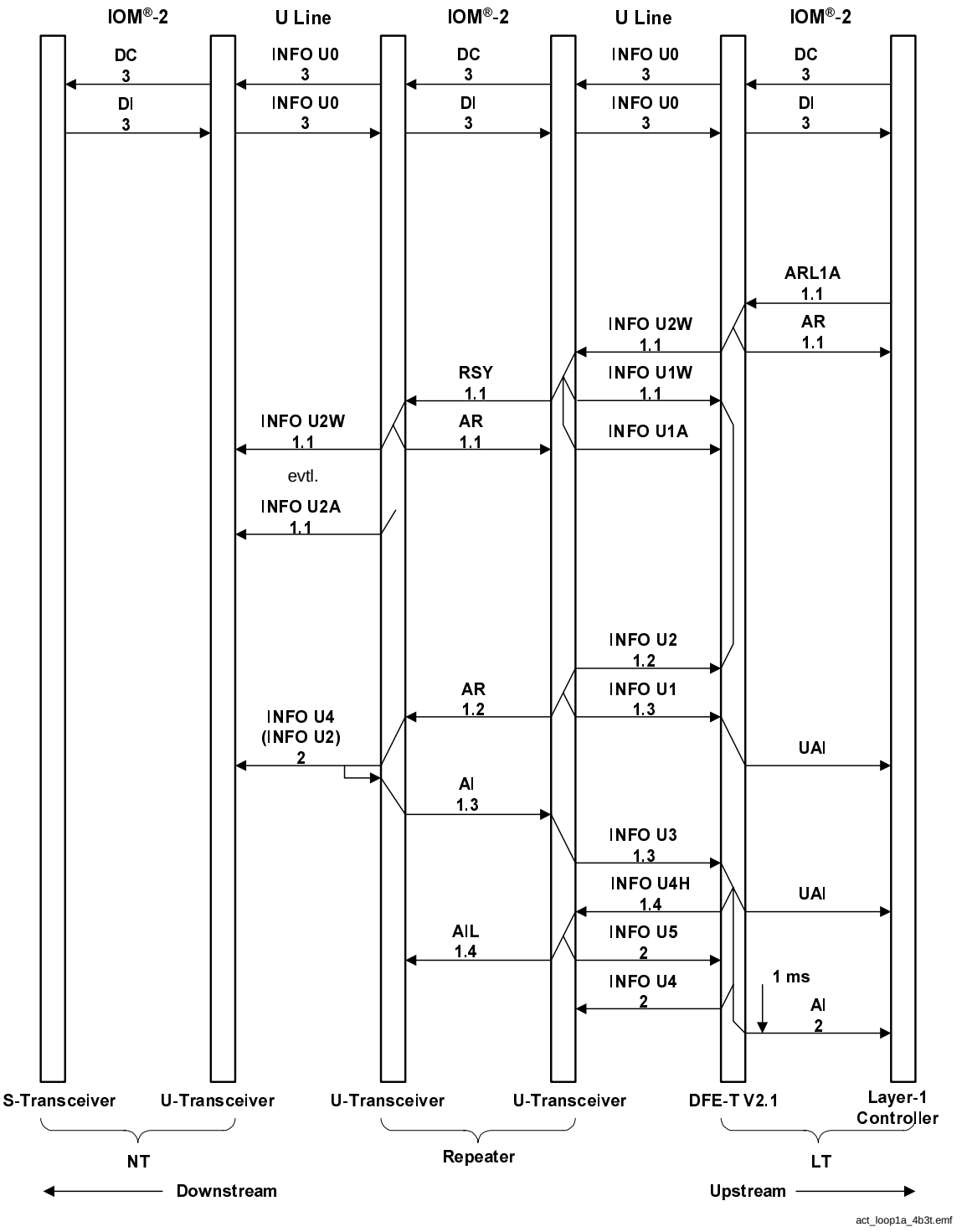


Figure 4-7 Activation of Loop#1A (Repeater)

4.3.8 Activation of Loop#2

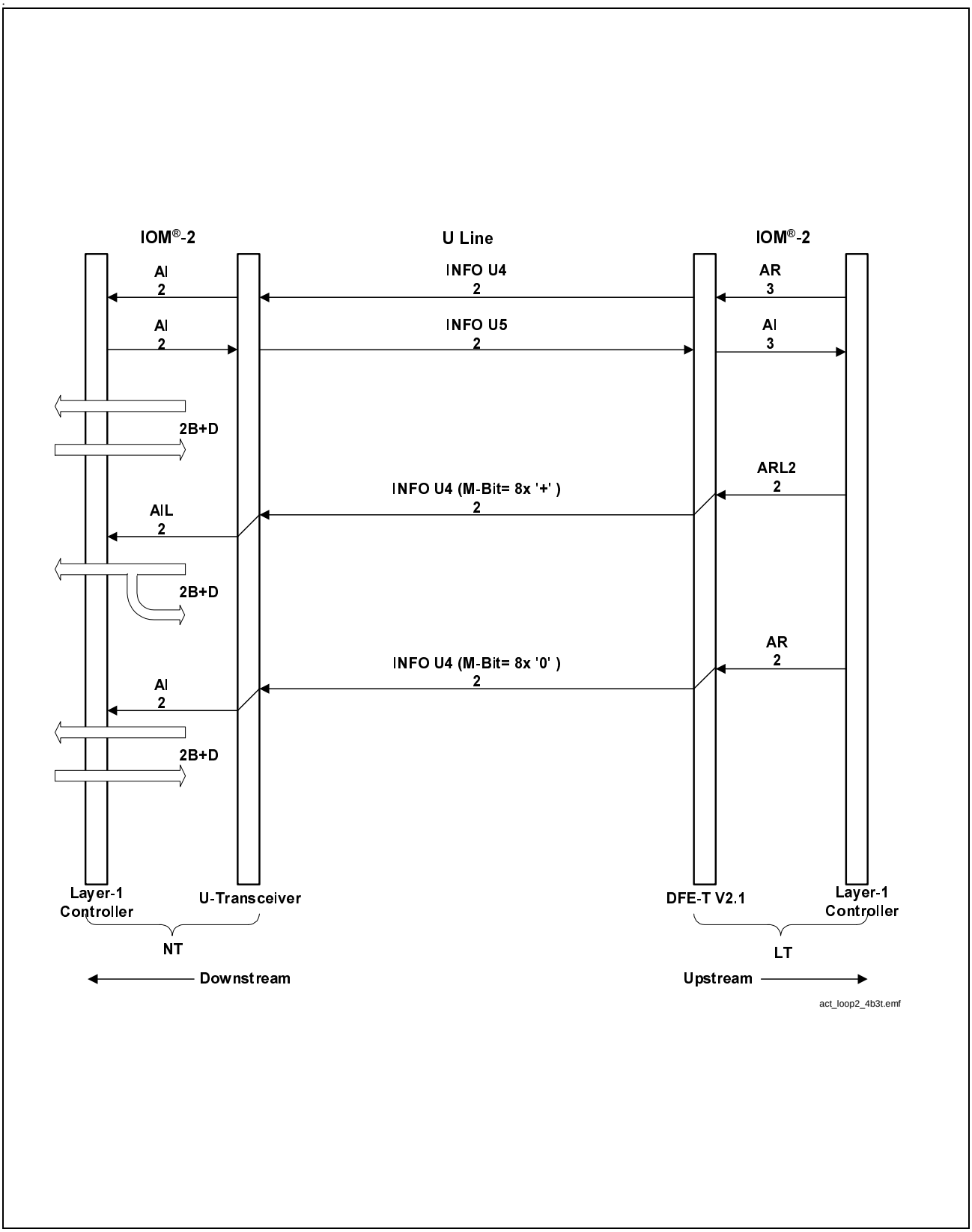


Figure 4-8 Activation of Loop#2

4.4 Maintenance and Test Functions

This chapter summarizes all features provided by the U-transceiver to support maintenance functions and system measurements. They are classified into three main groups:

– maintenance functions to close and open test loopbacks
– features facilitating the recognition of transmission errors
– test modes required for system measurements

The next four sections describe how these maintenance functions are used in applications.

4.4.1 Test Loopbacks

Four different loopbacks are defined for maintenance purposes and in order to facilitate the location of defect systems. The position of each loopback is illustrated in **Figure 4-9**. Remote control by the exchange is featured. When a test loop is closed all channels (B1 + B2 + D) are looped back and data from the other end of the line is ignored. There are no separate loops for single channels.

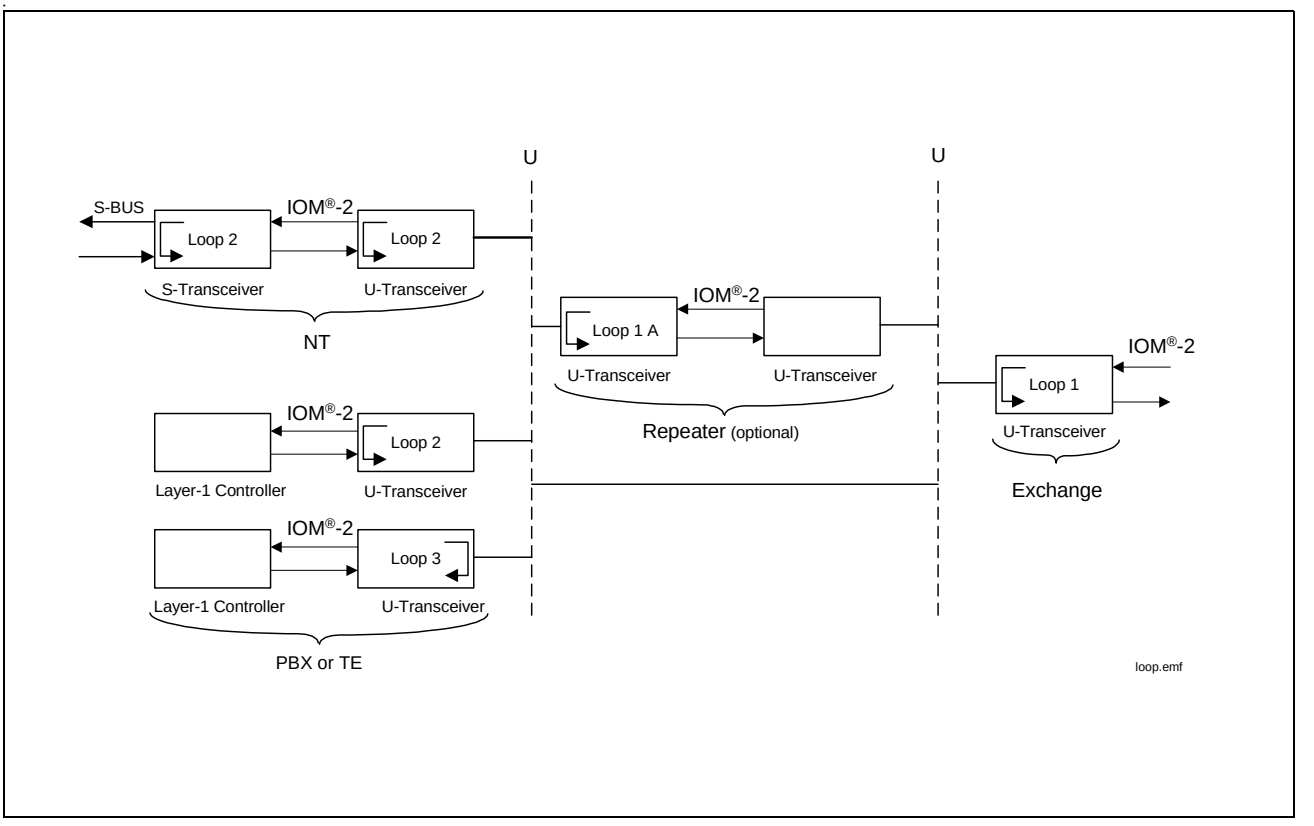


Figure 4-9 Test Loopbacks

All test loops are transparent loops. The line signal is still transmitted although the analog loop is closed. Nevertheless the NT receives this signal and synchronizes on it. The NT can not distinguish between line signals sent from the LT during loop 1 or loop 1A and

signals sent during normal operation. Loopback no.1 is closed by the DFE-T V2.1 itself, whereas loopback no 1A and no.2 are remote controlled by C/I code ’ARL1A’ and ’ARL2’ and are closed in the NT. Loopback no.3 is not supported since the DFE-T V2.1 operates only in LT mode.

4.4.1.1 Analog Loopback (No.1)

The analog loop no.1 is closed in the DFE-T V2.1 as close to the U-interface as possible. The signal from the line driver is fed back directly to the input. It is like a short-circuit between the pins AOUT and AIN as well as between BOUT and BIN. The input signal from the hybrid is ignored in this mode. The analog loop mode is controlled via the IOM®-2 C/I-channel code ’ARL’.

To request a LT-repeater to close the analog loop no.1A, C/I code ’ARL1A’ must be applied to the DFE-T V2.1. It will send in turn alternating plus and zero polarity within 8 subsequent frames in the M-channel (+ 0 + 0 + 0 + 0 ...).

4.4.1.2 Loopback No.2

Loopback no. 2 is controlled by the exchange. It is transparent which means that all bits that are looped back are also passed on to the S-bus. The DFE-T V2.1 features the remote control of loop no.2 via its C/I channel. C/I code ’ARL2’ requests the NT to close the loop, ’AR’ or ’DR’ requests the NT to open the loop again.

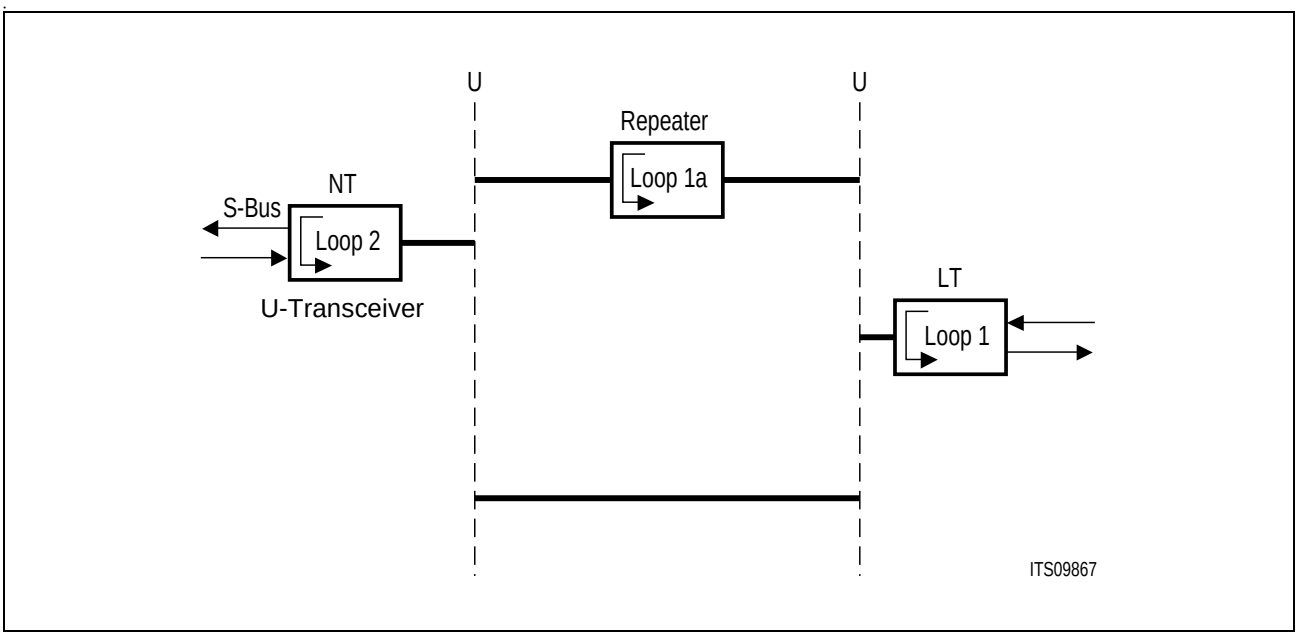


Figure 4-10 Loopback No.2

The DFE-T V2.1 translates the received C/I codes into the following pattern sequence in the M-channel of the U-interface:

- continuous ’+’ polarity
  The NT closes loopback no.2 after 8 consecutive pulses with plus polarity has been received in the M-channel (+ + + + + + + + ...).
- continuous ’0’ polarity
  The NT closes loopback no.2 after 8 consecutive zeros has been received in the M-channel (0 0 0 0 0 0 0 0 ...) or on a deactivation request.

During normal transmission without loops, the M-symbol is set to zero or minus.

The loopback comprises both B-channels and the D-channel. It is closed in the NT as close to the S-transceiver as possible. The NT U-transceiver passes the request on to the S-transceiver by issuing C/I-code AIL in the “Transparent” state or C/I-code ARL in all other states.

4.4.1.3 Available Loopbacks by Register Map

Besides the remote loopback stimulation and the local analog loopback (C/I= ARL) the DFE-T V2.1 features digital local loopbacks via its internal register set. The loopbacks that are additionally available with the internal LOOP register are shown in **Figure 4-11**. They can be activated regardless of the current activation status using the MON-12 protocol and have direct effect.

By the LOOP register it can be configured whether the digital looback is closed only for the B1 and/or B2 or for all ISDN-BA channels and whether the loopback is closed towards the IOM®-2 interface or towards the U-Interface.

By default the loopbacks are set to transparent mode. In transparent mode the data is both passed on and looped back. In non-transparent mode the data is not forwarded but substituted by 1s (idle code).

Besides the loopbacks in the system interface a further digital loopback, the Framer/ Deframer loopback is featured. It allows to test all digital functions of the 4B3T U-transceiver besides the signal processing blocks.

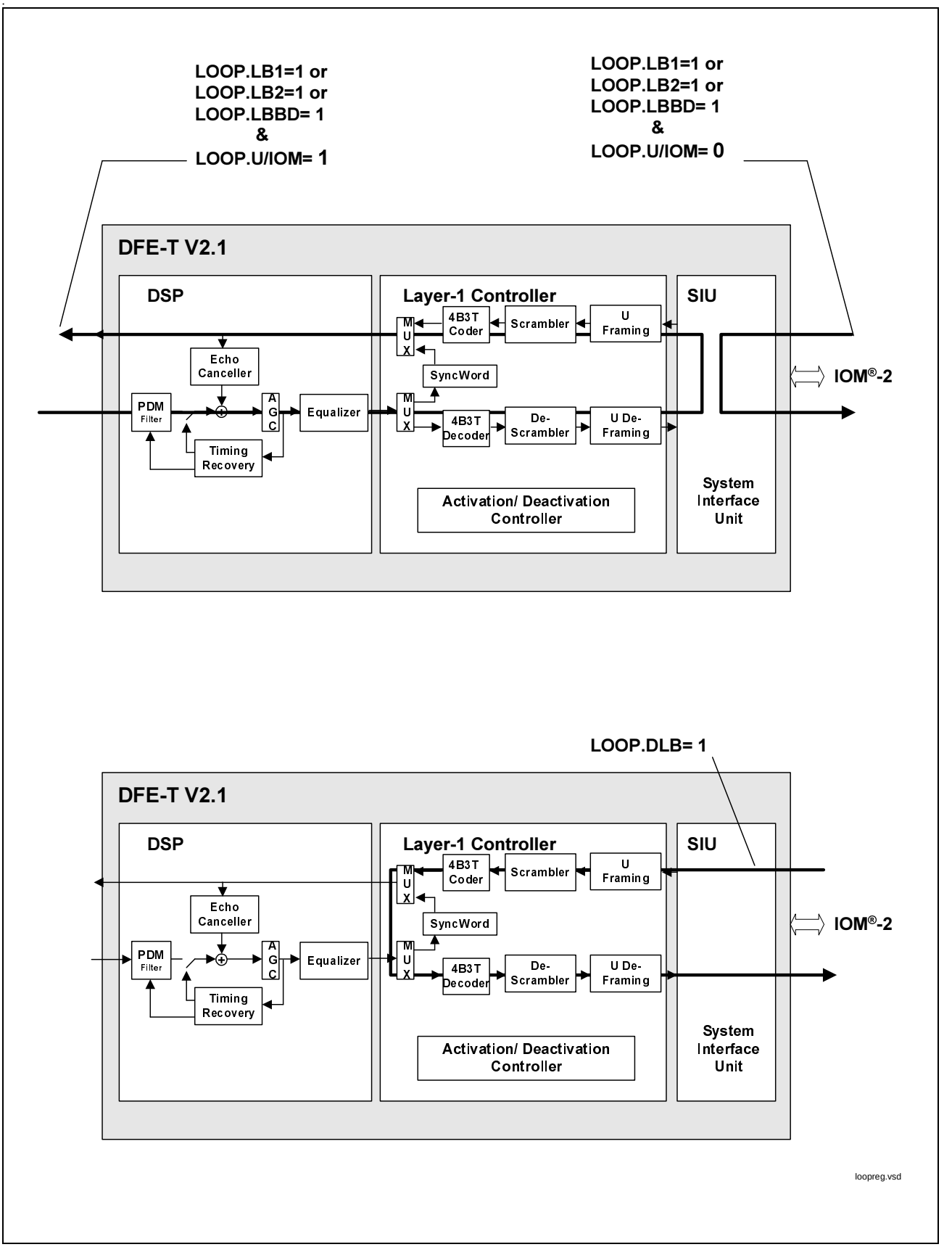


Figure 4-11 Loopbacks Featured by Register LOOP

4.4.2 Block Error Counter

The DFE-T V2.1 provides a block error counter per channel. This feature allows a comfortable surveillance of the transmission quality on the U-interface.

A block error is given if a U-frame with at least one code violation has been detected in the LT (near-end block error) or a positive M-symbol has been received from the NT (far-end block error). The NT transmits a positive M-symbol upstream if any code error has been detected within a frame (position 25 upstream in the U-frame from NT to LT).

The current status of the block error counter can be retrieved by the MON-8 command 'RDS'. Upon reception of 'RDS' the counter value is issued with the corresponding MON-8 message. If the block error counter is read it is automatically reset. The counter is also automatically reset in the course of a deactivation procedure. It is enabled again to count code violations from the moment the C/I code 'UAI' is written into the C/I-channel indicating that the U-line is sychronized (in state 'Line Active'). The counter does not overflow but stops at its maximum value (255).

Note that each counted frame with a detected code violation causes about 10 to 20 binary bit errors on average. So a bit error rate of 10^{-7} in both directions results in 2 detected frame errors within 1000 s in the LT (1 frame error detected in the NT and transmitted via M-symbol).

4.4.3 Bit Error Rate Counter

For bit error rate monitoring the DFE-T V2.1 features an 16-bit Bit Error Rate counter (BERC) per line. The measurement is performed for the B1, B2 and the D channel. Prerequisite is that loop #2 of the addressed line port has been closed before on the NT side via the M-channel.

The measurement is initiated by two BER control bits in the TEST register. As soon as the BER function is enabled zeros are sent in the selected channels and incoming ones are counted until the BER function has been disabled again by the user.

4.4.4 System Measurements

The DFE-T V2.1 features dedicated test modes to enable and ease system measurements. How these test modes can be used to conduct the most frequently needed system measurements is described in the following sections.

4.4.4.1 Send Single Pulses Test Mode (SSP)

In the send-single-pulses test mode, the U-transceiver transmits on the U-interface +1 pulses spaced by 1 ms. Two options exist for selecting the “Send-Single-Pulses” (SSP) mode:

– hardware selection: Pin-SSP= ’1’
– software selection: C/I code= SSP (0101_B)

Both methods are fully equivalent besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line. The SSP-test mode is required for pulse mask measurements.

4.4.4.2 Data Through Mode (DT)

If selected the data-through mode forces the DFE-T V2.1 directly into the “Transparent” state. This is possible from any state in the state diagram.

The Data-Through option (DT) provides the possibility to transmit a standard scrambled U-signal even if no U-interface wake-up protocol is possible. This feature is of interest if no counter station can be connected to supply the wake-up protocol signals. As with the SSP-mode, two options are available.

– hardware selection: Pin-DT= ’1’
– software selection: C/I code= DT (0110_B)

Note that the hardware selection offers the option to initiate further actions via C/I-code (e.g. simultaneous stimulation of an analog loop-back by C/I ’ARL’).

The DT-mode is required for power spectral density and total power measurements.

4.4.4.3 Master Reset Mode

The master-reset mode characterizes the mode where the U-transceiver does not transmit any signals. The chip is in the “Reset” state. All echo canceller and equalizer coefficients are reset. As can be seen from the state diagram, no activation is possible if the device is in the “Reset” state.

For measurements two methods are recommended in order to transfer the U-transceiver into the master-reset mode:

– hardware selection: Pin-$\overline{\text{RES}}$= ’0’
– software selection: C/I-code= RES (0001_B)

Both alternatives are fully compatible besides the fact that the SW selection is channel selective. The master-reset test mode is used for the return-loss measurements.

4.4.4.4 Pulse Mask Measurement

– Pulse mask is defined in FTZ Guideline 1TR 220 and ETSI TS 102 080
– U-interface has to be terminated with 150 Ω
– U-transceiver is in “Send-Single-Pulses” mode (C/I = ’SSP’ or Pin-SSP = ’1’)
– Measurements are done using an oscilloscope

4.4.4.5 Power Spectral-Density Measurement

– PSD is defined in FTZ Guideline 1TR 220 and ETSI TS 102 080
– U-interface has to be terminated with 150 Ω
– U-transceiver is in “Data-Through” mode (C/I = ’DT’ or Pin-DT= ’1’)
– For measurements a spectrum analyzer is employed

4.4.4.6 Return-Loss Measurement

– Return loss is defined in FTZ Guideline 1TR 220 and ETSI TS 102 080
– U-transceiver is in “Reset” state (C/I = ’RES’ or Pin-$\overline{\text{RES}}$= ’0’)
– Measure complex impedance “Z” from 5 kHz – 100 kHz
– Calculate return loss with formula:
RL(dB) = 20log (abs((Z + 150) / (Z –150)))

4.4.4.7 Quiet Mode Measurement

– Quite mode is defined in FTZ Guideline 1TR 220 and ETSI TS 102 080
– U-transceiver is in the “Reset” state (C/I = ’RES’ or Pin-$\overline{\text{RES}}$= ’0’)
– Trigger and exit criteria have to be realized externally

4.4.4.8 Insertion Loss Measurement

– Insertion loss is defined in FTZ Guideline 1TR 220 and ETSI TS 102 080
– U-transceiver is in “Data-Through” mode (C/I = ’DT’ or Pin-DT= ’1’)
– Trigger and exit criteria have to be realized externally

4.4.5 Retrieving DSP Data

Beyond the test and maintenance features described in the previous sections, the DFE-T V2.1 permits access to specific DSP data. Access is provided via the MON-12 protocol. The data transfer between the DSP and an external device is synchronized by two handshake signals, ’DATA_REQ’ and ’DATA_ACK’.

In the following text the technical term ’read’ stands for the process of sending a read request via the Monitor channel using the MON-12 protocol.

DSP Data Exchange via Handshake Signals

The handshake signal DATA_REQ is accommodated at bit position 0 in register DSP_DREQ, the handshake signal DATA_ACK at bit position 0 in register DSP_DACK.

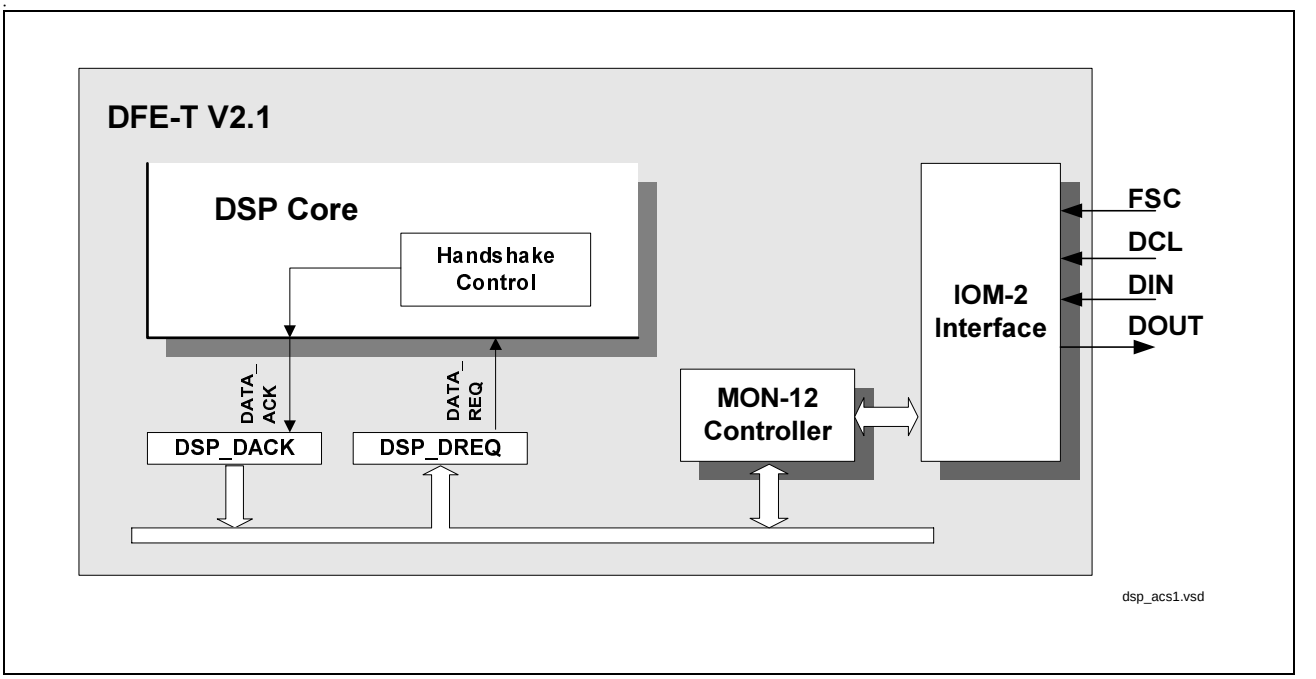


Figure 4-12 DSP Data Transfer Synchronization by Handshake Signals

Significance of DATA_REQ

Via DATA_REQ an external device is able to control the data exchange and to adapt the data rate to its needs.

- During a read access the layer-1 controller indicates with an active DSP_REQ signal (=’1’) that it requests new data.
- DATA_REQ set to ’0’ signals that the layer-1 controller is busy.

Significance of DATA_ACK

Signal DATA_ACK is controlled by the DSP.

- During a read access the DSP informs an external controller by DATA_ACK set to ’0’ that the data in the DSP Read Registers (DSP_RD1..3) has been updated.
- An active DATA_ACK bit (= ’1’) signals that the DSP is busy.

Below the single steps of the handshake protocol in the course of a read access is given.

Read direction (DSP -> Layer-1 controller):

1. Layer-1 controller polls if DATA_ACK bit is set to ’0’
2. Layer-1 controller signals its readiness for a read access by DATA_REQ= ’1’
3. DSP signals with DATA_ACK= ’0’ that the DSP_RD1..3 registers have been loaded
4. Layer-1 controller reads the DSP Read Registers, DSP_RD1..3

For subsequent read accesses this procedure has to be repeated

4.4.5.1 Reading Coefficient Values

By means of the DSP_RD1..3 registers it is possible to read coefficient values. The coefficient subsets of the various filter banks are addressable by the 3-bit DAT_TYP field in register DSP_CR2. Below the accessible coefficient clusters are listed:

’100’	Coefficient Set 1
’110’	Coefficient Set 2
’001’	Coefficient Set 3
’011’	Coefficient Set 4

Figure 4-13 shows the register structure that is provided for the access to coefficient values.

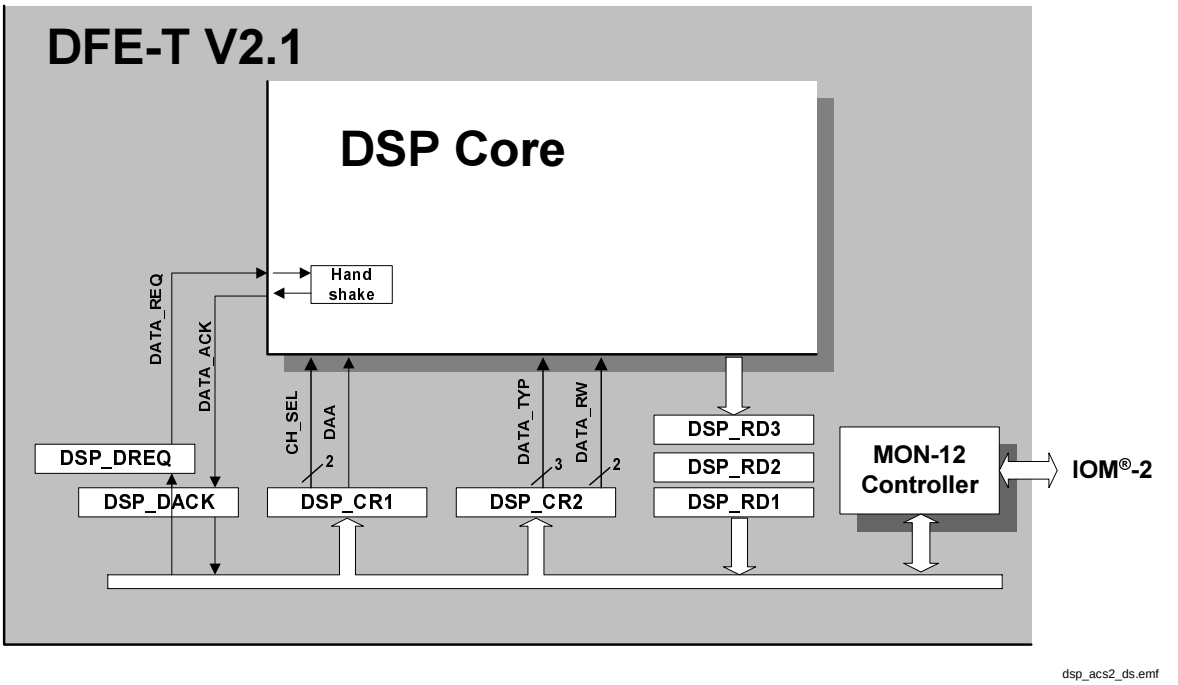


Figure 4-13 Provided DSP Registers for Access to Coefficient Data

To read out coefficient data the following programming sequence must be carried out

1. Select the addressed line port by CH_SEL in register DSP_CR1
2. Set DAA to ’1’ in register DSP_CR1. Thereby all coefficients are freezed.
3. Program the DSP Control Register No.2, DSP_CR2 as follows:
   - Select the proper coefficient type by DATA_TYP (e.g. coefficient set= ’100’)

     If the same coefficient set is repeatedly read out DSP_TYP must be set to another value and then reset again to the desired coefficient type. This is required to reset internal counters.

   - Set COM_MOD to ’1’ to enable the handshake mechanism
4. Trigger the read procedure by setting DATA_RW to ’01’ in register DSP_CR2.
5. Read out DSP_RD1..3 registers using either the handshake procedure as described in the chapter before.

4.4.6 Boundary Scan

The DFE-T V2.1 provides a boundary scan support for a cost effective board testing. It consists of:

- Complete boundary scan for 47 signals (pins) according to IEEE 1149.1 specification
- Test Access Port controller (TAP)
- Five dedicated pins (TCK, TMS, TDI, TDO, $\overline{\text{TRST}}$)
- Pins $\overline{\text{TRST}}$, TDI and TMS are provided with an internal pullup resistor
- One 32-bit IDCODE register
- Pin $\overline{\text{TRST}}$ tied to low resets the Boundary Scan TAP Controller
- Instructions CLAMP and HIGHZ were added, instruction SSP was removed in V2.1

Boundary Scan

All pins except the power supply pins, the "Not Connected" pins and the pins TDI, TDO, TCK, TMS, and $\overline{\text{TRST}}$ are included in the boundary scan chain. Depending on the pin functionality one, two or three boundary scan cells are provided.

Table 4-1 Boundary Scan Cells.

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	input
Output	2	output, enable
I/O	3	input, output, enable

When the TAP controller is in the appropriate mode data is shifted into or out of the boundary scan via the pins TDI/TDO using the 6.25 MHz clock on pin TCK.

The pins are included in the following sequence in the boundary scan chain:

Boundary Scan Number TDI –––>	Pin Number	Pin Name	Type	Number of Scan Cells
1.	62	**DT**	I	1
2.	61	CLS3	I/O	3
3.	60	$\overline{\text{RES}}$	I	1
4.	56	**SSP**	I	1
5.	55	SLOT0	I	1
In V2.1 pin 53 is not provided with a BScan cell (N.C.)				

Boundary Scan Number TDI –––>	Pin Number	Pin Name	Type	Number of Scan Cells
6.	52	CLS2	I/O	3
7.	51	D3D	I/O	3
8.	50	D2D	I/O	3
9.	49	**TP1**	I	1
10.	48	D1D	I/O	3
11.	47	D0D	I/O	3
12.	46	D3C	I/O	3
13.	45	SLOT1	I	1
14.	44	D2C	I/O	3
15.	43	D1C	I/O	3
16.	42	D0C	I/O	3
17.	40	D3B	I/O	3
18.	39	D2B	I/O	3
19.	37	D1B	I/O	3
20.	35	D0B	I/O	3
21.	34	D3A	I/O	3
22.	33	D2A	I/O	3
23.	32	**PUP**	I	1
24.	31	D1A	I/O	3
25.	30	D0A	I/O	3
26.	29	CLS0	I/O	3
27.	28	ST00	I	1
28.	27	ST01	I	1
29.	26	ST10	I	1
30.	24	ST11	I	1
31.	23	ST20	I/O	3
32.	21	ST21	I/O	3
33.	20	CLS1	I/O	3
34.	19	ST30	I/O	3
35.	18	ST31	I/O	3

Boundary Scan Number TDI –––>	Pin Number	Pin Name	Type	Number of Scan Cells
36.	17	SDX	I/O	3
37.	16	**MTO**	I	1
38.	15	DOUT	I/O	3
39.	14	DIN	I	1
40.	13	FSC	I	1
41.	12	DCL	I	1
42.	11	PDM0	I	1
43.	10	PDM1	I	1
44.	8	PDM2	I	1
45.	7	PDM3	I	1
46.	5	SDR	I	1
47.	4	CL15	I	1

TAP Controller

The *Test Access Port* (TAP) controller implements the state machine defined in the JTAG standard IEEE 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change. Before operation the TAP controller has to be reset by $\overline{\text{TRST}}$. According to the IEEE 1149 standard 7 instructions are executable. The instructions ’CLAMP’ and ’HIGHZ’ were added. Instruction ’SSP’ is no more supported since its function is identical to that of the SSP pin.

Table 4-2 TAP Controller Instructions:

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing
0011	IDCODE	Reading ID code
0100	CLAMP	Reading outputs

Code	Instruction	Function
0101	HIGHZ	Z-State of all boundary scan output pins
11XX	BYPASS	Bypass operation

EXTEST is used to examine the board interconnections.

When the TAP controller is in the state "update DR", all output pins are updated with the falling edge of TCK. When it has entered state "capture DR" the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.

When the TAP controller is in the state "update DR", all inputs are updated internally with the falling edge of TCK. When it has entered state "capture DR" the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

0001 (INTEST) is the default value of the instruction register.

SAMPLE/PRELOAD provides a snap-shot of the pin level during normal operation or is used to preload (TDI) / shift out (TDO) the boundary scan with a test vector. Both activities are transparent to the system functionality.

IDCODE Register

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

Version	Device Code	Manufacturer Code	Output	
0001	0000 0000 0110 0111	0000 1000 001	1	--> TDO

Note: In the state "test logic reset" the code "0011" is loaded into the instruction code register.

CLAMP allows the state of the signals included in the boundary scan driven from the PEF 24901 to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. These output signals driven from the DFE-T V2.1 will not change while CLAMP is selected.

HIGHZ sets all output pins included to the boundary scan path into a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by the DFE-T V2.1 outputs without incurring the risk of damage to the DFE-T V2.1.

BYPASS, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

5 Monitor Commands

This chapter summarizes the Monitor commands and messages that are available in an 4B3T U-Transceiver application. Please refer to section "IOM®-2 Monitor Channel" on page 3-5 for a detailed description of the Monitor handshake procedure.

Besides the existing MON-8 commands two new MON classes, MON-0 and MON-12 are introduced. MON-0 commands/messages provide access to the 1kbit/s transparent channel of the 4B3T frame. MON-12 commands allow to address new functions that are available with the 4B3T register map.

Defined MON-8 Commands

Chip identification, echocanceller coefficients and the block error counter can be read-out with two-byte MON-8 commands as given in **Table 5-1**. Each command is executed after having been transferred by proper use of the handshake procedure.

MON-8 commands have the 3rd highest priority.

Table 5-1 MON-8 Commands

Code	NT		LT		Function
(Hex)	D	U	D	U	
80 00		RID	RID		**Read Identification** requests the U-Transceiver to issue the ID code
80 EF		RDS	RDS		**Read and Reset the Block Error Counter**
DFE-T Specific MON-8 Functions					
81 7X (X= DCBA)			SETD		**Set Relay Driver Pins DiA, DiB, DiC, DiD** per port the status of 4 output pins can be set via this MON-8 command, Binary: 1000 0001 0111 DCBA
81 00			RST		**Read Request of Status Pins** via this MON-8 command information on the current status of general purpose input pins can be retrieved, per port 2 status pins are provided

The indications are summarized in **Table 5-2**. The messages "Answer Identification", "Answer Block Error Counter Read Request" and "Answer 'RST' Request" are two-byte messages.

Table 5-2 MON-8 Indications

Code (Hex)	NT D	NT U	LT D	LT U	Function
80 08	AID			AID	**Answer Identification** The DFE-T V2.1 replies the ID code.
80 XX	ARDS			ARDS	**Answer Block Error Counter Read Request** 2nd monitor byte contains the 8-bit counter value 'XX'

DFE-T Specific MON-8 Functions

88 0X (X= $00S_1S_0$)			AST		**Answer 'RST' Request** also issued without request on change of either STi0, STi1 pin, Binary: 1000 1000 0000 $00S_1S_0$

Defined MON-0 Commands

Following the systematics of 2B1Q MON-0 commands and messages are used to exchange transparent messages via the 4B3T Maintenance-channel. With the MON-0 command 'MWR' a 8-bit message can be transferred to the DFE-T V2.1. The DFE-T V2.1 then inserts the data bit for bit in the 1kbit/s transparent channel. The NT station stores the received bits until a 8-bit word is complete and sends out an autonomous MON-0 message 'MRD' which carries the received information.

The usage of the transparent channel must be enabled first by bit 'MTRANS' in register OPMODE. This can be done by a single MON-12 write command.

MON-0 commands have the 2nd highest priority (1st MON-12).

For more details on the access and synchronization issues please refer to the chapter "IOM®-2 Monitor Channel" on page 3-5.

Table 5-3 MON-0 Commands

Code	NT		LT		Function
(Hex)	D	U	D	U	
00 XX		MWR	MWR		**Send Transparent Message** data 'XX' is sent via the Transparent channel (M-Bit) across the U-interface

Table 5-4 MON-0 Indications

Code	NT		LT		Function
(Hex)	D	U	D	U	
00 XX	MRD			MRD	**Receive Transparent Message** data 'XX' that was received across the U-interface via the Transparent channel (M-Bit) is output

6 Register Description

In this section the complete register map is described that is provided with the new MON-12 protocol. For the protocol details please refer to page 3-11.

The register address arrangement is given in **Figure 6-1**. The U-interface registers are provided per line port. By register LP_SEL it can be determined which U register bank and by that which line port number is addressed. LP_SEL adds an offset value to the current address. The offset value is latched as long as register LP_SEL is overwritten again.

For access to DSP registers the MSB of the 8-bit wide address must be set to ’1’.

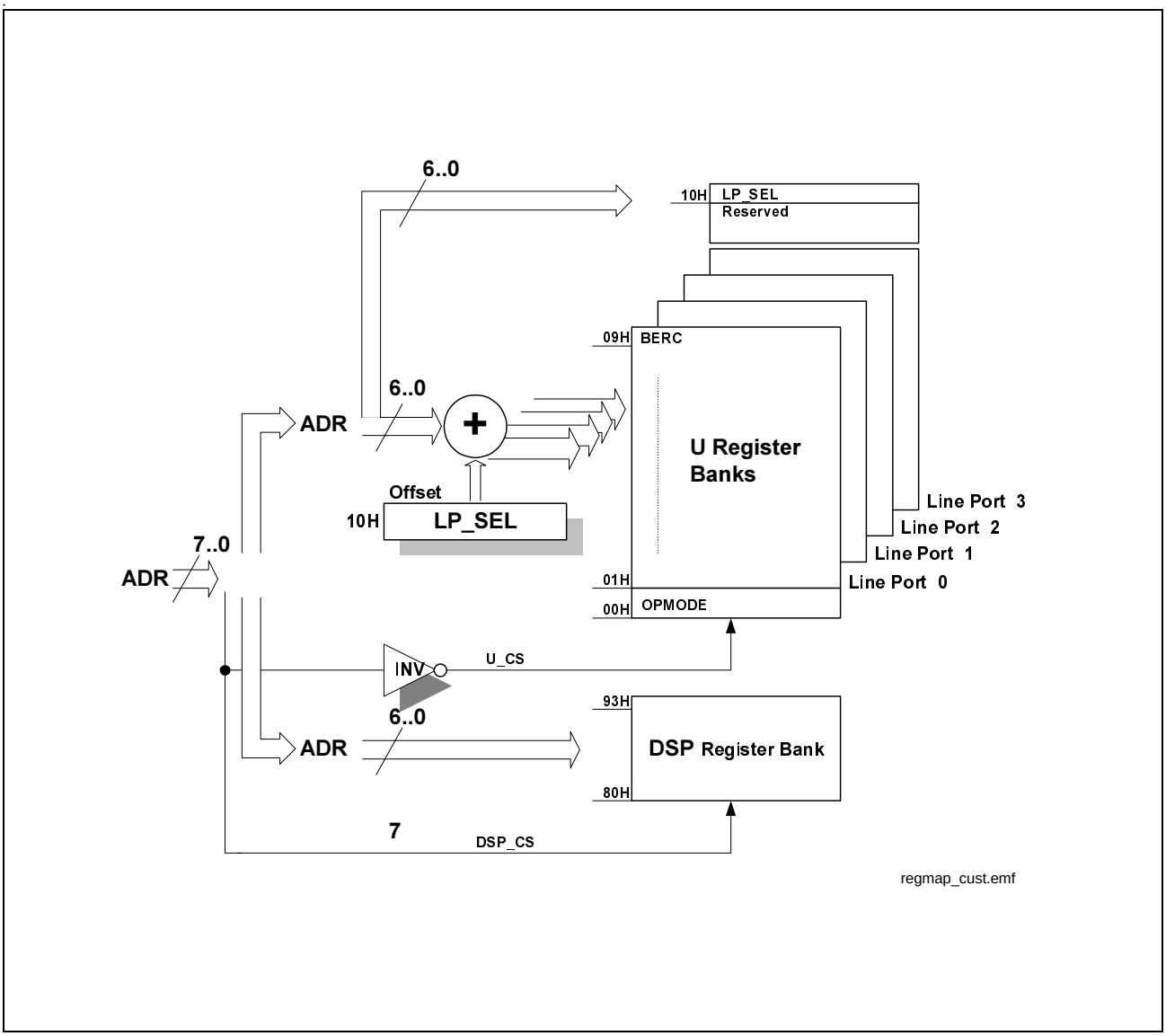


Figure 6-1 DFE-T V2.1 Register Map

6.1 Register Summary

	ADR	7	6	5	4	3	2	1	0	WR/RD	1/n Ch.
LP_SEL	10_H	0	0	0	0	0	0	LN2	LN1	**WR**/RD*	1

U-Interface Registers

OPMODE	00_H	0	0	M TRANS	0	0	0	1	0	**WR**/RD*	1
MRD	01_H	M-Bit data of the last 8 received U-frames								**RD**	1/4
MWR	02_H	M-Bit data of the next 8 transmit U-frames								**WR**	1/4
TEST	05_H	0	0	BER		0	0	0	0	**WR**/RD*	1/4
LOOP	06_H	0	DLB	TRANS	U/IOM	0	LBBD	LB2	LB1	**WR**/RD*	1/4
RDS	07_H	Block Error Counter Value								**RD**	1/4
BERC	08_H	BERC Counter Value (Bit 15-8)								**RD**	1/4
	09_H	BERC Counter Value (Bit 7-0)									

DSP Registers

		7	6	5	4	3	2	1	0		
DSP_CR1	80_H	0	CH_SEL		DAA	0	0	0	0	**WR**/RD*	1
DSP_CR2	81_H	0	0	1	DATA_TYP			DATA_RW		**WR**/RD*	1
DSP_DREQ	82_H	0	0	0	0	0	0	0	DATA _REQ	**WR**	1
DSP_DACK	90_H	0	0	0	0	0	0	0	DATA _ACK	**RD**	1
DSP_RD1	91_H	Coefficient Data								**RD**	1
DSP_RD2	92_H	Coefficient Data								**RD**	1
DSP_RD3	93_H	Reserved						Coefficient Data		**RD**	1

*) read-back function for test use

Table 6-1 Register Map Reference Table

Reg Name	Access	Address	Reset Value	Comment	Page No.
U-Interface Registers					
LP_SEL	WR	10_H	00_H	**Line Port Selection Reg.** line port 1 is selected by default	**6-4**
OPMODE	WR	00_H	02_H	**Opmode Register** LT mode, C/I channel controlled via IOM®-2	**6-5**
MRD	RD	01_H	00_H	**M-Bit Read Register** value meaningful after an activation	**6-6**
MWR	WR	02_H	00_H	**M-Bit Write Register** appropriate value must be loaded	**6-7**
TEST	WR	05_H	00_H	**TEST Register** all test modes disabled	**6-8**
LOOP	WR	06_H	00_H	**LOOP Register** transparent loop mode set, all local loops deactivated	**6-9**
RDS	RD	07_H	00_H	**Running Digital Sum Counter**	**6-10**
BERC	RD	08_H – 09_H	0000_H	**BER Counter Value**	**6-11**
DSP Registers					
DSP_CR1	WR	80_H	00_H	**DSP Control Register 1** all functions enabled	**6-12**
DSP_CR2	WR	81_H	20_H	**DSP Control Register 2** normal operation mode	**6-12**
DSP_ DREQ	WR	82_H	00_H	**DSP Data Request Register**	**6-14**
DSP_ DACK	RD	90_H	00_H	**DSP Data Acknowl. Register**	**6-15**
DSP_RD	RD	91_H–93_H	00_H	**DSP Read Registers**	**6-16**

6.2 Detailed Register Description

6.2.1 LP_SEL - Line Port Selection Register

The **Line Port Selection** register selects the register bank that is associated with the addressed line port. All line port specific register operations - line port specific registers are indicated by a ’4’ in the last column of the register summary - are performed on the line port that is addressed by the value of LP_SEL.

LP_SEL read/**write** Address: 10_H

Reset value: 00_H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LN2	LN1

LN2,1 Line Port Number

00 = Line port no. 0 is addressed by the following command

01 = Line port no. 1 is addressed by the following command

10 = Line port no. 2 is addressed by the following command

11 = Line port no. 3 is addressed by the following command

U-Interface Registers

6.2.2 OPMODE - Operation Mode Register

The **Op**eration **Mode** register determines the operating mode of the DFE-T V2.1.

OPMODE read*)/**write** Address: 00_H

Reset value: 02_H

7	6	5	4	3	2	1	0
0	0	M TRANS	0	0	0	MODE1 =1	MODE0 =0

MTRANS Enable/Disable Transparent Channel
(see "Exchanging Transparent Messages" on page 3-22)

0 = Transparent Channel disabled
M-channel transports only loop (LT-> NT) and code violation information (NT-> LT), no data is exchanged

1 = Transparent Channel enabled
transparent messages can be exchanged across the 1kbit/s M-channel using MON-0 commands and messages

MODE 1,0 Operation Mode Setting

10 = LT mode

6.2.3 MRD - M-Bit Read

The **M**-Bit **R**ead register contains the data of the last received eight M-bits. Data is shifted into the MRD register as soon as the transmission line is transparent. In combination with the MWR register it is possible to exchange transparent messages across the U-interface.

The value of MRD is output on IOM®-2 in a MON-0 message each time a 8-bit word has been stacked in the MRD register. The autonomous MON-0 message can be used to synchronize the MON-0 'MWR' command transmission in the opposite direction.

MRD read Address: 01_H

Reset value: 00_H

7	6	5	4	3	2	1	0
M Bit data of the last 8 received U-frames							

Received transparent channel messages are interpreted as follows

'0'= is mapped to logic '1' if no loop is requested
'+'= is mapped to logic '1' if a loop is requested simultaneously
'-'= is mapped to logic '0'

6.2.4 MWR - M-Bit Write Register

The **M**-Bit **W**rite register allows to transmit transparent messages across the U-interface. New data that is written to the MWR register is sent in the next 8 subsequent U-frames. After 8 U-frames zeros are sent if the MWR register is not reloaded again in time.

A MON-0 command ’MWR’ is provided which allows to overwrite the MWR register value. Use the periodic MON-0 ’MRD’ messages to synchronize the transmission of MON-0 ’MWR’ commands.

Note that transparent messages have priority and may override loopback commands.

MWR write Address: 02_H

Reset value: 00_H

7	6	5	4	3	2	1	0
M Bit data of the next 8 transmit U-frames							

MWR data is mapped to the following symbol values

0= is mapped to symbol ’0’ if no loopback is requested
is mapped to symbol ’+’ if a loopback is requested at the same time

1= is mapped to symbol ’-’

6.2.5 TEST - Test Register

The **Test** register sets the U-transceiver in the desired test mode. Note that the test modes 'Data Through' and 'Send Single Pulses' are activated via the C/I channel or by pin strapping.

TEST read*)/**write** Address: 05_H

Reset value: 00_H

7	6	5	4	3	2	1	0
0	0	BER		0	0	0	0

BER Bit Error Rate Measurement Function

allows to measure the BER of the B1-, B2- and D-channel in the Transparent state,
prerequisite: closed loopback on the NT side

a continuous series of zeros is sent

00 = Bit Error Rate (BERC) counter disabled

01 = Reserved

10 = Reserved

11 = Bit Error Rate counter (BERC) is enabled,
starts BER measurement for the B1-, B2- and D-channel,
zeros are sent in channel B1, B2 and D

6.2.6 LOOP - Loopback Register

The **Loop** register controls local digital loopbacks of the DFE-T V2.1. The analog loopback (No. 1) and remote loopbacks are closed by use of C/I codes. For the loopback configurations that are available by the LOOP register see also Chapter 4.4.1 on page 4-12.

LOOP read*)/**write** Address: 06_H

Reset value: 00_H

7	6	5	4	3	2	1	0
0	DLB	TRANS	U/IOM®	0	LBBD	LB2	LB1

DLB Close Framer/Deframer loopback

0 = Framer/Deframer loopback open

1 = Framer/Deframer loopback closed

TRANS Transparent/ Non-Transparent Loopback
in transparent mode data is both passed on and looped back whereas in non-transparent mode data is not forwarded but substituted by ’1’s (idle code) and just looped back

Note: has no effect on the analog loopback since ’ARL’ operates always in transparent mode

0 = transparent mode

1 = non-transparent mode
’1’s are sent on the IOM®-2 interface in the corresponding time-slot

U/IOM® Switch that selects whether looback LB1, LB2 or LBBD is closed towards U or IOM®-2

0 = LB1, LB2, LBBD loops are closed towards IOM®

1 = LB1, LB2, LBBD loops are closed towards U

LBBD Close complete loop (B1, B2, D) near the system interface
the direction towards the loop is closed is determined by bit ’U/IOM®’

0 = complete loopback open

1 = complete loopback closed

LB2 Close loop B2 near the system interface
the direction towards the loop is closed is determined by bit 'U/IOM®'

0 = loopback B2 open

1 = loopback B2 closed

LB1 Close loop B1 near the system interface
the direction towards the loop is closed is determined by bit 'U/IOM®'

0 = loopback B1 open

1 = loopback B1 closed

6.2.7 RDS - Block Error Counter Register

The Block Error Counter register 'RDS' monitors and counts code violations of the near-end and far-end side. The counter stops at 255 and does not overflow. If the register is read out or if the line is deactivated the block error counter is automatically reset to '0'.

The register value can be requested either by the MON-8 command 'RDS' or can be directly addressed using the MON-12 protocol.

RDS read Address: 07_H

Reset value: 00_H

7	6	5	4	3	2	1	0
Block Error Counter Value							

6.2.8 BERC - Bit Error Rate Counter Register

The **B**it **E**rror **R**ate **C**ounter register contains the number of bit errors that occurred during the period the bit TEST.BER was set active. If the register is read out it is automatically reset to ’0’

BERC read Address: $08/09_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
Bit Error Rate Counter Value							

7	6	5	4	3	2	1	0
Bit Error Rate Counter Value							

6.2.9 DSP Registers

DSP_CR - DSP Control Registers

Via the **DSP C**ontrol register 1 the operational function of the DSP core can be controlled. With the DSP Control register 2 the data type and access direction is determined for the data exchange between the DSP and an external controller.

DSP_CR1 read*)/**write** Address: 80_H

Reset value: 00_H

7	6	5	4	3	2	1	0
0	CH_SEL		DAA	0	0	0	0

CH_SEL Channel Selection
selects the addressed line port - subsequent data transfers are assigned to the selected line port no.

00= selects line port no. 0

01= selects line port no. 1

10= selects line port no. 2

11= selects line port no. 3

DAA Disable all adjust - freeze coefficients
line port selective command: takes only effect for the selected line port as set by CH_SEL

0= inactive

1= disables coefficient update

DSP_CR2 read*)/**write** Address: 81_H

Reset value: 20_H

7	6	5	4	3	2	1	0
0	0	1	DATA_TYP			DATA_RW	

DATA_TYP DSP Data Access Type

’100’	coefficients set 1
’110’	coefficients set 2
’001’	coefficients set 3
’011’	coefficients set 4

DATA_RW Read DSP Data

00 =	disabled
01 =	read DSP data
10, 11	reserved

DSP_DREQ - DSP Data Request Register

The **DSP D**ata **Req**uest register contains the handshake signal 'DATA_REQ' for communication between the DSP and an external microcontroller. DATA_REQ is controlled by an external controller and signals when the layer-1 controller requests new data.

DSP_DREQ **write** Address: 82_H

Reset value: 00_H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DATA_REQ

DATA_REQ DSP Data Request

0= External controller busy or inactive

1= indicates that the layer-1 controller has read the data and requests new data

DSP_DACK - DSP Data Acknowledge Register

The **DSP D**ata **Ack**nowledge register contains the handshake signal 'DATA_ACK' for communication between the DSP and an external microcontroller. DATA_ACK is controlled by the DSP and signals whether the DSP is busy or ready for new data access.

DSP_DACK **read** Address: 90_H

Reset value: 00_H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DATA_ACK

DATA_ACK DSP Data Acknowledge

0= DSP DATA register value has been updated

1= DSP busy

DSP_RD - DSP Read Registers

The **DSP Read** Data registers contain the data that have been requested by an external controller. The data type is determined by the setting of the DSP_CR2 register.

DSP_RD1 **read** Address: 91_H

Reset value: 00_H

7	6	5	4	3	2	1	0
Coefficient Data							

DSP_RD2 **read** Address: 92_H

Reset value: 00_H

7	6	5	4	3	2	1	0
Coefficient Data							

DSP_RD3 **read** Address: 93_H

Reset value: 00_H

7	6	5	4	3	2	1	0
Reserved						Coefficient Data	

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PEF	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 125	°C
IC supply voltage	V_{DD}	– 0.3 to 6	V
Input/Output voltage on any pin with respect to ground	V_S	– 0.3 to V_{DD} + 0.3 (max. 6)	V
Maximum current on all lines connected to the backplane when the DFE-T V2.1 is without power supply; at 3.3V external signal level	I_{max}	TBD	mA
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	2000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	– 40	85	°C	
Supply voltage	V_{DD}	3.0	3.6	V	
Ground	V_{SS}	0	0	V	

Note: In the operating range, the functions given in the circuit description are fulfilled.

7.3 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	– 0.3	0.8	V	
Input high voltage	V_{IH}	2.0	V_{DD} + 0.3	V	

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Output low voltage	V_{OL}		0.45	V	I_{OL} = 7 mA [1] I_{OL} = 2 mA [2]
Output high voltage	V_{OH}	2.4		V	I_{OH} = – 7 mA [1] I_{OH} = – 2 mA [2]
Avg. power supply current	I_{CC} (AV)		TBD	mA	V_{DD} = 3.3 V, T_A = 25 °C: DCL = 4.096 MHz Clock = 15.36 MHz
Input leakage current	I_{IL}	-1	1	µA	V_{DD} = 3.3 V, V_{SS} = 0 V; all other pins are floating; 0 V< V_{IN} < V_{DD}
Output leakage current	I_{OZ}	-1	1	µA	V_{DD} = 3.3 V, V_{SS} = 0 V; 0 V< V_{OUT} < V_{DD}

[1] Apply to: DOUT

[2] Apply to all the I/O and O pins that do not appear in the list in note **1)**

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

7.4 AC Characteristics

Inputs are driven to 2.4 V for a logical ’1’ and to 0.45 V for a logical ’0’. Timing measurements are made at 2.0 V for a logical ’1’ and 0.8 V for a logical ’0’. The AC testing input/output waveforms are shown in **Figure 7-1.**

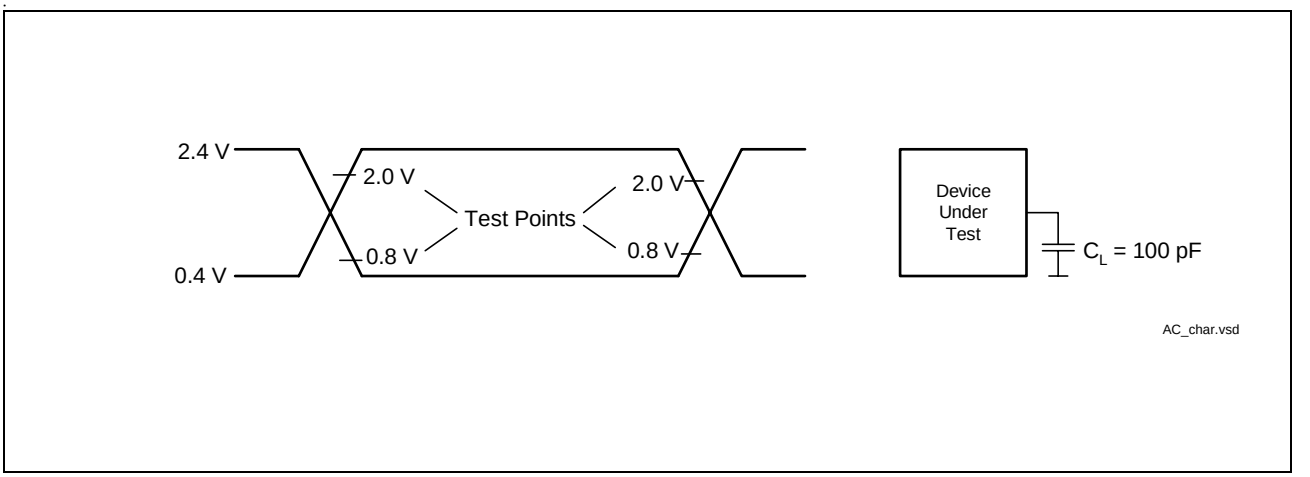


Figure 7-1 Input/Output Waveform for AC Tests

7.4.1 Reset Timing

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Active Low Period	$t_{\overline{RES}}$	200		ns	**reset is executed 400µs after the low active phase** **15.36MHz master clock has to be applied**

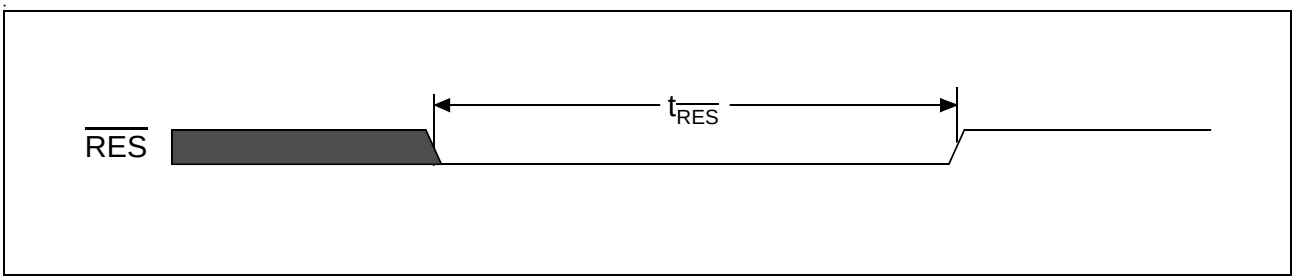


Figure 7-2 Reset Timing

7.4.2 IOM®-2 Interface Timing

The dynamic characteristics of the IOM®-2-interface are given in **Figure 7-3**. In case the period of signals is stated the time reference will be at 1.4 V; in all other cases 0.8 V (low) and 2.0 V (high) thresholds are used as reference.

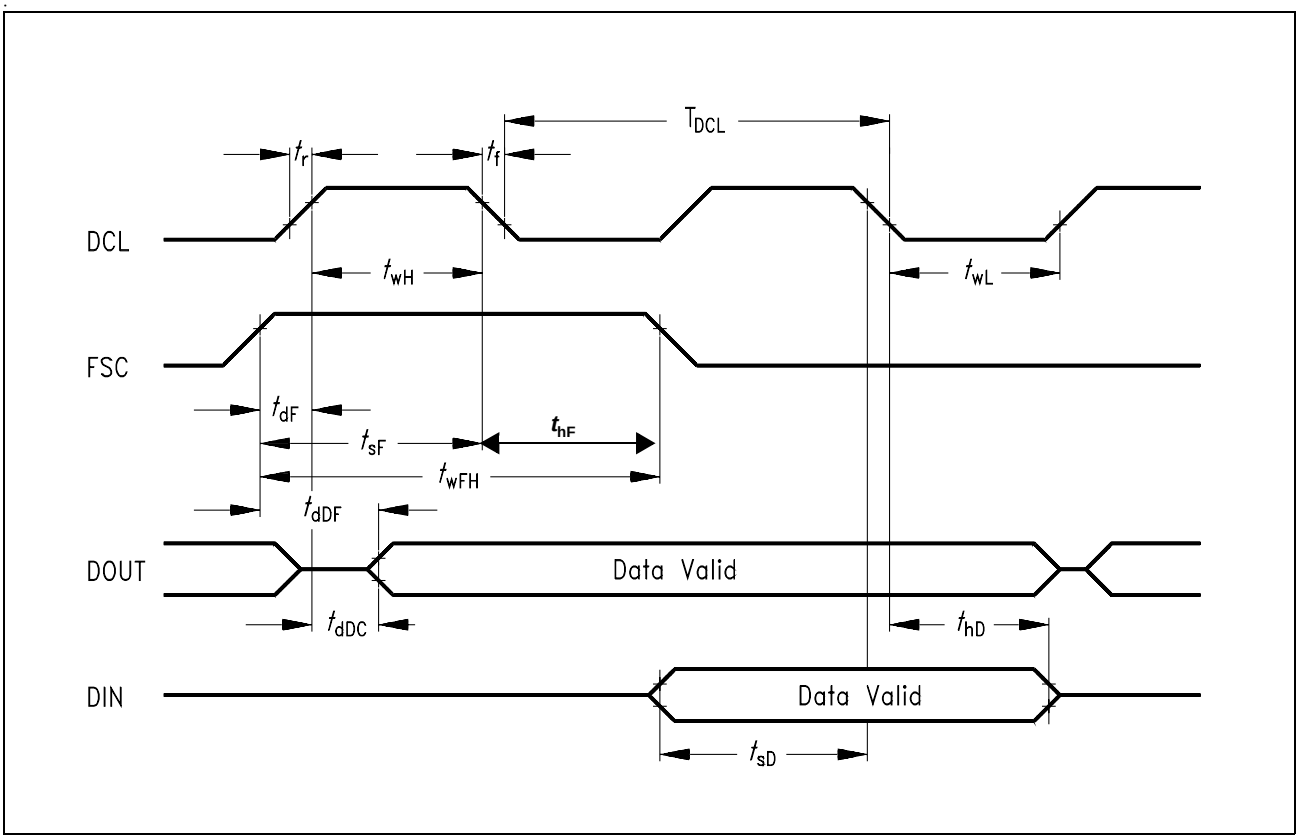


Figure 7-3 IOM®-2 Interface Timing (Double Clock Mode)

Table 7-1 IOM®-2 Dynamic Input Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCL rise/fall time	t_r, t_f			<60	ns
DCL period	T_{DCL}	122			ns
DCL pulse width, high low	t_{wH} t_{wL}	<53 <53	1/2 xT_{DCL} 1/2 xT_{DCL}		ns ns
FSC rise/fall	t_r, t_f			<60	ns
FSC setup time	t_{sF}	<30			ns
FSC hold time	t_{hF}	$t_{wFH} - t_{sF}$			ns
FSC advance	t_{dF}			$t_{wL} - 30$	ns

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
FSC pulse width, high low	t_{wFH} t_{wFL}	100 $2 \times T_{DCL}$			ns
Superframe FSC pulse width, high low	t_{wFH} t_{wFL}	100 $1 \times T_{DCL}$			ns
DIN setup time	t_{sD}	$< t_{wH} + 20$			ns
DIN hold time	t_{hD}	50			ns

Table 7-2 IOM®-2 Dynamic Output Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
DCL Data delay clock [1)]	t_{dDC}			<100	ns	C_L = 150 pF
FSC Data delay frame [1)]	t_{dDF}			<150	ns	C_L = 150 pF

Notes: [1)] The point of time at which the output data will be valid is referred to the rising edges of either FSC (t_{dDF}) or DCL (t_{dDC}). The rising edge of the signal appearing last (normally DCL) shall be the reference.

7.4.3 Interface to the Analog Front End

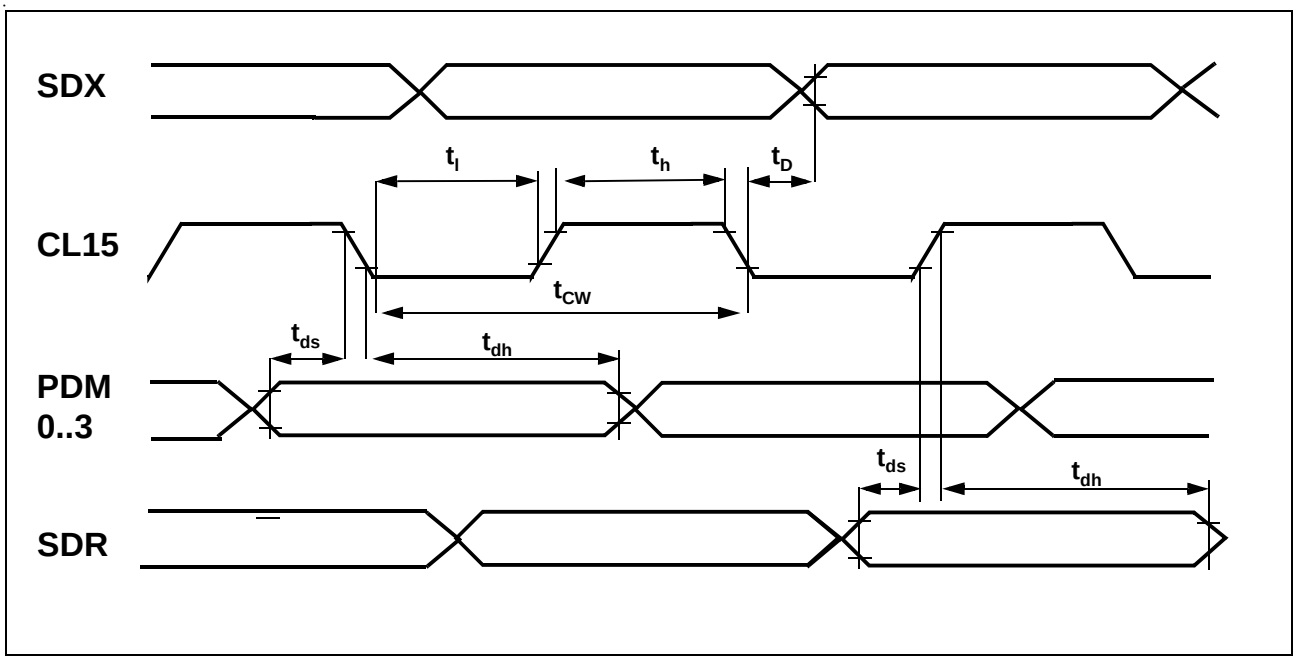


Figure 7-4 Dynamic Input and Output Requirements at the Analog Interface

Table 7-3 Dynamic Input Characteristics

Parameter	Signal	Symbol	Limit Values			Unit
			min.	typ.	max.	
Clock period	CL15	t_{cw}		65		ns
Pulse width high/ low	CL15	t_h t_l	25 25			ns ns
Data setup	SDR PDM0..3	t_{ds}	0 12			ns
Data hold	SDR PDM0..3	t_{dh}	15 8			ns

Table 7-4 Dynamic Output Characteristics

Parameter	Signal	Symbol	Limit Values			Unit
			min.	typ.	max.	
SDX data delay	SDX	t_D			22	ns

7.4.4 Boundary Scan Timing

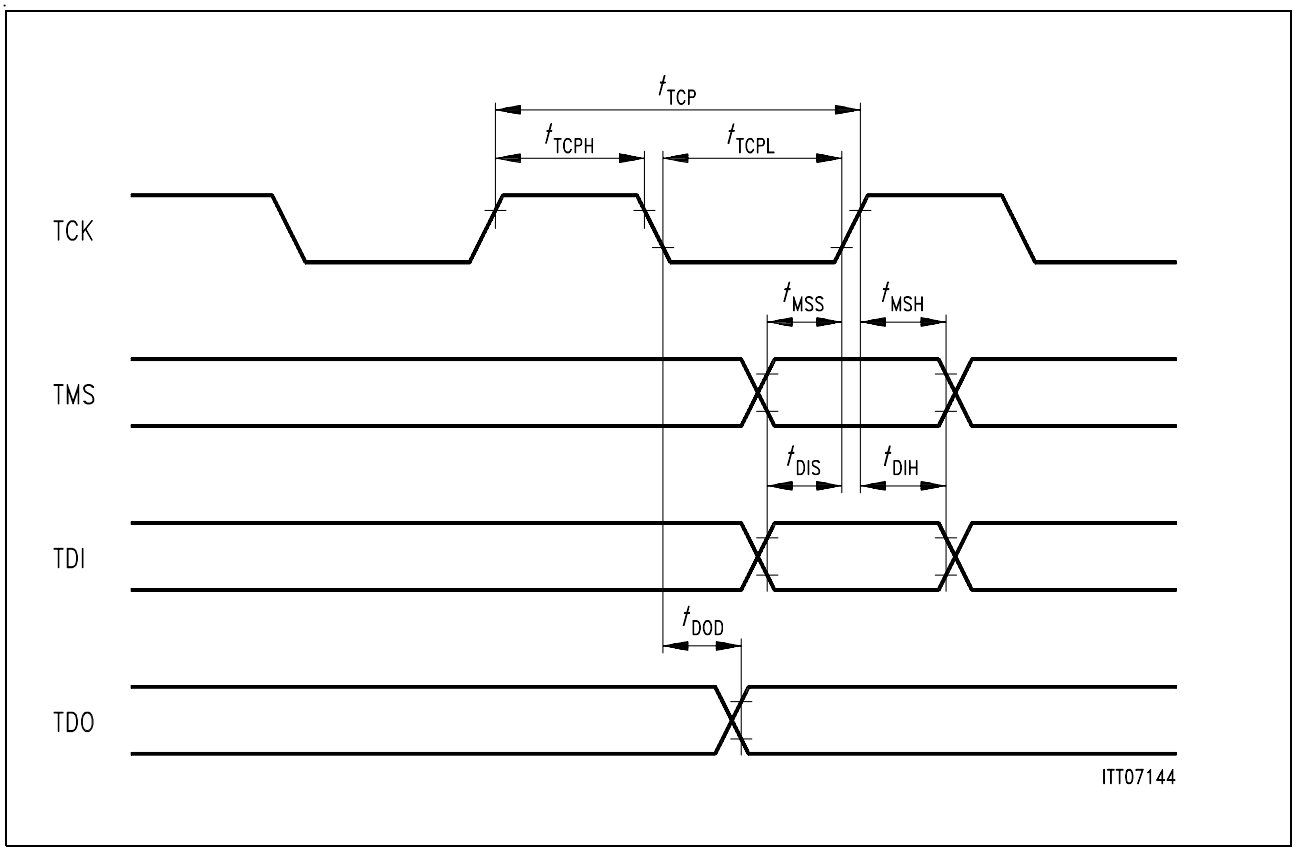


Figure 7-5 Boundary Scan Timing

Table 7-5 Boundary Scan Dynamic Timing Requirements

Parameter	Symbol	Limit Values		Unit
		min.	max.	
test clock period	t_{TCP}	160	-	ns
test clock period low	t_{TCPL}	70	-	ns
test clock period high	t_{TCPH}	70	-	ns
TMS set-up time to TCK	t_{MSS}	30	-	ns
TMS hold time from TCK	t_{MSH}	30	-	ns
TDI set-up time to TCK	t_{DIS}	30	-	ns
TDI hold time from TCK	t_{DIH}	30	-	ns
TDO valid delay from TCK	t_{DOD}	-	60	ns

7.5 Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Clock input capacitance	C_{XIN}		TBD	pF	f_C = 1 MHz The pins, which are not under test, are connected to GND
Input capacitance	C_{IN}		7	pF	
Output capacitance	C_{OUT}		10	pF	

7.6 Power Supply

7.6.1 Supply Voltage

V_{DD} to GND = +3.3V ±0.3V

7.6.2 Power Consumption

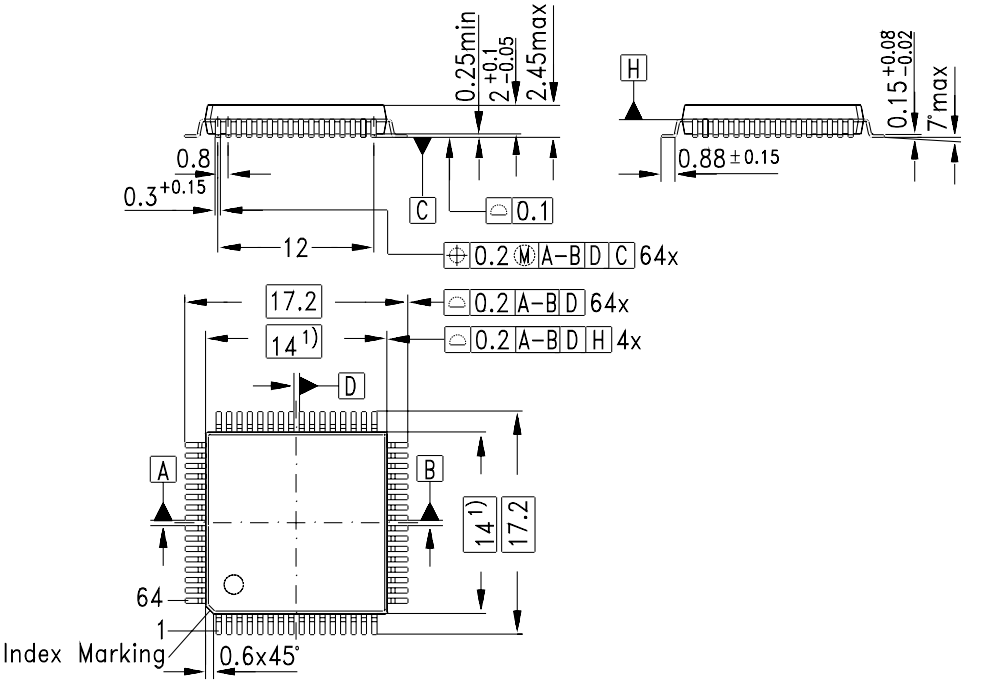
All measurements with random 2B+D data in active states, 3.3V (0°C - 70°C)

Table 7-6 Power Consumption

Mode	Typ. values	Max. values	Unit	Test conditions
Power-up all Channels	<50	<70	mA	3.3 V, open outputs, inputs at V_{DD} /V_{SS}
Power-down	<15	<25	mA	3.3 V, open outputs, inputs at V_{DD} /V_{SS}

8 Package Outlines

P-MQFP-64
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

GPM05247

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

9 Appendix A: Standards and Specifications

The table below lists the relevant standards concerning transmission performance the DFE-T V2.1 claims to comply with.

Organization		Valid for	Document	
ETSI	European Telecommunications Standards Institute	EU	TS 102 080 V1.3.1 (1998-11), formerly called ETR080	Transmission and Multiplexing (TM); Integrated Services Digital Network (ISDN) basic rate access; Digital transmission system on metallic local lines
FTZ	Fernmeldetechnisches Zentralamt	D	1 TR 220 08/91	Spezifikation der ISDN-Schnittstelle U_{k0} Schicht 1
			1 TR 210 11/87	ISDN Aktivierung/ Deaktivierung des Basisanschlusses Schicht 1
			1 TR 215 04/90	Euro-ISDN Aktivierung/ Deaktivierung des Basisanschlusses Schicht 1

10 Glossary

A/D	Analog to digital
ADC	Analog to digital converter
AGC	Automatic gain control
AIN	Differential U-interface input
ANSI	American National Standardization Institute
AOUT	Differential U-interface output
B1, B2	64-kbit/s voice and data transmission channel
BIN	Differential U-interface input
BOUT	Differential U-interface output
C/I	Command/Indicate (channel)
D	16-kbit/s data and control transmission channel
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DCL	Data clock
DD	Data downstream
DT	Data through test mode
DU	Data upstream
EC	Echo canceller
EOM	End of message
ETSI	European Telephone Standards Institute
FEBE	Far-end block error
FIFO	First-in first-out (memory)
FSC	Frame synchronizing clock
GND	Ground
HDLC	High-level data link control
IEC-Q	ISDN-echo cancellation circuit conforming to 2B1Q-transmission code
IOM®-2	ISDN-oriented modular 2nd generation
INFO	U- and S-interface signal as specified by ANSI/ ETSI
ISDN	Integrated services digital network
LBBD	Loop-back of B- and D-channels

LT	Line termination
MON	Monitor channel command
MR	Monitor read bit
MTO	Monitor procedure time-out
MX	Monitor transmit bit
NEBE	Near-end block error
NT	Network termination
PLL	Phase locked loop
PSD	Power spectral density
PTT	Post, telephone, and telegraph administration
PU	Power-up
RMS	Root mean square
S/T	Two-wire pair interface
SSP	Send single pulses (test mode)
TE	Terminal equipment
U	Single wire pair interface
4B3T	Transmission code requiring 120-kHz bandwidth

11 Index