Preliminary Data Sheet, DS1, Nov. 2000

MuPP µC

Multichannel Processor for POTS

PEB 31666 Version 1.3

PEB 31664 Version 1.3

Wired Communication

Infineon
technologies

Never stop thinking.

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Revision History:	**2000-11-06**	DS1
Previous Version:	Preliminary Target Specification DS2	

Page	Subjects (major changes since last revision)
Page 22	Interrupt (INTR) signal active level for Intel mode and Motorola mode added.
Page 23	Version register added to **Table 5**.
Page 26	Max. values for power dissipation added.
Page 27	**Figure 14** “Write Access to the µC-Interface Intel Mux Mode” modified.
Page 28	**Figure 15** “Read Access to the µC-Interface Intel Mux Mode” modified.
Page 29	**Figure 16** “Write Access to the µC-Interface Intel Demux Mode” modified.
Page 30	**Figure 17** “Read Access to the µC-Interface Intel Demux Mode” modified.
Page 31	**Table 6** “Timing Specifications µC-Interface Intel Mux/Demux Modes” replaces former tables 4-1 and 4-2.
Page 32	**Figure 18** “Write Access to the µC-Interface Motorola Mode” modified.
Page 32	**Figure 19** “Read Access to the µC-Interface Motorola Mode” modified.
Page 33	**Table 7** “Timing Specifications µC-Interface Motorola Mode” replaces former table 4-3.

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1 General Description

The highly integrated MuSLIC chip set supports to realize an extremely compact analog subscriber line interface module. Only a few external components are required and there is no trimming or adjustment necessary to meet worldwide recommendations.

The chip set consists of three out of seven available ICs:

Table 1 MuSLIC Chip Set ICs

PEB 31664 PEB 31665 PEB 31666	MuPP µC-S MuPP IOM®-2 MuPP µC-E	Multichannel Processor for POTS
PEB 3465	QAP	Quad Analog POTS
PEB 4164 PEB 4165 PEB 4166	AHV-SLIC-S AHV-SLIC AHV-SLIC-E	Advanced High Voltage Subscriber Line Circuit

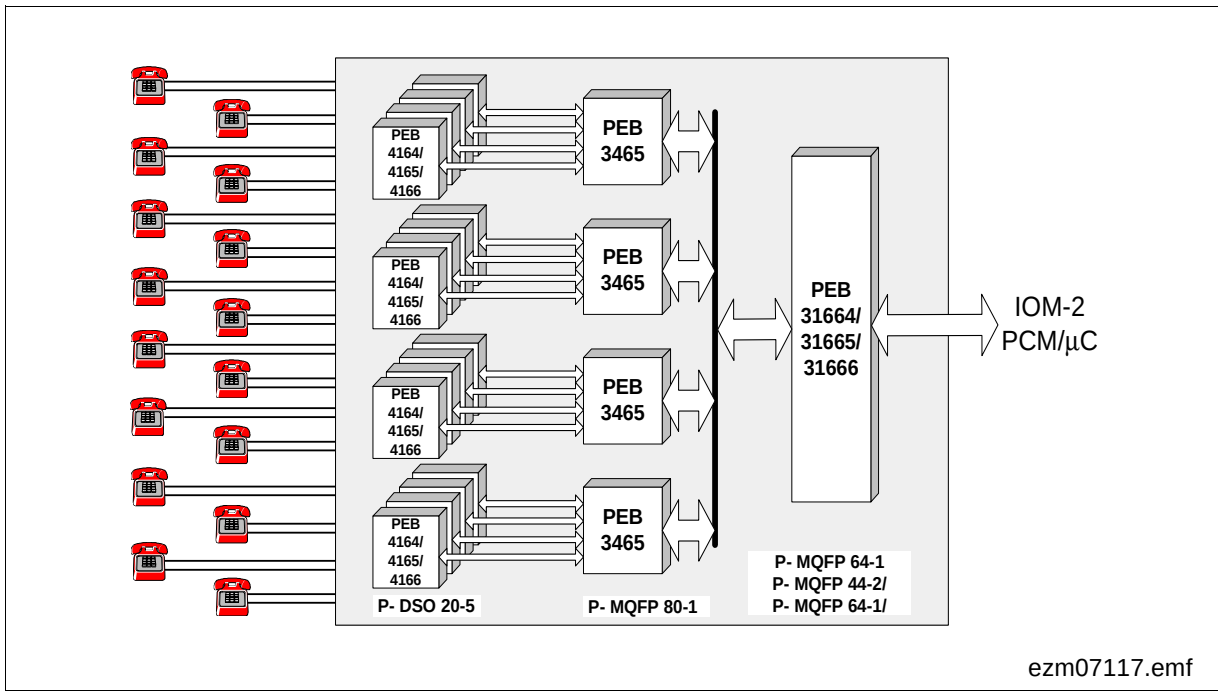


Figure 1 Application of an Analog Linecard for 16 Subscribers using MuSLIC

Note: The term "MuPP-µC" in this document applies to both chips MuPP µC-E (PEB31666) and MuPP µC-S (PEB31664).

The Multichannel Processor for POTS MuPP µC (MuPP IOM-2) offers all digital signal processing capabilities for 16 analog subscriber lines. It is a fully digital IC consisting of seven DSPs. Through their programmability, functions like DC-feeding, voice

processing, Teletax and metering functions are easy to adapt to country and line specific requirements.

Additionally with the Integrated Test and Diagnostic Functions (ITDF)[1)] the MuPP µC (MuPP IOM-2) offers a toolbox for integrated line and board testing.

The main functional difference between the two versions of the MuPP is the interface to the digital switching system. While the MuPP IOM-2 offers a IOM-2 interface, MuPP µC supports a PCM interface. Both of them have also a 8 bit µC interface as well as an efficient highspeed serial interface, which can interface to a maximum of four QAPs (PEB 3465).

Note: For system aspects and programming Bits refer to the Kit-Specification.

1) Teletax metering and ITDF are not available with MuPP µC-S.

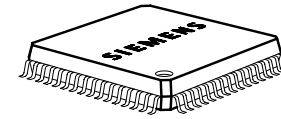
PRELIMINARY

Multichannel Processor for POTS MuPP µC

PEB 31666
PEB 31664

Version 1.3 **CMOS**

1.1 Features



P-MQFP-64-1

- Digital chip optimized for control of a 16 POTS-based system
- Only a few external components are required
- No trimming or adjustments are required
- Specification according to relevant ITU-T Q.552 Z interface, LSSGR and DTAG recommendations
- Digital signal processing technique
- Advanced low power CMOS[1)] technology
- PCM encoded digital voice transmission (A-Law or µ-Law)
- 8 bits parallel microcontroller interface for Intel- and Motorola- like processors
- Multiplexed and demultiplexed address mode possible
- Programmable digital filters for
  - Impedance matching
  - Transhybrid balancing
  - Frequency response
  - Gain
- Advanced test capabilities
  - Integrated line and circuit tests[2)]
  - Two programmable tone generators
- Fully digital programmable DC-Characteristic
  - Programmable constant current from 0 to 50 mA
  - Programmable resistive values from 0 to 2 × 800 Ω
  - Programmable constant voltage
- Programmable integrated Teletax injection and filtering during Active in on-hook and off-hook[2)]
  - Programmable up to 10 Vrms at Ring/Tip-wire of the AHV-SLIC
  - Programmable frequency (12/16 kHz)

1) Abbreviations see **Chapter 6**
2) not available with MuPP µC-S.

Type	Package
PEB 31666 V1.3	P-MQFP-64-1

- Polarity reversal (programmable soft or hard)
- Integrated (balanced) ringing generation with zero crossing injection[1)]
  - Programmable frequency between 16.6 and 70 Hz
  - Programmable amplitude up to 85 Vrms at Ring/Tip-wire of the AHV-SLIC
- Three operating modes: Power Down, Active and Ringing
- Off-hook detection with programmable thresholds for all operating modes
- Integrated Ring Trip detection with zero crossing turn off function
- Ground Start and Loop Start possible
- Integrated checksum calculation for CRAM (AC and DC separated)
- Linecard identification
- Standard SMD P-MQFP-64-1 packages

1) not available with MuPP µC-S

1.2 Pin Configuration

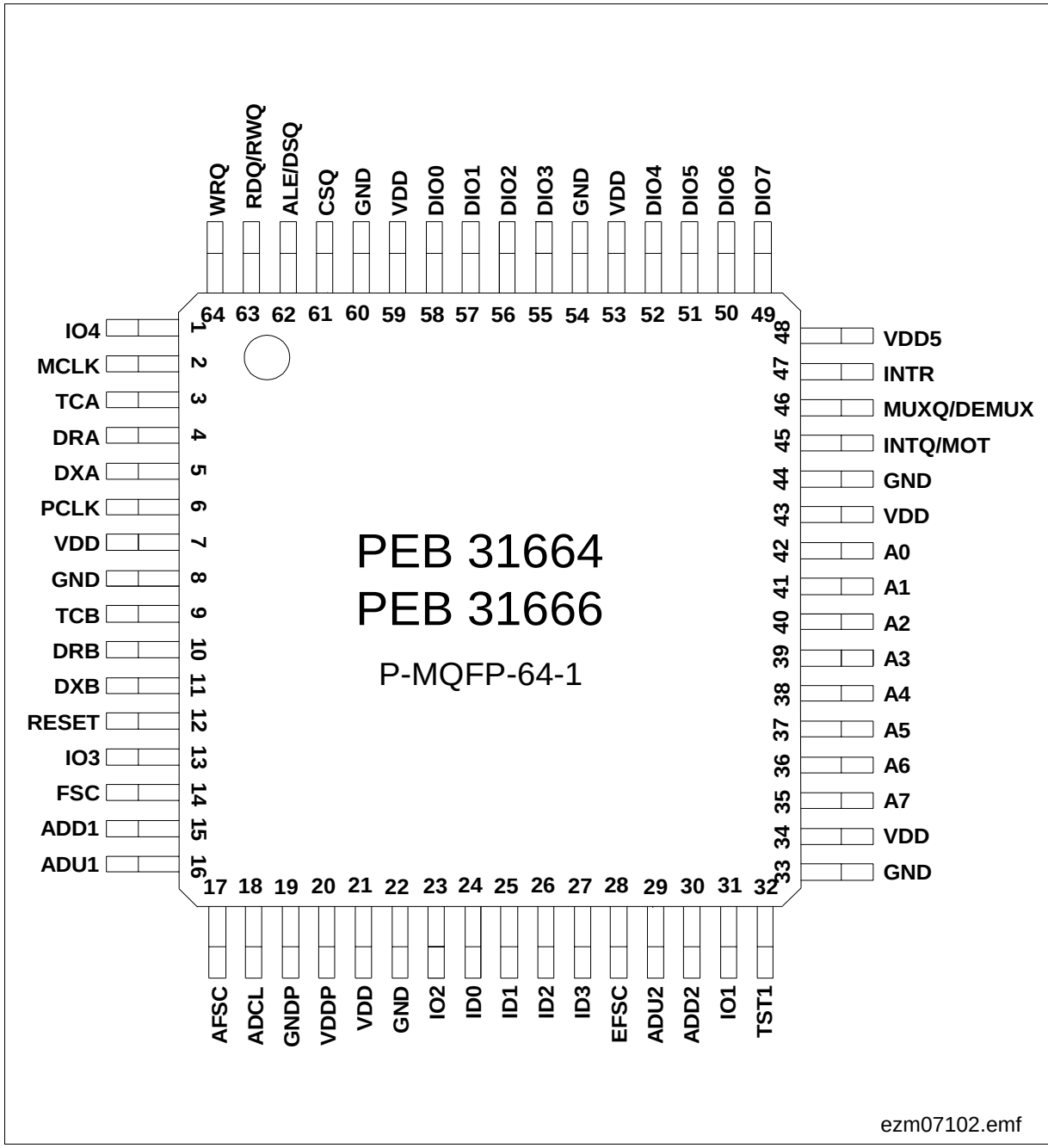


Figure 2 Pin Configuration (Top View)

1.2.1 Pin Definitions and Functions

The following tables group the pins according to their functions. They include pin number, pin name, type, a brief description of the function, and cross-references referring to the sections in which the pin functions are discussed.

Table 2 Pin Definitions and Functions

Pin No.	Name	Type	Function
Power Supply Pins			
8, 22, 33, 44, 54, 60	GND	–	Digital ground
19	GNDP	–	Digital ground for PLL
7, 21, 34, 43, 53, 59	VDD	–	+ 3.3 V digital supply voltage
20	VDDP	–	+ 3.3 V digital supply voltage for PLL
48	VDD5	–	+ 5 V digital supply voltage
PCM Pins			
3	TCA	O	Transmit control output for highway A, open drain
4	DRA	I	Receive data for highway A
5	DXA	O	Transmit data for highway A
9	TCB	O	Transmit control output for highway B, open drain
10	DRB	I	Receive data for highway B
11	DXB	O	Transmit data for highway B
6	PCLK	I	PCM-clock

Table 2 Pin Definitions and Functions (cont'd)

Pin No.	Name	Type	Function
MuPP µC/QAP Interface			
15	ADD1	O	1st QAP-bus data downstream
16	ADU1	I	1st QAP-bus data upstream
17	AFSC	O	QAP frame sync
18	ADCL	O	QAP data-clock
30	ADD2	O	2nd QAP-bus data downstream
29	ADU2	I	2nd QAP-bus data upstream
Microcontroller Interface			
2	MCLK	I	Master-clock (4.096 MHz)
14	FSC	I	frame sync
42	A0	I	Address 0
41	A1	I	Address 1
40	A2	I	Address 2
39	A3	I	Address 3
38	A4	I	Address 4
37	A5	I	Address 5
36	A6	I	Address 6
35	A7	I	Address 7
61	CSQ	I	µC chip select (active low)
62	ALE / DSQ	I	µC sddress latch enable / dataselect (active low), (Motorola)
63	RDQ / RWQ	I	µC data-clock read (active low)/ read-write (Motorola)
64	WRQ	I	µC data-clock write (active low)
46	MUXQ / DEMUX	I	µC multiplex / demultiplex mode
45	INTQ / MOT	I	µC Intel / Motorola mode

Table 2 Pin Definitions and Functions (cont'd)

Pin No.	Name	Type	Function
58	DIO0	I/O	µC data / address
57	DIO1	I/O	µC data / address
56	DIO2	I/O	µC data / address
55	DIO3	I/O	µC data / address
52	DIO4	I/O	µC data / address
51	DIO5	I/O	µC data / address
50	DIO6	I/O	µC data / address
49	DIO7	I/O	µC data / address
47	INTR	O	Interrupt
IO Pins			
31	IO1	I/O	User-programmable I/O pin
23	IO2	I/O	User-programmable I/O pin
13	IO3	I/O	User-programmable I/O pin
1	IO4	I/O	User-programmable I/O pin
Miscellaneous Function Pins			
12	RESET	I	Reset (active high)
24	ID0	I	External identification
25	ID1	I	External identification
26	ID2	I	External identification
27	ID3	I	External identification
28	EFSC	O	External ASIC frame sync
32	TST1	I	Test pin (for normal operation it must be connected to GND)
2	MCLK	I	Master clock 4.096 MHz
14	FSC	I	Frame sync

1.2.2 Functional Block Diagram

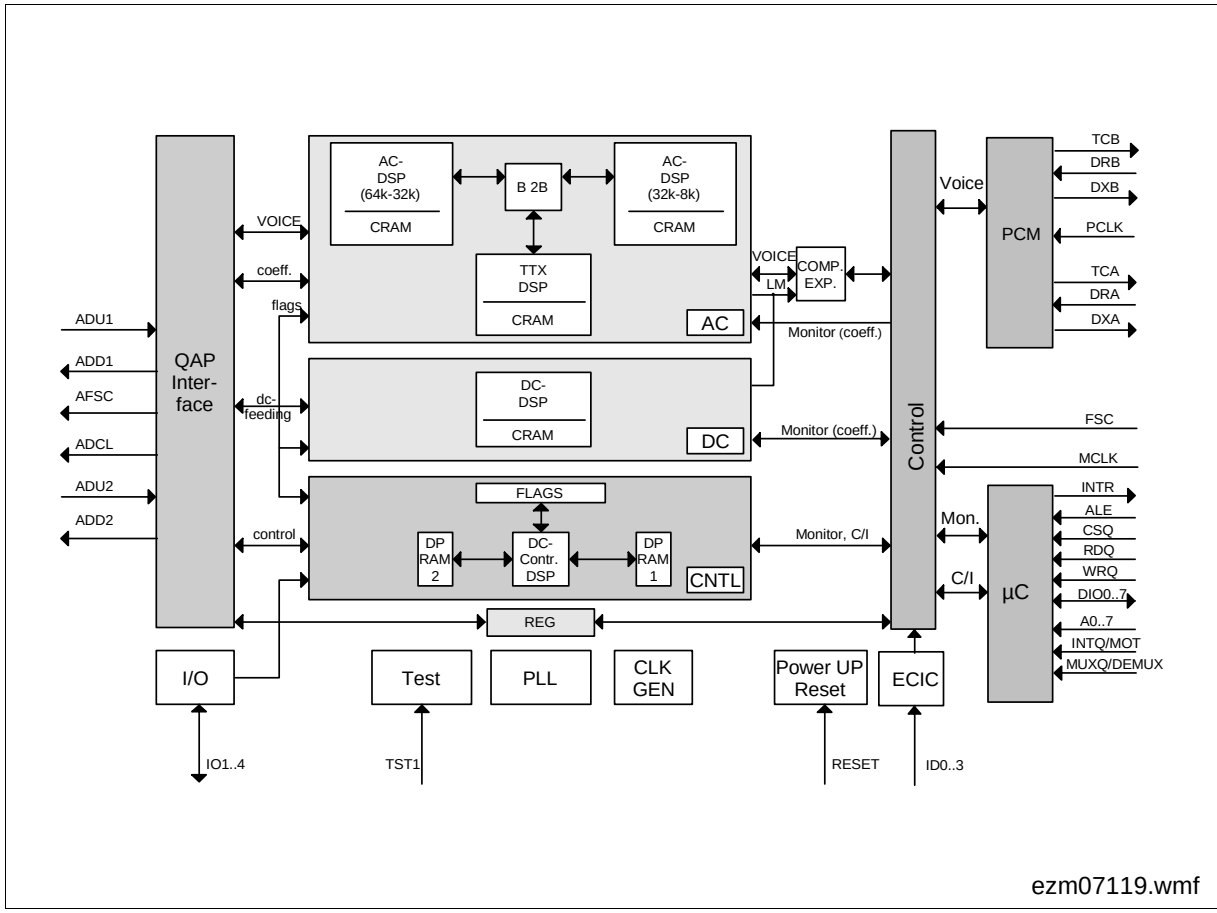


Figure 3 Functional Block Diagram

1.2.3 Application Diagram

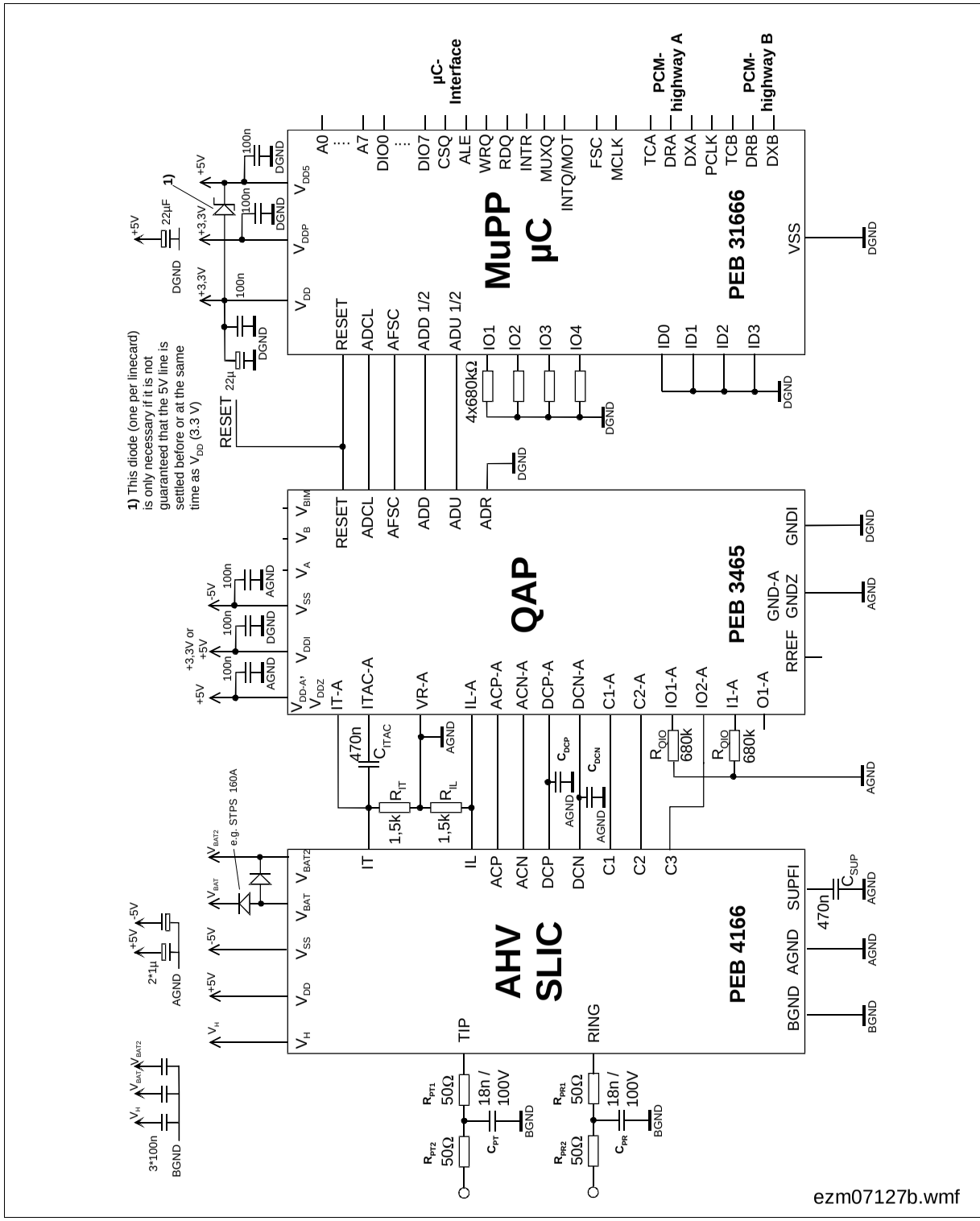


Figure 4 MuPP µC with QAP and AHV-SLIC (for one Subscriber)

Table 3 List of Components in Typical Application Circuit (Figure 4)

Symbol	Value			Unit	Tolerance
	min.	typ.	max.		
R_{PT1} [1)]	30	50		Ω	0,1 %
R_{PT2} [2)]	0	50		Ω	0,1 %
R_{PR1}	30	50		Ω	0,1 %
R_{PR2}	0	50		Ω	0,1 %
R_{IT}		1.5		kΩ	1 %
R_{IL}		1.5		kΩ	1 %
R_{QIO}		680		kΩ	5 %
R_{MIO}		680		kΩ	5 %
C_{PT}	0.2	18	20	nF	10 %
C_{PR}	0.2	18	20	nF	10 %
C_{ITAC}		470		nF	10 %
$C_{DCP/N}$		100		nF	10 %
C_{SUP}		470		nF	10 %

1) Absolut value not critical, but matching with RPR1 is important

2) Absolut value not critical, but matching with RPR2 is important

2 Functional Description

The Multichannel Signal Processing Subscriber Line Interface Codec Filter chip set, MuSLIC, is a logic continuation of the well established family of the Infineon Technologies PCM-Codec-Filter-ICs with the integration of all DC-feeding, supervision and meterpulse injection features on chip as well. Fabricated in advanced CMOS, BiCMOS and high voltage technology SPT170 the MuSLIC is tailored for very flexible solutions in analog/digital communication systems.

The chip set consists of the digital signal processor for 16 channels (MuPP µC, multichannel processor for POTS), the analog/digital and digital/analog converter for 4 channels (QAP, quad analog POTS) and the high voltage interface chip for 1 channel (AHV-SLIC, advanced high voltage subscriber line interface circuit).

The MuPP µC uses the benefits of a DSP not only for the voice channel but even for line feeding and supervision which leads to a very high flexibility without the need of external components. Based on an advanced digital filter concept, the PEB 31664 / PEB 31666 (MuPP µC) and the PEB 3465 (QAP) provides excellent transmission performance. The new filter concept leads to a maximum of independence between the different filter blocks. Each filter block can be seen as a one to one representative of the corresponding network element. Together with the software package MuSLICOS, filter optimizing to different applications can be done in a clear and straight forward procedure. The AC frequency behavior is mainly determined by the digital filters. Using the oversampling 1 bit ΣΔ-AD/DA converters, linearity is only limited by second order parasitic effects.

The digital solution of line feeding offers free programmability of feeding current and voltage as well as very fast settling of the DC-operating point after transitions. A 0.3 Hz lowpass filter in the DC-loop is mainly responsible for the system stability.

In MuPP µC-E additionally Teletax generation and filtering is implemented as well as free programmable balanced ring generation with zero-crossing injection. Off-hook detection with programmable thresholds is possible in all operating modes. To reduce overall power consumption of the linecard, the MuPP µC, the QAP and the AHV-SLIC provide a Power Down mode.

To program the MuSLIC or to get status information about the chip set or the system the MuSLIC has an 8-bit-parallel simple microcontroller interface.

The AHV-SLIC-E PEB4166 provides battery feeding between – 15 V and
– 80 V and ringing injection with a differential ring voltage up to 85 Vrms. In order to achieve these high amplitudes, an auxiliary positive battery voltage is used during ringing. This voltage can also be applied to drive very long telephone lines. The AHV-SLIC-S PEB4164 does not support this auxiliary positive voltage.

A kind of power management can be performed by using a second battery supply voltage for power saving at short lines.

The AHV-SLIC is designed for a voltage feeding - current sensing line interface concept and provides sensing of transversal and longitudinal currents on both wires. In Power

Down mode the AHV-SLIC is switched off turning the line outputs to a high impedance state. Off-hook supervision is provided by activating a ine current sensor.

2.1 Principles

2.1.1 Signal Flow Graph: AC

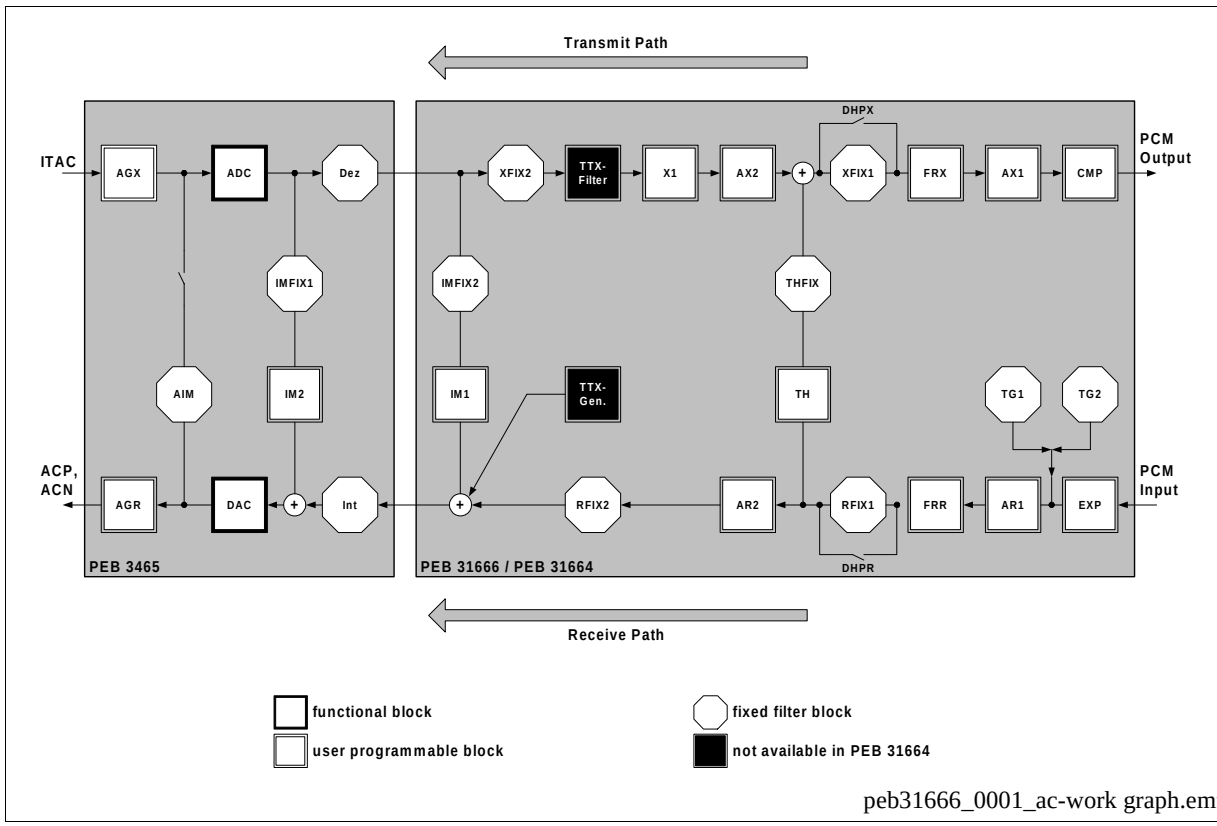


Figure 5 Signal Flow Graph: AC

Transmit Path

The analog input signal has to be connected to pin ITAC of the PEB 3465 by an external capacitor (470 nF) for AC/DC separation. After passing a programmable gain stage (AGX = 0, 3.5 or 9.5 dB) and a simple antialiasing prefilter the voice signal is converted to a 1-bit digital data stream in the Σ/Δ-converter. The first down sampling steps are done in fast running digital hardware filters on the PEB 3465. This down sampled AC-signal (64 kHz sampling rate) is sent to the PEB 31664 / PEB 31666 via the MuPP µC/QAP-Interface in the ADU-channel. The following signal processing is done in the DSP-machine of the PEB31664 / PEB31666. The benefits of this are the programmability of frequency and gain behavior. At the end the fully processed signal is transferred to the PCM Interface to the PCM Interface (A-law / µ-law / 16 Bit linear) signal representation.

Receive Path

The digital input signal is received via the PCM Interface of the PEB 31664 / PEB 31666. Expansion, PCM-lowpass-filtering, gain correction and frequency response correction are the next steps which are done by the DSP-machine. This 64 kHz AC signal is sent from the MuPP µC to the QAP via the MuPP µC/QAP-Interface in the ADD-channel. The up sampling interpolation steps are processed by fast hardware structures in the PEB 3465 to reduce the DSP-workload. The 1-bit data stream is then converted to an analog equivalent. A subsequent programmable gain stage (AGR = 0 or – 3,5 dB) and smoothing filter provides the AC output signal at the Pins ACP and ACN of the PEB 3465 for direct connection to the AHV-SLIC.

Loops

There are two different loops implemented: The Impedance Matching (IM) loop which is divided into 3 separate loops to guarantee very high flexibility to various impedances, and the Transhybrid Balancing (TH) loop.

2.1.2 Signal Flow Graph: DC

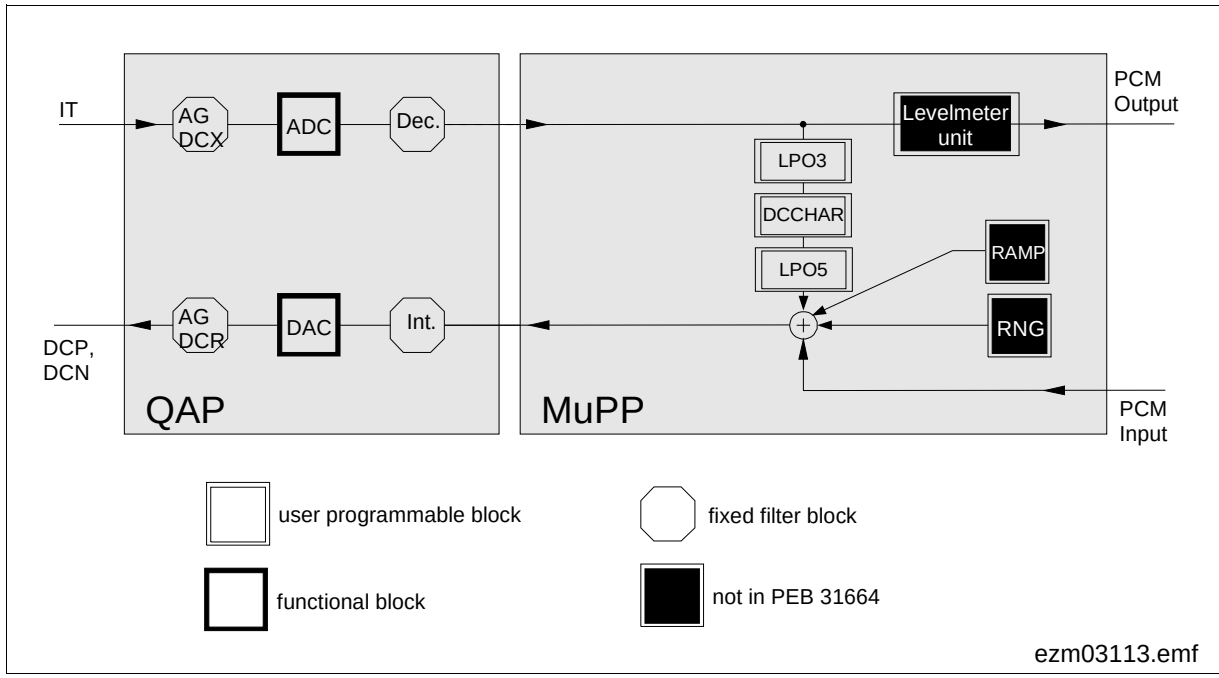


Figure 6 Signal Flow Graph: DC

DC Characteristic

The incoming information (transmit direction) at pin IT (scaled transversal AC + DC-current, transferred to a voltage via an external 1.5 kΩ resistor at IT) passes first an antialiasing filter and is then converted to a 1-bit digital data stream in the ΣΔ-converter. Down sampling is done in hardware filters of the PEB 3465. This DC-information (2 kHz sampling rate) is then fed to the PEB 31664 / PEB 31666 where it is first lowpass filtered (0.3 Hz corner frequency) for stability and noise reasons. The following DC-characteristic consists of three branches which represents different kinds of feeding behavior. In typical applications it acts as a programmable constant current source (R_{in} > 30 kΩ). If the desired value cannot be held feeding switches automatically and smoothly to the resistive branch (R_{in} programmable between 0 … 1.6 kΩ). The third branch is used for feeding long lines - the DC-characteristic switches to a constant voltage behavior. For superimposing voice as well as Teletax pulses the necessary drop at the line can be calculated and taken into account as well. The outgoing bit stream (2 kHz sampling rate), representing the DC-feeding value is then sent back to the PEB 3465 where a 1-bit ΣΔ-converter and a following smoothing filter (using external 100 nF capacitors) establish the desired values at the Pins DCP and DCN, respectively. Depending on the operating mode (Active, Ringing, Active with Boosted Battery) a gain of 0 or 4 dB is inserted.

For test purposes it is possible to close a loop to test either the analog part or the digital part of the DC path.

3 Interfaces

3.1 PCM-Interface

Two serial PCM-Interfaces are used for the transfer voice data. The PCM-Interface consist of 8 pins:

PCLK: PCM-clock, 512 kHz to 8192 kHz

FSC: Frame synchronization clock, 8 kHz

DRA: Receive data input for PCM-highway A

DRB: Receive data input for PCM-highway B

DXA: Transmit data output for PCM-highway A

DXB: Transmit data output for PCM-highway B

TCA: Transmit control output for PCM-highway A, active low during transmission

TCB: Transmit control output for PCM-highway B, active low during transmission

The Frame Sync (FSC) pulse identifies the beginning of a receive and transmit frame for all of the 16 channels. The PCLK clock is the signal to synchronize the data transfer on both lines DXA (DXB) and DRA (DRB). Bytes in all channels are serialized to 8 bit width and MSB first. As default setting, the rising edge indicates the start of the bit, while the falling edge is used to latch the contents of the received data on DRA (DRB). If the double clock rate is chosen (twice the transmission rate) the first rising edge indicates the start of a bit, while the second falling edge is used for latching the contents of the data line DRA (DRB) by default.

The data rate of the interface can vary from 2*512 kb/s to 2*8192 kb/s (2 highways). A frame may consist of up to 128 time slots of 8 bits each. In the time slot configuration registers SCR6 and SCR7 the user can select an individual time slot, and an individual PCM-highway, for any of the 16 voice channels. Receive and transmit time slots can be programmed individually in normal mode (PCM) and in linear mode. An extra delay of up to 7 clocks, valid for all channels, as well as the sampling slope may be programmed (see XR9).

When the MuPP µC is transmitting data on DXA (DXB), pin TCA (TCB) is activated to control an extra external driving device.

The following table shows possible examples for the PCM-Interface, other frequencies like 768 kHz or 1536 kHz are also possible.

Table 4 PCM-Interface Examples

	Frequency [kHz]	**Single/Double** [1/2]	**Time Slots** [per highway]	**Datarate** [kbit/s per highway]
	512	1	8	512
	1024	2	8	512
	1024	1	16	1024
	2048	2	16	1024
	2048	1	32	2048
	4096	2	32	2048
	4096	1	64	4096
	8192	2	64	4096
	8192	1	128	8192
Formula	**f**	**1**	**f/64**	**f**
Formula	**f**	**2**	**f/128**	**f/2**

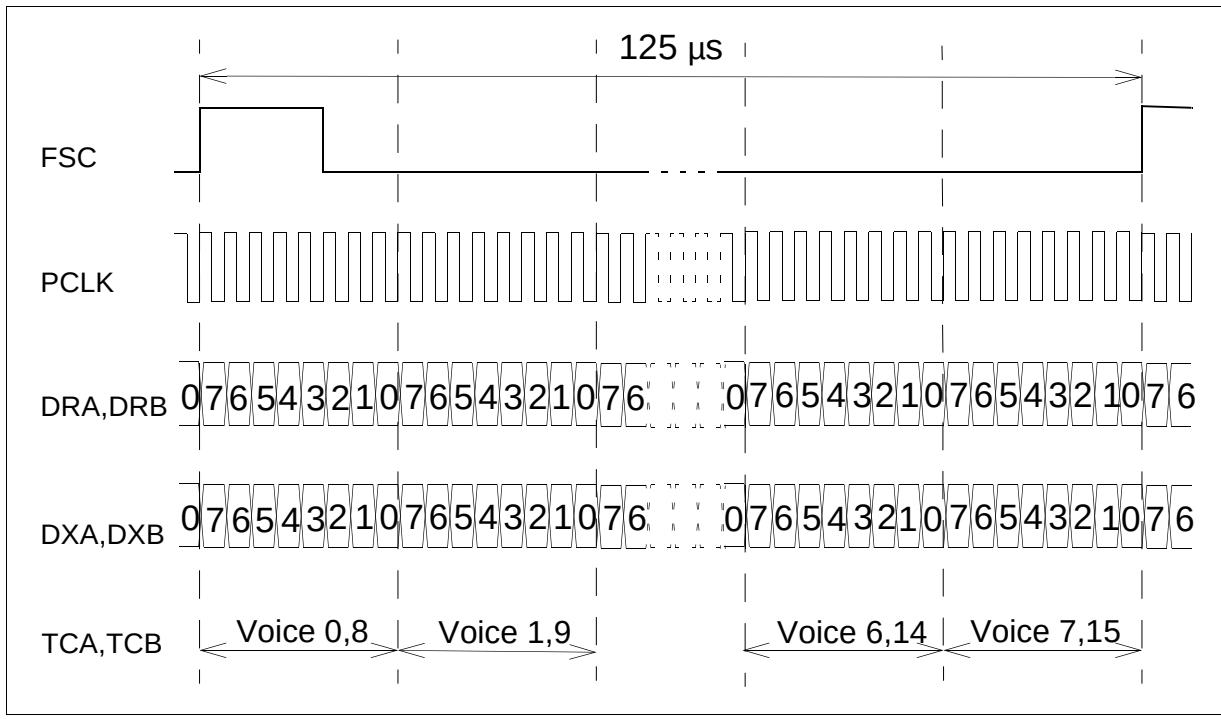


Figure 7 Example for Single Clock Rate, 512 kb/s

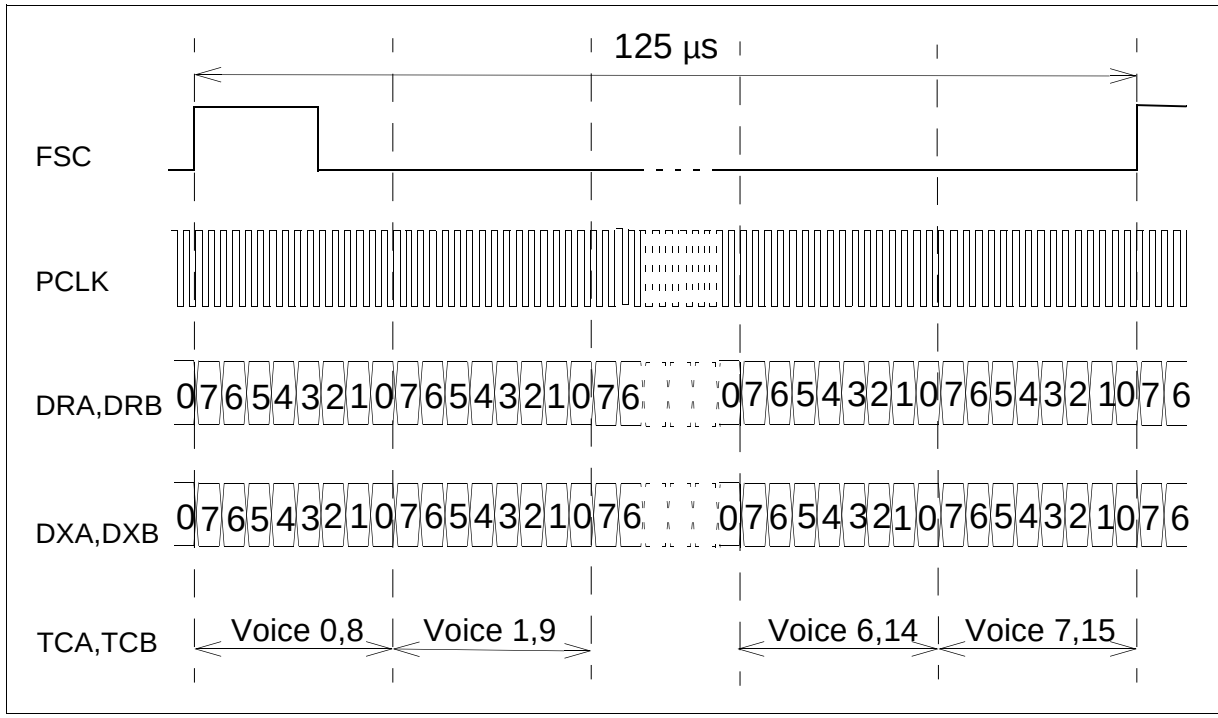


Figure 8 Example for Double Clock Rate, 512 kb/s

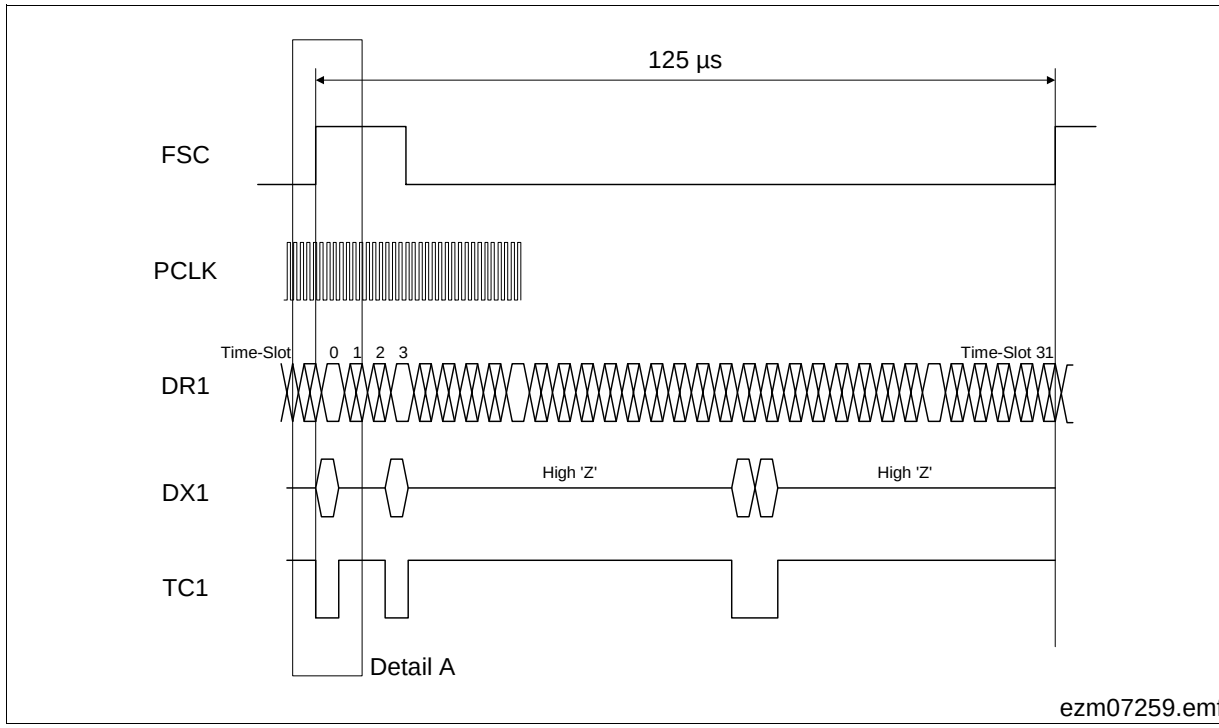


Figure 9 2048 kb/s, Single Clock Operation, only Highway A used

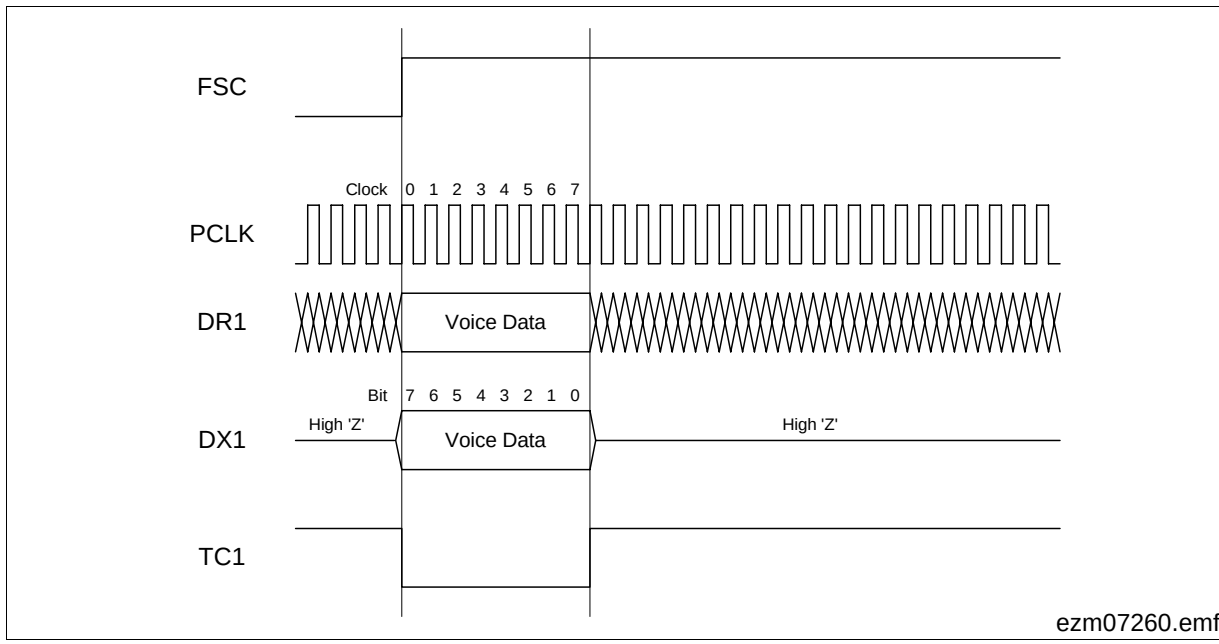


Figure 10 Detail A in Figure 9

For special purposes the DRA/B and DXA/B pins may be strapped together, and form bi-directional data-‘pin’ (SIP with the SLD-bus).

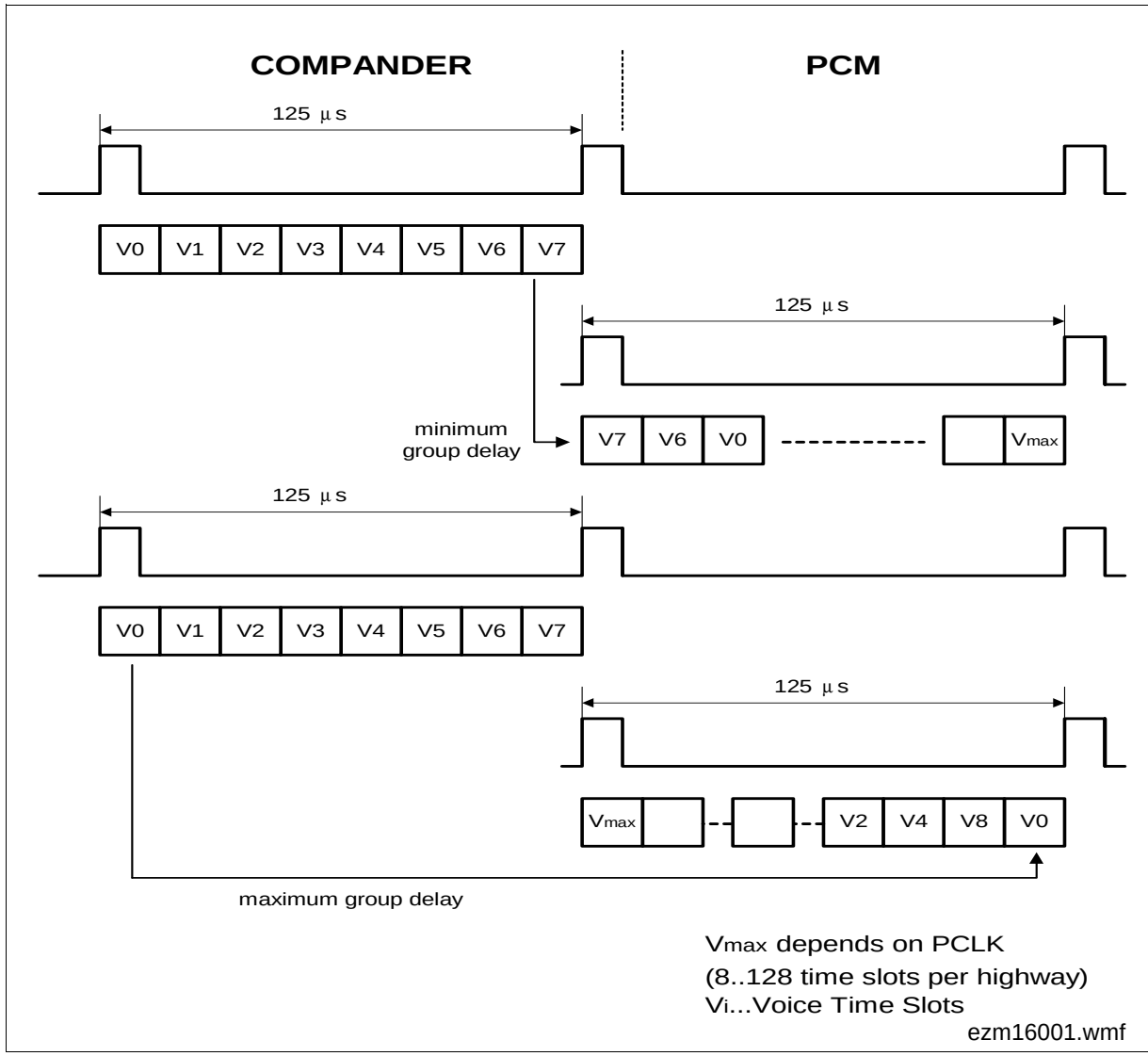


Figure 11 PCM-Group Delay Transmit

The group delay of the voice has 1 FSC (in average).

Figure 11 shows the conditions for the minimum and maximum group delay. In the minimum the group delay is almost 0, whereas in the maximum the delay will be almost 2 FSC's (~ 250 µs).

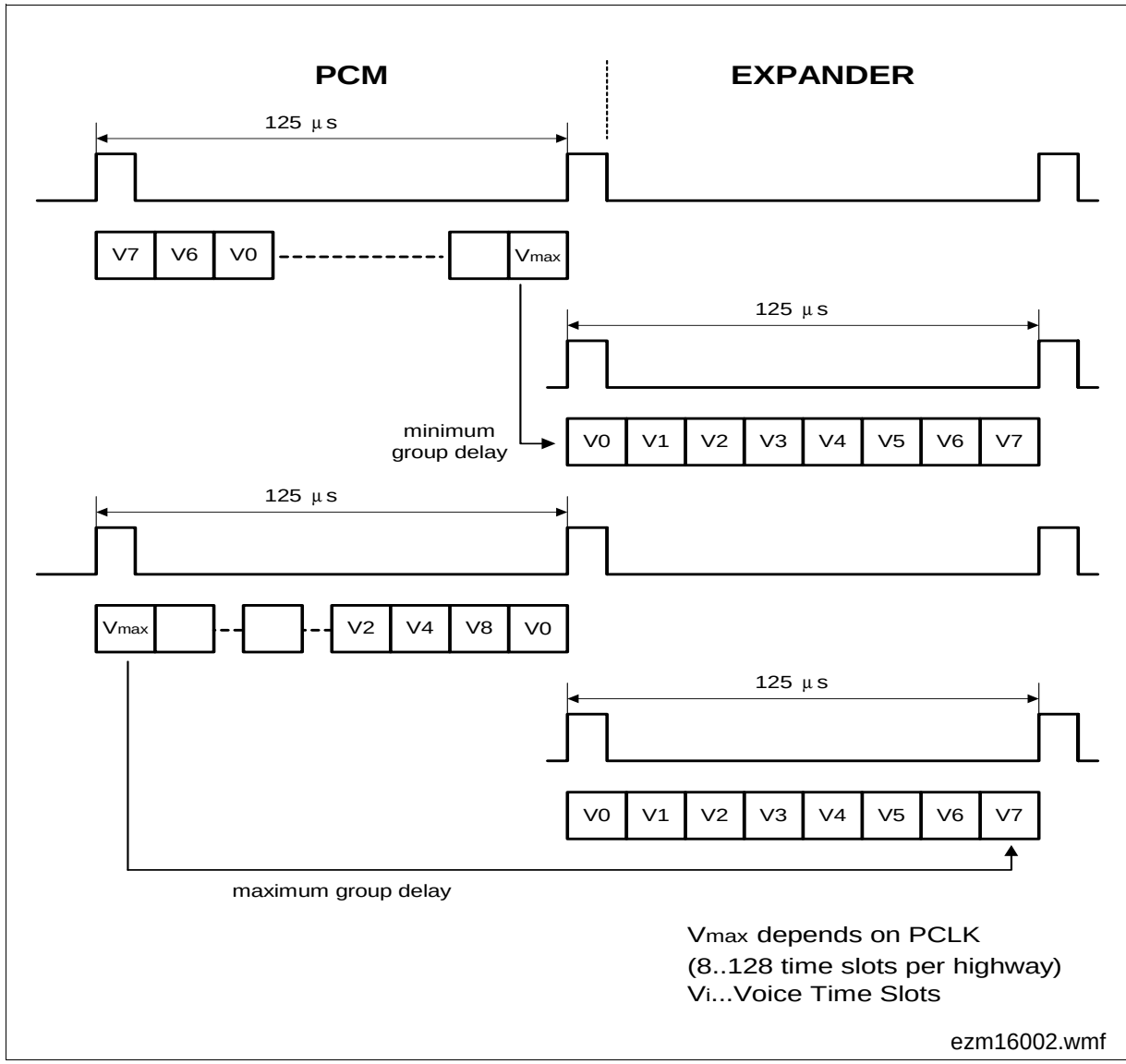


Figure 12 PCM-Group Delay Receive

The group delay of the voice has 1 FSC (in average).

Figure 12 shows the conditions for the minimum and maximum group delay. In the minimum the group delay is almost 0, whereas in the maximum the delay will be almost 2 FSC's (~ 250 µs).

3.2 µC-Interface

The parallel µC-Interface is used to communicate with an external master device and consists of six control lines (ALE/DSQ, CSQ, RDQ/RW, WRQ, DEMUX/MUXQ, INTQ/MOT), 8 bidirectional address/data lines (DIO0 … DIO7) and 8 address-lines (A0 ... A7) and provides fast parallel data transfer to a microcontroller device (Intel compatible and Motorola compatible families).

The µC-Interface of the MuPP µC has a multiplexed / non multiplexed 8-bit address/data bus and allows direct connection to a microcontroller of the Intel 8051-(MCS51/251-) family, the Infineon Technologies C16X-family and Motorola M68HCXX or M683XX[1)] family without additional components.

Intel / Infineon Technologies family:

Intel multiplexed mode:

MUXQ/DEMUX = 0

INTQ/MOT = 0

INTR active high

With each falling edge of ALE-line the MuPP µC latches the bus data on the 8 data lines DIO0 … DIO7 and stores it as an address information. CSQ combined with RDQ or WRQ starts the data transfer cycle via the parallel µC-Interface. If CSQ is low, the data on DIO0 … DIO7 will be valid on the rising edge of WRQ/RDQ (see **Page 27**). Depending on the previously latched address information, these data have a different meaning.

In case of a reset command for the µC-Interface the address information 0000 0011 has to be sent together with the data information 1010 1010.

Data transfer to and from the MuSLIC is asynchron and the data will be transferred in bytes.

Intel demultiplexed mode:

MUXQ/DEMUX = 1

INTQ/MOT = 0

INTR active high

In Intel demultiplexed mode, the address- and the data-information is given on separate bus lines A0 ... A7 and DIO0 ... DIO7.

Every falling edge of the ALE-line latches the address information. CSQ combined with RDQ or WRQ starts the data transfer cycle in the same way as in the multiplexed mode.

Motorola demultiplexed mode

MUXQ/DEMUX = X (don’t care)

INTQ/MOT = 1

INTR active low

In Motorola mode address information and data information are given on separate bus lines (A0 ... A7, DIO0 ... DIO7). The address information has to be valid before RDQ/RWQ and ALE/DSQ are indicating a read- or write-cycle. The data information is latched by the raising edge of the ALE/DSQ signal (see **Page 27**)**.**

Table 5 Possible Address Information to Identify the Following Data Nibbles

Address	Command	Function
00000000, 00H	Channel	Preselection of channel for channel specifc commands SOP, TOP, COPI
00000001, 01H	Status	Status register to control the read/ write-operations
00000010, 02H	Interrupt register (read only)	Indicates channel and sources of pending interrupts
00000011, 03H	Reset	Reset of the µC-Interface by write of data 0AAH to this address
00000100, 04H	Reserved	
00000101, 05H	Interrupt Channel Reg. 1	Indication of pending interrupts on channel 0..7
00000110, 06H	Interrupt Channel Reg. 2	Indication of pending interrupts on channel 8..15
00000111, 07H	Data	Data port for all register read/write-operations
00001100, 0CH	Version register	When read, indicates the version of the MuPP µC device in hexadecimal representation. Value returned by current version = 13H

3.3 MuPP µC/QAP-Interface

The MuPP µC/QAP-Interface, the link between the MuPP µC and the QAP, is a serial interface based on the 6 signals AFSC (analog frame sync), ADCL (analog data clock), ADU1/ADU2 (analog data upstream) and ADD1/ADD2 (analog data downstream). ADU1 and ADD1 are common to the first group of 8 time slots (channels) and ADU2 and ADD2 to the second 8 time slots (channels). AFSC and ADCL are common to both groups of time slots (timing diagram see **Chapter 4.3.2**).

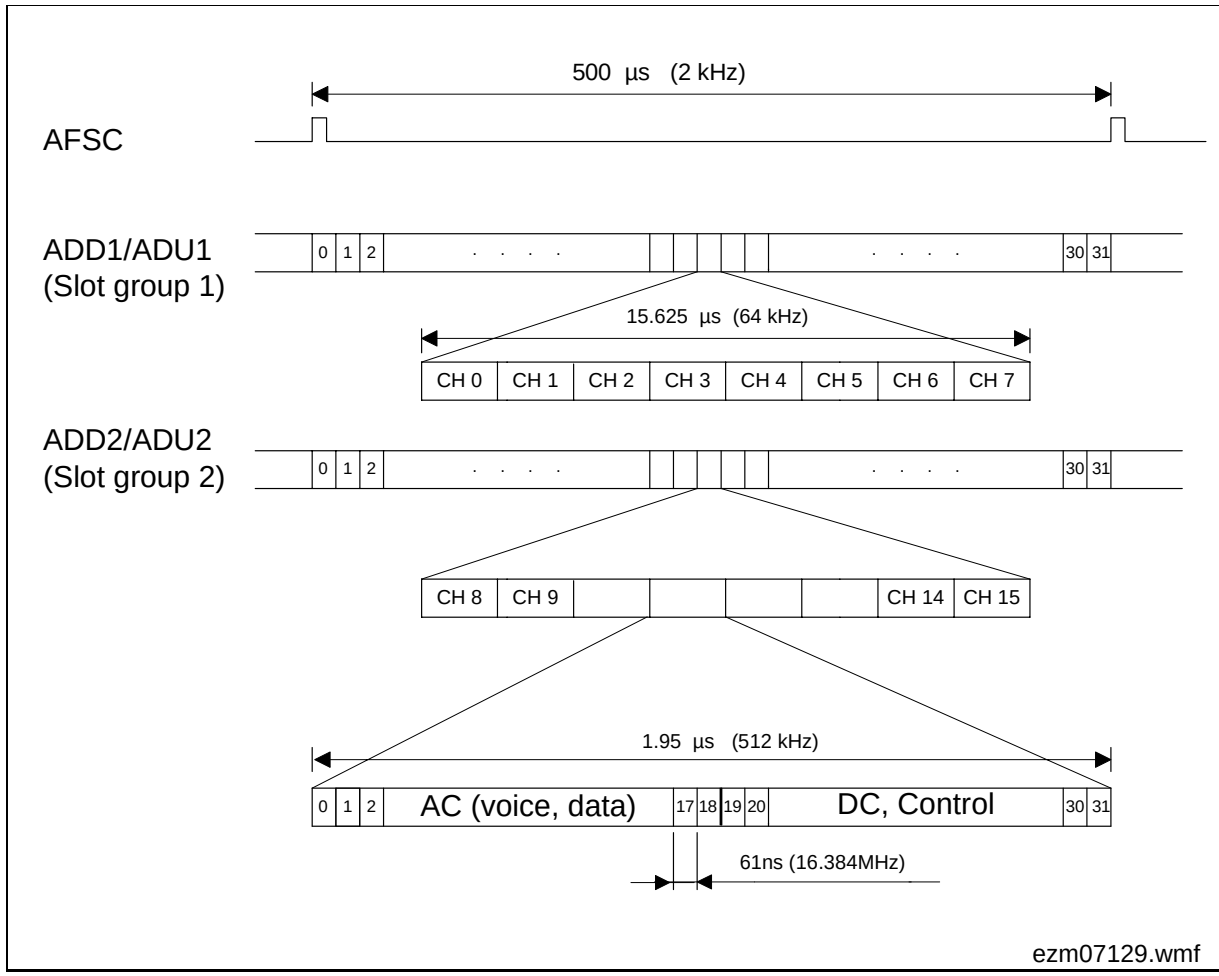


Figure 13 MuPP µC / QAP Interface: Frame, Bit Structure

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{DD} referred to GND		– 0.3	3.6	V	
V_{DD5} referred to GND		– 0.3	5.5	V	
All digital input voltages (V_{DD5} = 5 V) referred to GND = 0 V; (V_{DD} = 3.3 V)		– 0.3	5.3	V	
DC input and output current at any input or output pin (free from latch-up)			100	mA	
Storage temperature	T_{STG}	– 65	125	°C	
Ambient temperature under bias	T_A	– 45	90	°C	
Package power dissipation	P_D		1	W	

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional operation under these conditions is not implied. Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may effect device reliability.

4.2 Operating Range

T_A = – 40 to 85 °C; V_{DD} = 3.3 V ± 5%; V_{GND} = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power supply current			115	125	mA	V_{DD} = 3.3 V
Power dissipation (all channels active			380	410	mW	V_{DD} = 3.3 V
Power dissipation (only 1 channel active)			165	198	mW	V_{DD} = 3.3 V
Power dissipation (no channel active)			148	180	mW	V_{DD} = 3.3 V

Note: In the operating range the functions given in the circuit description are fulfilled.

4.3 Digital Interface

T_A = – 40 to 85 °C; V_{DD} = 3.3 V ± 5%; V_{GND} = 0 V

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
For all input pins					
Input low-voltage	V_{IL}		0.8	V	TTL Level
Input high-voltage	V_{IH}	2.0		V	
Input leakage current	I_{IL}	– 1	1	µA	$-0.3 \le V_{in} \le V_{DD5}$
Spike rejection for RESET	t_{rej}	50	200	ns	
For all output pins					
Set-up time	t_s		typ. 30	ns	Load capacitance 30 pF
Output low-voltage	V_{OL}		0.45	V	I_{OL} = – 3.2 mA
Output high-voltage	V_{OH}	0.7*V_{DD}		V	I_{OH} = 2 mA

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

4.3.1 µC-Interface Timing Characteristics

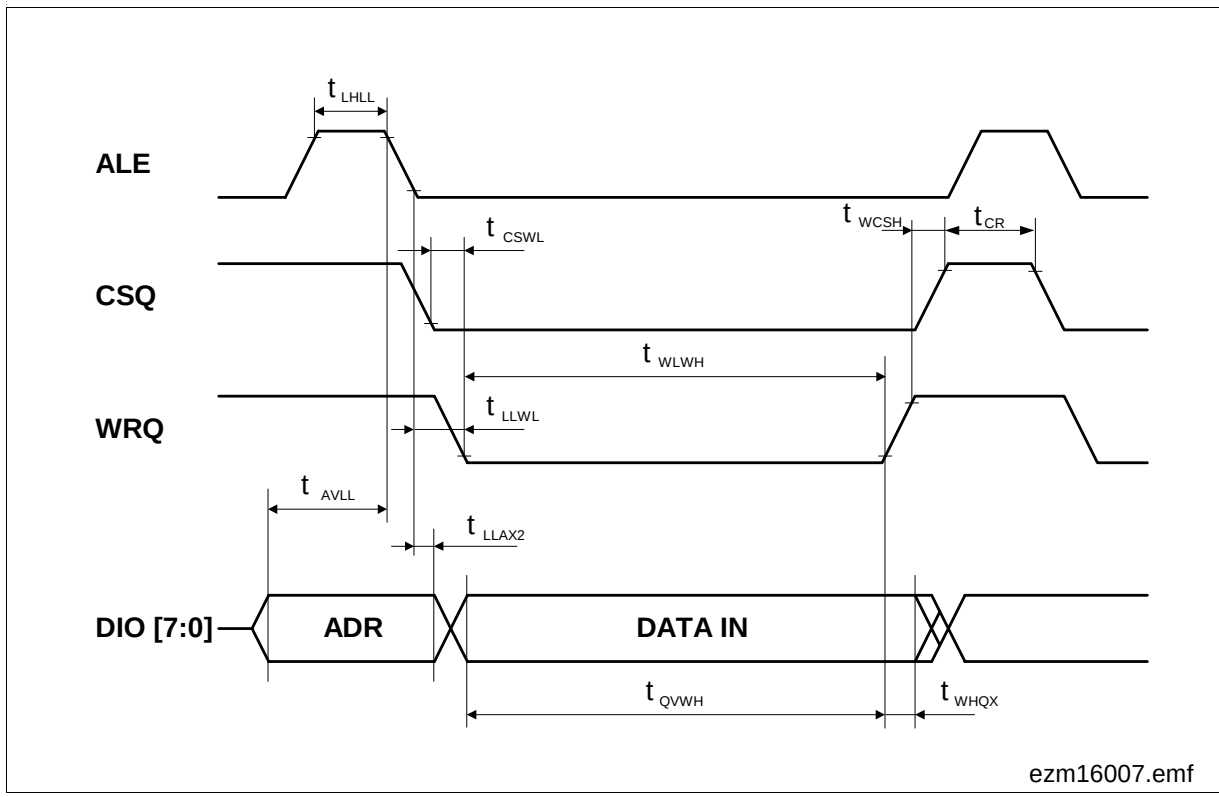


Figure 14 Write Access to the µC-Interface INTEL MUX Mode

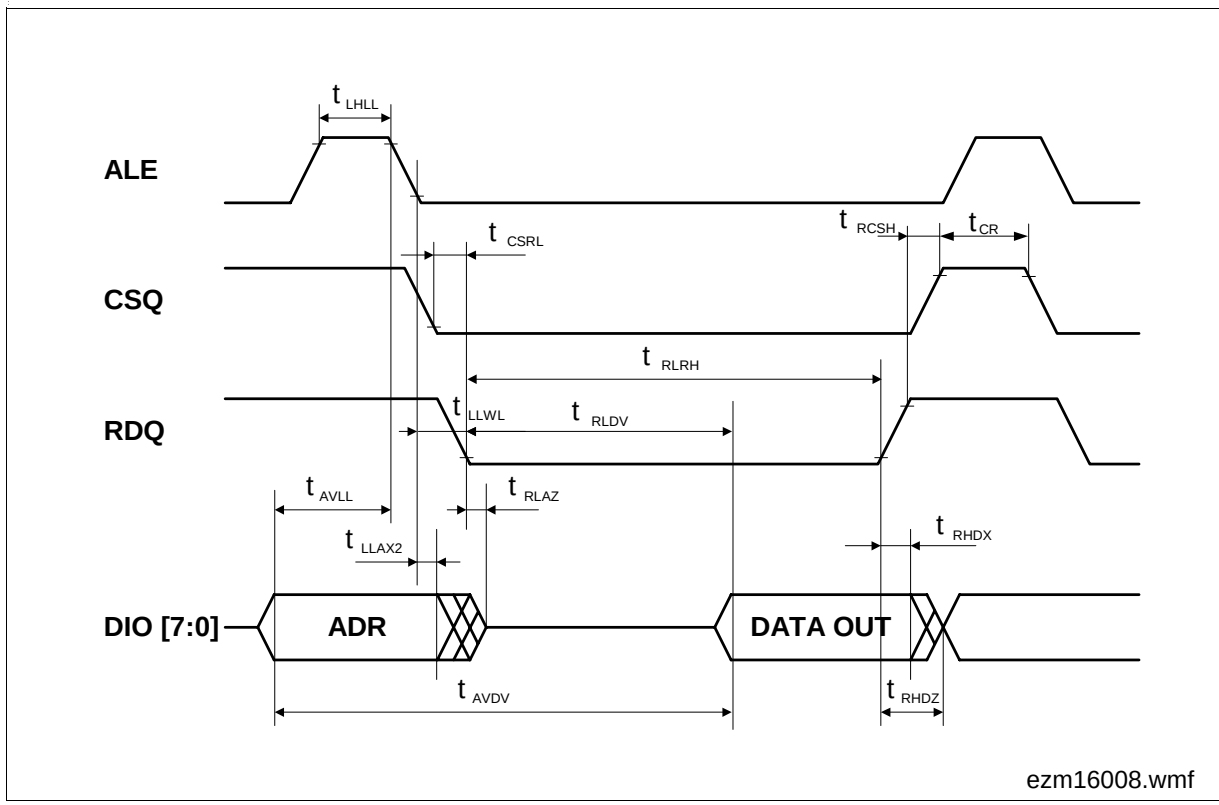


Figure 15 Read Access to the µC-Interface INTEL MUX Mode

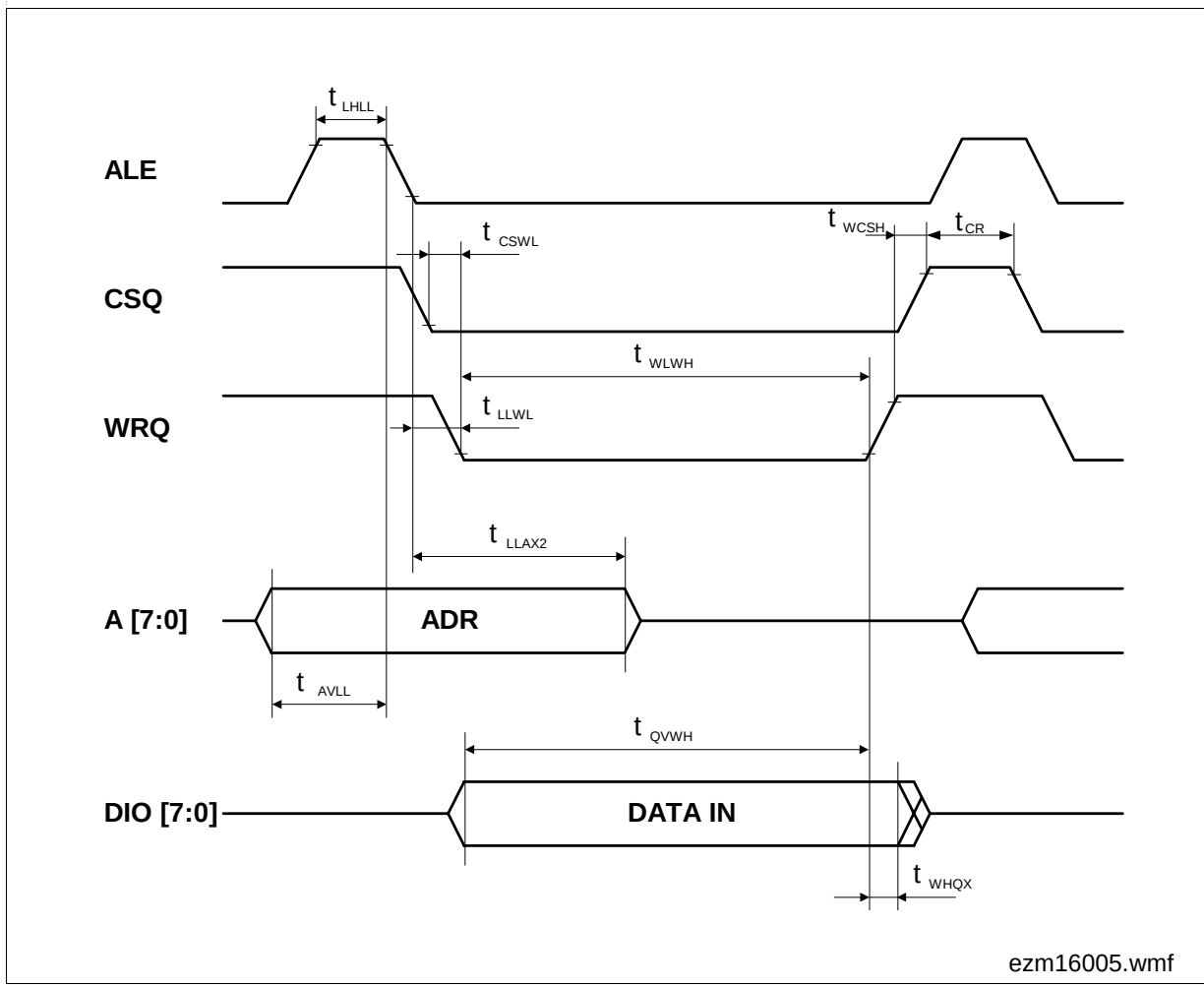


Figure 16 Write Access to the µC-Interface INTEL DEMUX Mode

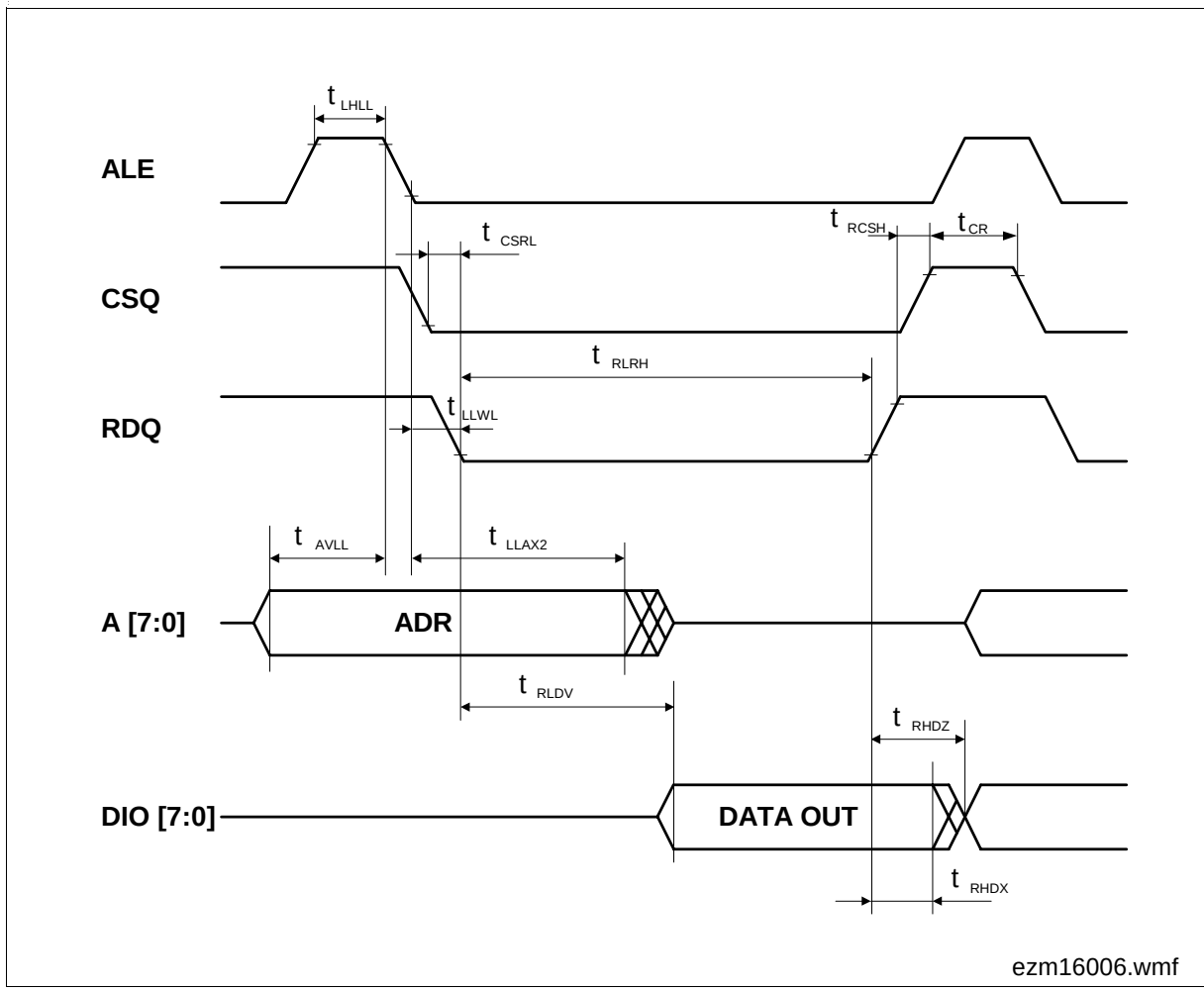


Figure 17 Read Access to the µC-Interface INTEL DEMUX Mode

Table 6 Timing Specifications µC-Interface INTEL MUX/DEMUX Modes

Parameter	Symbol	LimitValues		Unit
		min.	max.	
RD pulse width	t_{RLRH}	75		ns
WR pulse width	t_{WLWH}	75		ns
Address hold after ALE inactive	t_{LLAX2}	10		ns
RD active to valid data out	t_{RLDV}		70	ns
Data hold after RD inactive	t_{RHDX}	5		ns
Data float after RD inactive	t_{RHDZ}		30	ns
Address valid to valid data out	t_{AVDV}		100	ns
ALE to WR or RD active	t_{LLWL}	20		ns
ALE high time	t_{LHLL}	20		ns
Address setup to ALE	t_{AVLL}	10		ns
Data setup before WR inactive	t_{QVWH}	20		ns
Data hold after WR inactive	t_{WHQX}	5		ns
Address float after RD active	t_{RLAZ}		20	ns
CS low to WR low[1)]	t_{CSWL}	0		ns
CS low to RD low[1)]	t_{CSRL}	0		ns
WR high to CS high[1)]	t_{WCSH}	0		ns
RD high to CS high[1)]	t_{RCSH}	0		ns
Command recovery time	t_{CR}	200		ns
An increased command recovery time applies to the following commands:				
Any access to data port (adr. 7)	t_{CR}	2		µs
Broadcast	t_{CR}	8		µs
AC Checksum Generation	t_{CR}	60		µs
DC Checksum Generation	t_{CR}	25		µs
Init CRAM	t_{CR}	80		µs
ECIC Read	t_{CR}	250		µs

1) These parameters are for reference only. A valid access to MuPP is determined by CSQ and RDQ (WRQ) active. If the duration of CSQ is shorter than RDQ (WRQ) or vice verse, care must be taken, that the parameters for RDQ or WRQ width (t_{RLRH} or t_{WLWH}) and data access (t_{RLDV}, t_{RHDX} for read and t_{QVWH}, t_{WHQX} for write) still apply to the shorter one of the two signals CSQ or RDQ (WRQ).

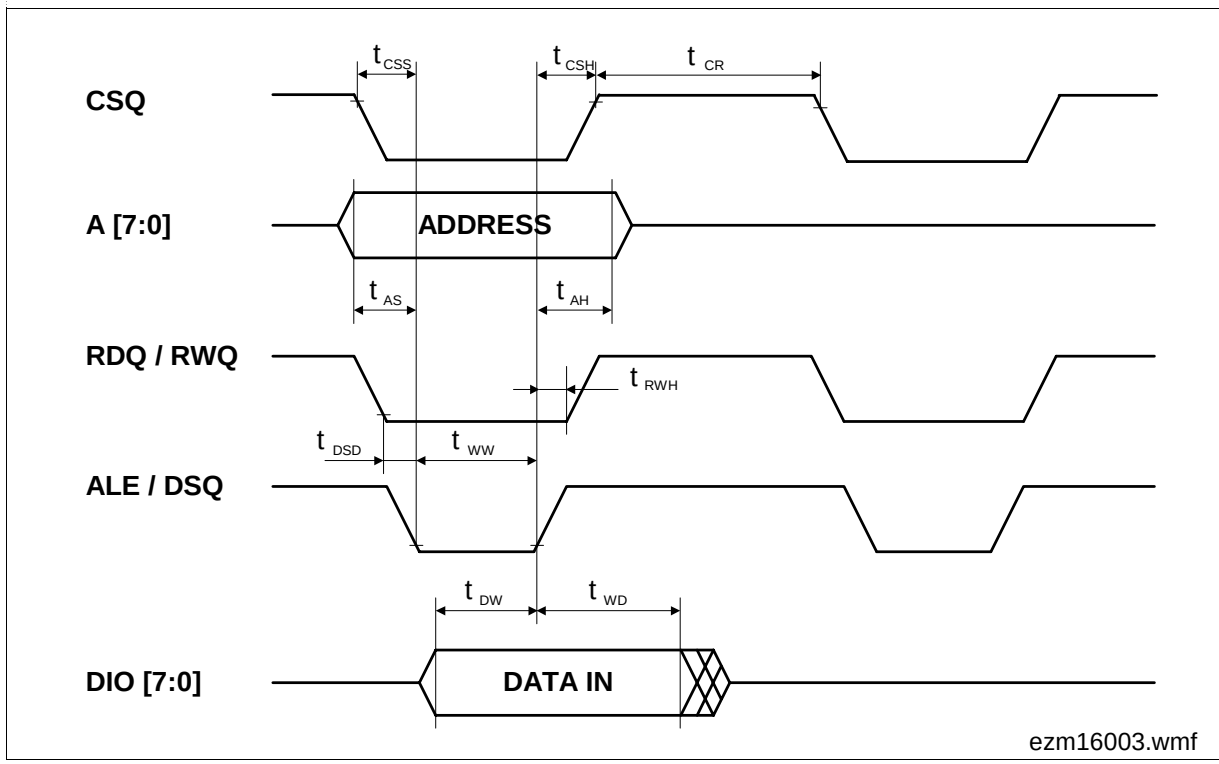


Figure 18 Write Access to the µC-Interface Motorola Mode

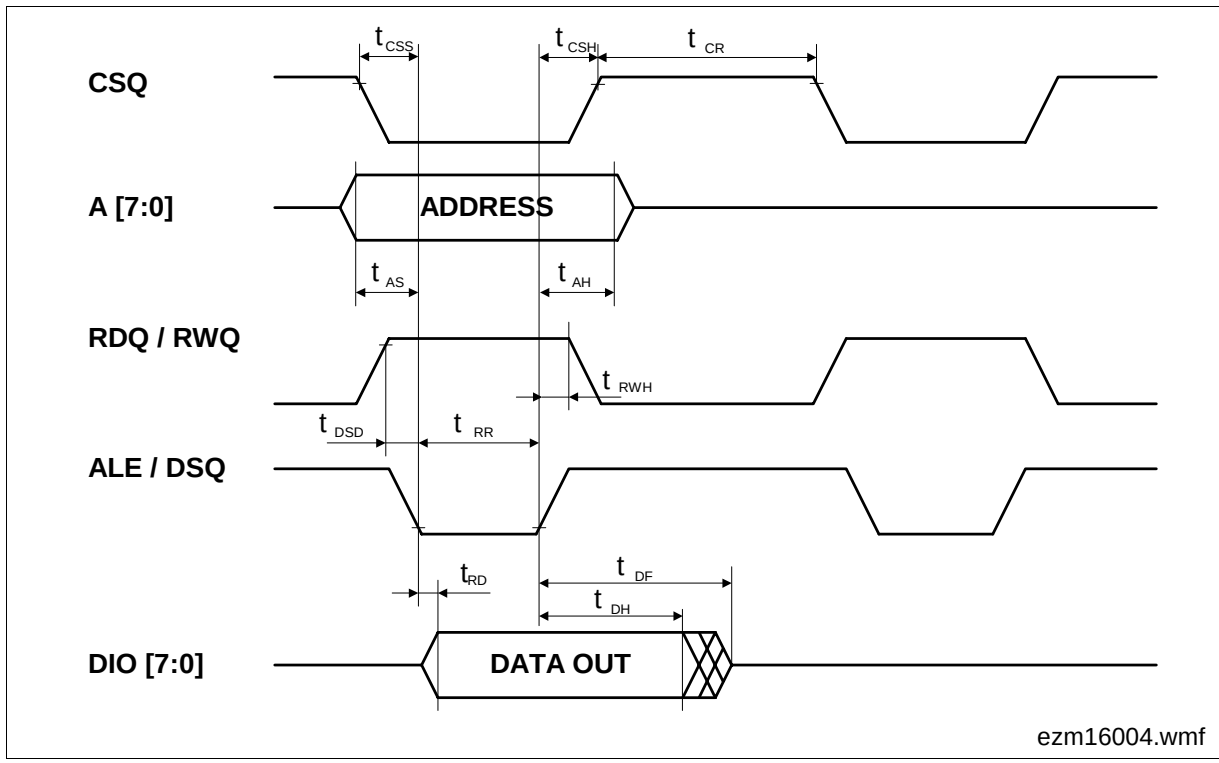


Figure 19 Read Access to the µC-Interface Motorola Mode

Table 7 Timing Specifications for the µC-Interface Motorola Mode

Parameter	Symbol	LimitValues		Unit
		min.	max.	
RDQ/RWQ setup to DSQ active	t_{DSD}	0		ns
DSQ pulse width (read)	t_{RR}	70		ns
Data output delay from DSQ active (read)	t_{RD}		50	ns
Data hold from DSQ inactive (read)	t_{DH}	5		ns
Data float delay from DSQ inactive (read)	t_{DF}		30	ns
DSQ pulse width (write)	t_{WW}	60		ns
Data setup time	t_{DW}	25		ns
Data hold time	t_{WD}	7		ns
Address setup time	t_{AS}	10		ns
Address hold time	t_{AH}	7		ns
Chip select setup time[1)]	t_{CSS}	0		ns
Chip select hold time[1)]	t_{CSH}	0		ns
RDQ/RWQ hold after DSQ inactive	t_{RWH}	0		ns
Command recovery time	t_{CR}	200		ns
An increased command recovery time applies to the following commands:				
Any access to data port (adr. 7)	t_{CR}	2		µs
Broadcast	t_{CR}	8		µs
AC Checksum Generation	t_{CR}	60		µs
DC Checksum Generation	t_{CR}	25		µs
Init CRAM	t_{CR}	80		µs
ECIC Read	t_{CR}	250		µs

1) These parameters are for reference only. A valid access to MuPP is determined by CSQ and DSQ active. If the duration of CSQ is shorter than DSQ or vice verse, care must be taken, that the parameters for DSQ width (t_{RR} for read and t_{WW} for write) and data access (t_{RD}, t_{DH} for read and t_{DW}, t_{WD} for write) still apply to the shorter one of the two signals CSQ or DSQ.

4.3.2 QAP-Interface Timing Characteristics

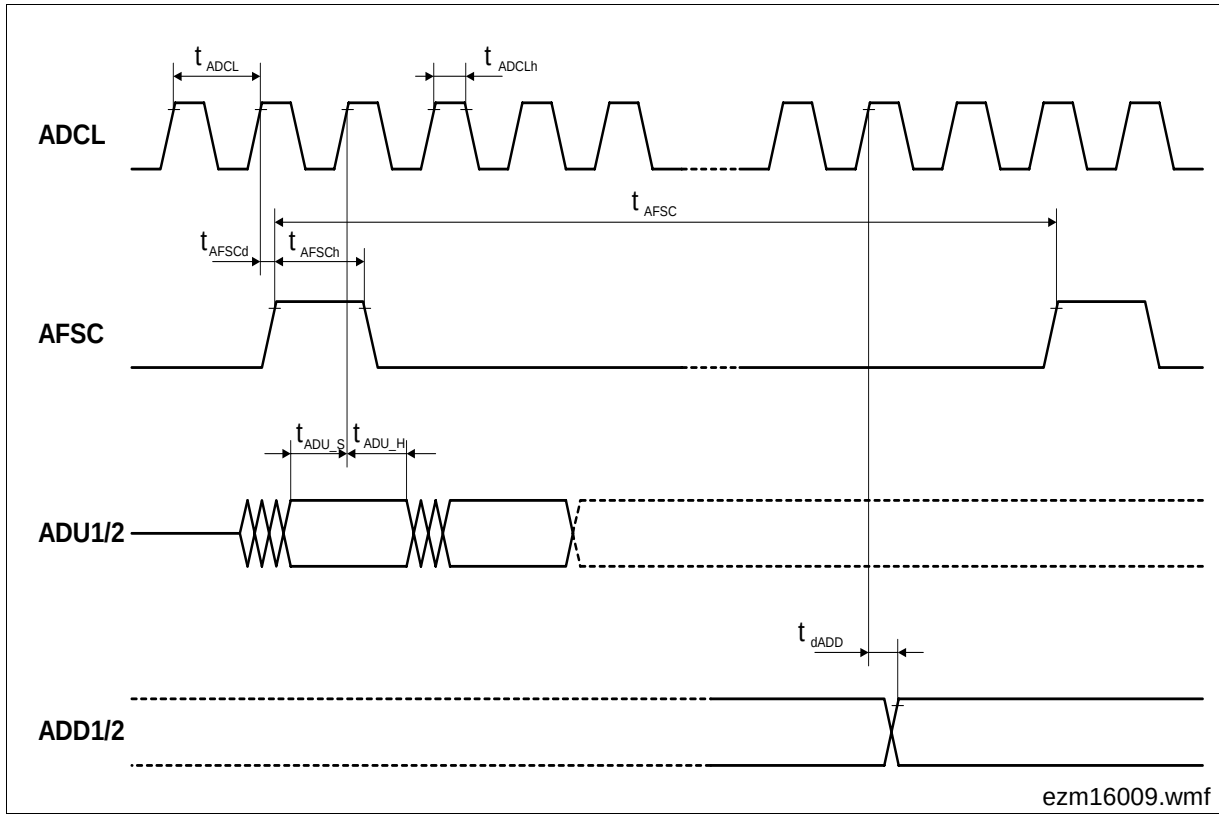


Figure 20 QAP-Interface Timing Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period ADCL	t_{ADCL}		1/16384		ms
ADCL duty cycle	t_{ADCLh}	40	50	60	%
Period AFSC	t_{AFSC}		500		µs
AFSC delay	t_{AFSCd}		5	20	ns
AFSC high	t_{AFSCh}		t_{DCL}		ns
ADU1/2 setup time	$t_{ADU\ S}$	20			ns
ADU1/2 hold time	$t_{ADU\ H}$	20			ns
ADD1/2 delay	t_{dADD}			20	ns

4.3.3 External ASIC Interface Timing Characteristics

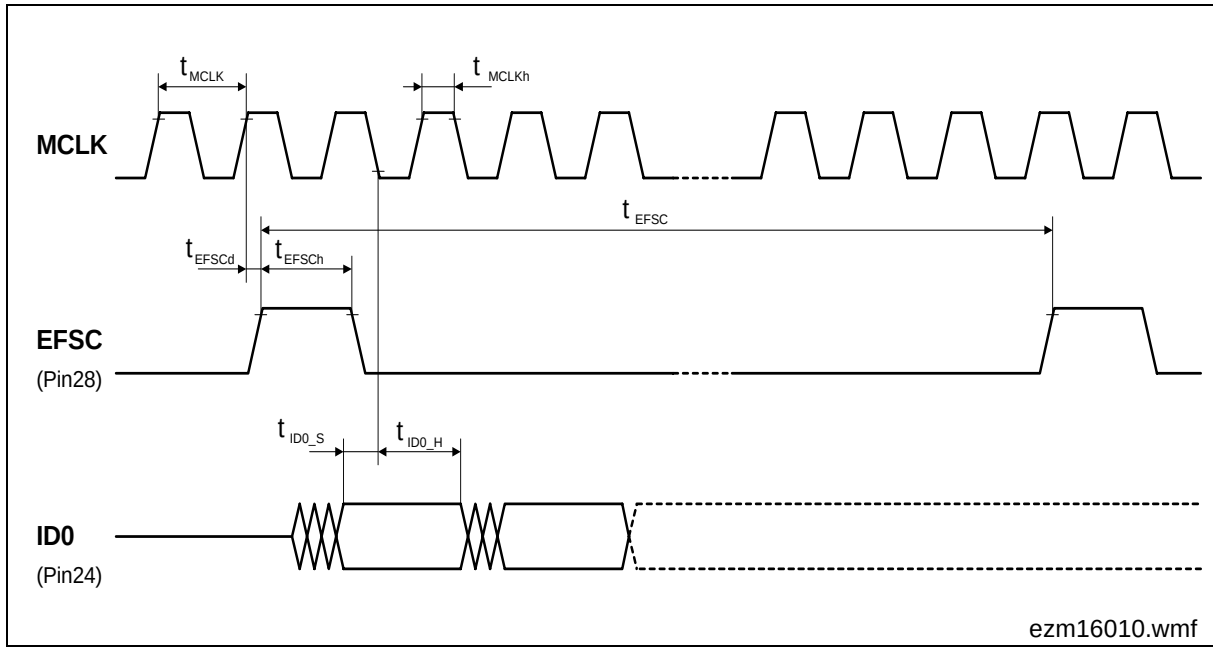


Figure 21 External ASIC Interface Timing Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period MCLK	t_{MCLK}		1/4096		ms
MCLK duty cycle	t_{MCLKh}	40	50	60	%
Period EFSC	t_{EFSC}		125		µs
EFSC delay	t_{EFSCd}		5	20	ns
EFSC high	t_{EFSCh}		t_{MCLK}		ns
ID0 setup time	$t_{ID0\ S}$		20		ns
ID0 hold time	$t_{ID0\ H}$		20		ns

4.3.4 PCM-Interface Timing

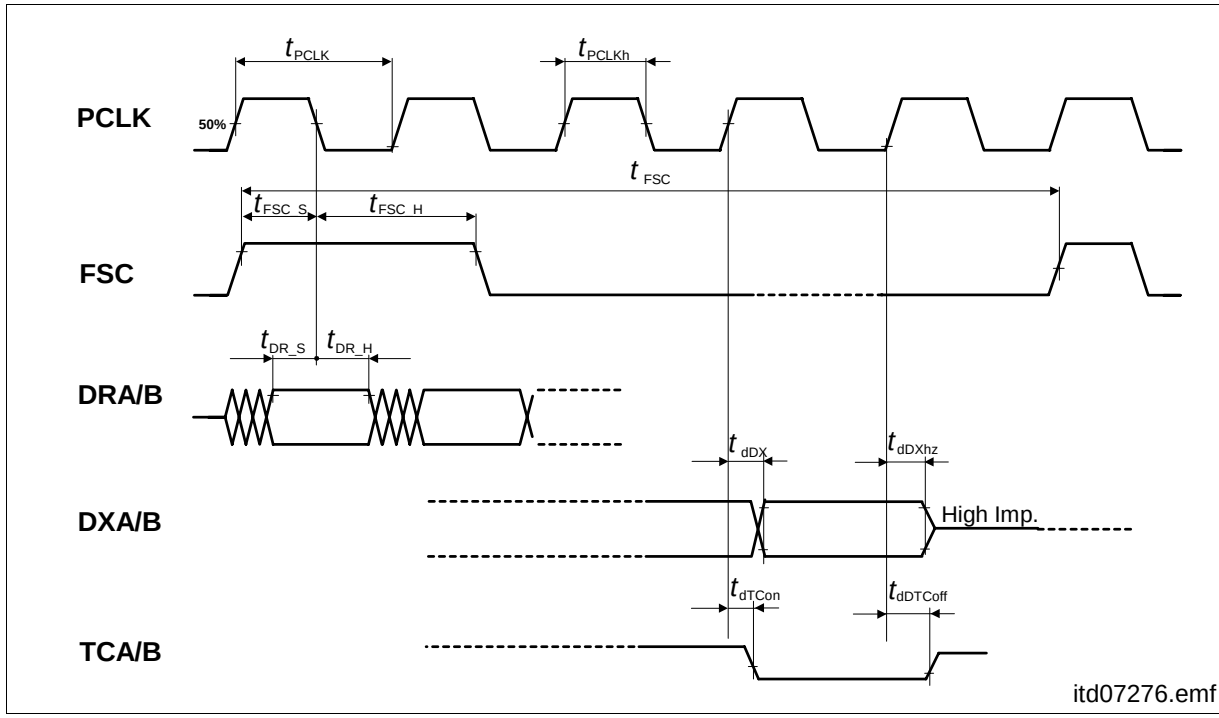


Figure 22 PCM-Interface Timing Single Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of PCLK	t_{PCLK}	1/8192		1/512	ms
PCLK high time	t_{PCLKh}		$t_{PCLK/2}$		µs
Period FSC	t_{FSC}		125		µs
FSC setup time	t_{FSC_s}	10	50		ns
FSC hold time	t_{FSC_h}	$(t_{PCLK} - t_{PCLKh})$ + 10	$(t_{PCLK} - t_{PCLKh})$ + 50		ns
DRA/B setup time	t_{DR_s}	10	50		ns
DRA/B hold time	t_{DR_h}	10	50		ns
DXA/B delay time [1]	t_{dDX}	25	50 (@ 200 pF)		ns
DXA/B delay time to high Z	t_{dDXhz}	25	50		ns
TCA/B delay time on	t_{dTCon}	25	50		ns
TCA/B delay time off	t_{dTCoff}	25	100		ns

[1] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C-load)

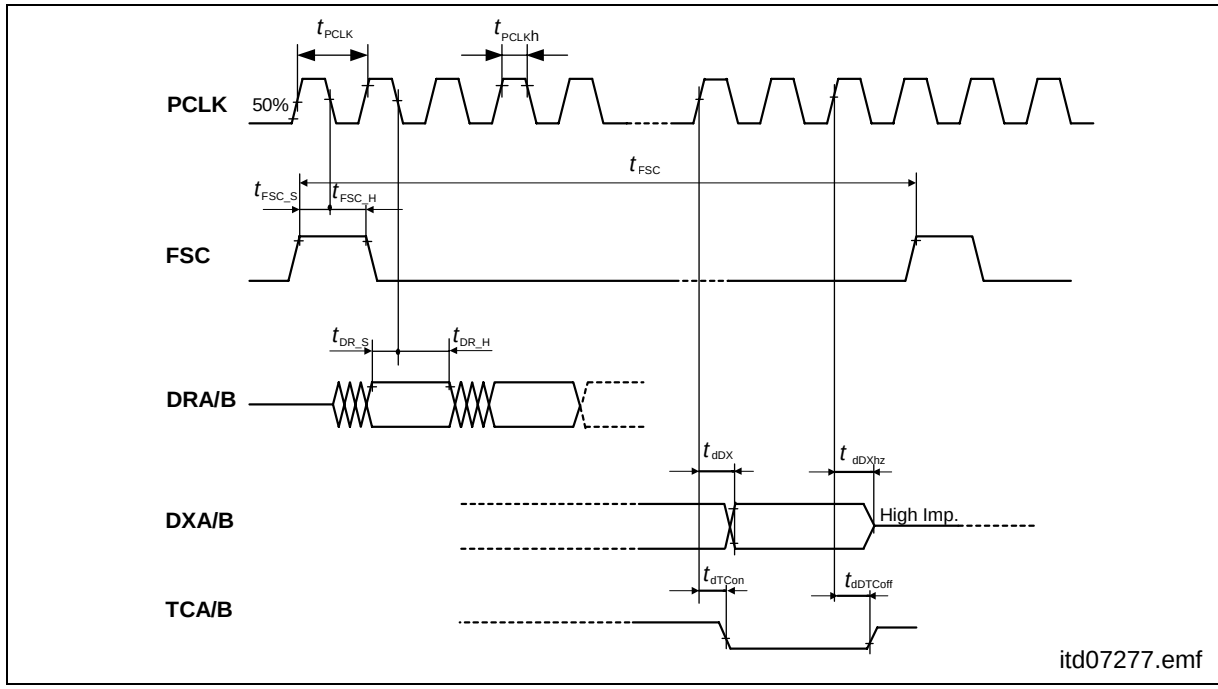


Figure 23 PCM-Interface Timing Double Clocking Mode

sd

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of PCLK	t_{PCLK}	1/8192		1/512	ms
PCLK high time	t_{PCLKh}		$t_{PCLK/2}$		µs
Period FSC	t_{FSC}		125		µs
FSC setup time	t_{FSC_s}	10	50		ns
FSC hold time	t_{FSC_h}	2 x ($t_{PCLK} - t_{PCLKh}$) + 10	2 x ($t_{PCLK} - t_{PCLKh}$) + 50		ns
DRA/B setup time	t_{DR_s}	10	50		ns
DRA/B hold time	t_{DR_h}	10	50		ns
DXA/B delay time [1)]	t_{dDX}	25	50 (@200 pF)		ns
DXA/B delay time to high Z	t_{dDXhz}	25	50		ns
TCA/B delay time on	t_{dTCon}	25	50		ns
TCA/B delay time off	t_{dTCoff}	25	100		ns

1) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C-load)

4.3.5 MCLK - FSC Timing Relationship

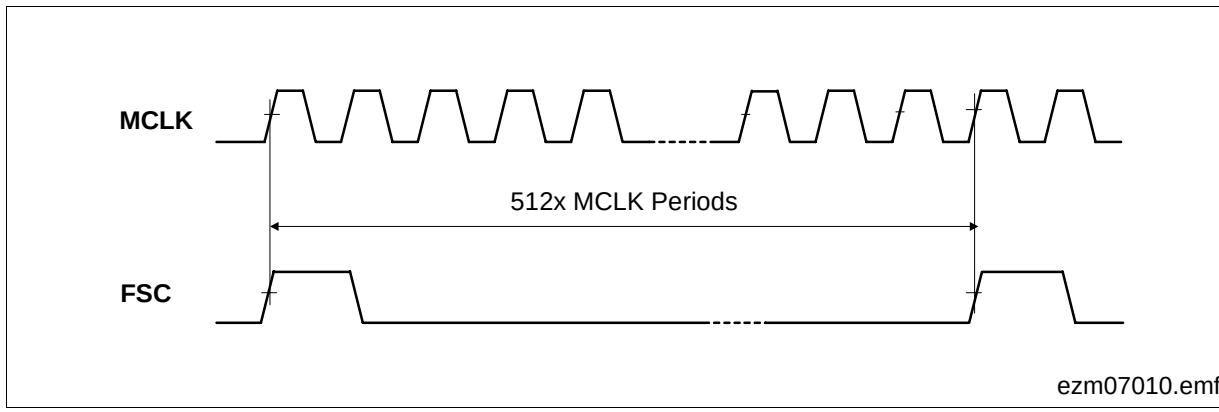
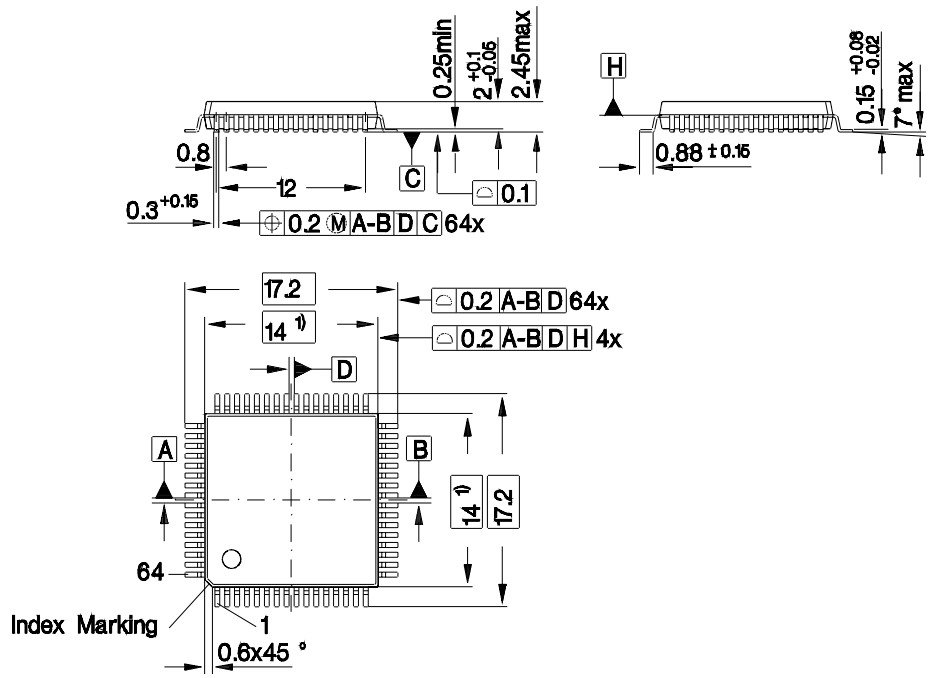


Figure 24 MCLK - FSC Timing Relationship

In order to keep internal synchronization, the number of MCLK periods within 2 FSCs must be kept constant, equal to 512 periods. This means that there must be a fixed phase relationship between FSC and MCLK.

5 Package Outlines

P-MQFP-64-1
(Plastic Metric Quad Flat Package)



gpm05250.eps

Figure 25 Package Outline: PEB 31664 / PEB 31666 (MuPP µC)

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our data book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

6 Glossary

AGR	Attenuation Receive
AGX	Attenuation Transmit
AHV-SLIC	Advanced High Voltage Subscriber Line Interface Circuit
ASIC	Application Specific Integrated Circuit
BiCMOS	Bipolar Complementary Metal Oxid Semiconductor
C1, 2	Digital Interface between QAP and AHV-SLIC
CMP	Compander
CODEC	Coder Decoder
COMP	Comparator (Testloops, Levelmetering)
CRAM	Coefficient RAM
DAC	Digital Analog Converter
DTAG	Deutsche Telecom AG
DCCHAR	DC Characteristic block
DCL	Data Clock
DD	Data Downstream
DSP	Digital Signal Processor
DU	Data Upstream
EXP	Expander
FRR	Frequency Response Receive Filter
FRX	Frequency Response Transmit Filter
FSC	Frame Sync.
GNK	Ground Key
I1	Fixed Input Pin
IL	Longitudinal Current Input
IO	User Programmable I/O Pin
IT	Transversal Current Input (for AC and DC)
ITAC	Transversal Current Input (for AC)
LSSGR	Local area transport access Switching System Generic Requirements

MuPP µC	Multi Channel Processor for POTS
MuSLIC	Multi Channel Subscriber Line Interface Circuit
MuSLICOS	MuSLIC Oriented Software
O1	Fixed Output Pin
PCM	Pulse Code Modulation
POTS	Plain Old Telephone Service
QAP	Quad Analog POTS
RES	Reset
RNG	Ring Generator
SLIC	Subscriber Line Interface Circuit
SOP	Status Operation
TST1	Test Pin
TH	Transhybrid Balancing
THFIX	Transhybrid Balancing Filter (fixed)
TOP	Transfer Operation
TTX	Teletax
X	Transmit Filter (programmable)

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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Dr. Ulrich Schumacher

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