

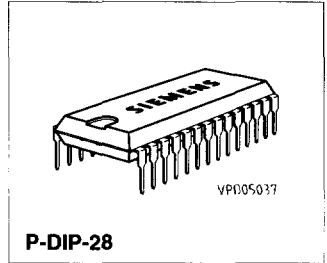
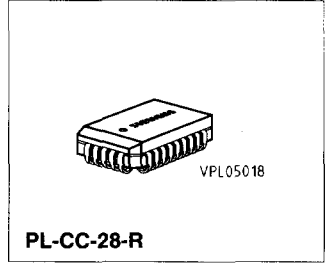
ISDN Primary Access Transceiver (IPAT®-2)

PEB 2236

CMOS IC

Features

- ISDN line interface for 1544 and 2048 kbit/s (T1 and CEPT)
- Data and clock recovery
- Transparent to ternary codes
- Low transmitter output impedance for a high return loss with reasonable protection resistors
(CCITT G.703 requirements for the line input return loss fulfilled)
- Adaptively controlled receiver threshold
- Programmable pulse shape for T1 applications
- Jitter specifications of CCITT I.431 and many AT&T / BELLCORE publications met
- Jitter tolerance of receiver: 0.43 UI s
- Implements local and remote loops for diagnostic purposes
- Monolithic line driver for a minimum of external components
- Low power, reliable CMOS technology
- Loss of signal indication for receiver and transmitter
- Power-on reset



Type	Version	Ordering Code	Package
PEB 2236-N	V2.1	Q67100-H6239	P-LCC-28-R (SMD)
PEB 2236-P	V2.1	Q67100-H6240	P-DIP-28

The ISDN Primary Access Transceiver IPAT[®]-2 (PEB 2236) is a monolithic CMOS device which implements the analog receive and transmit line interface functions to primary rate PCM carriers. It may be programmed or hard wired to operate in 1.544-Mbit/s (T1) or 2.048-Mbit/s (CEPT) carrier systems.

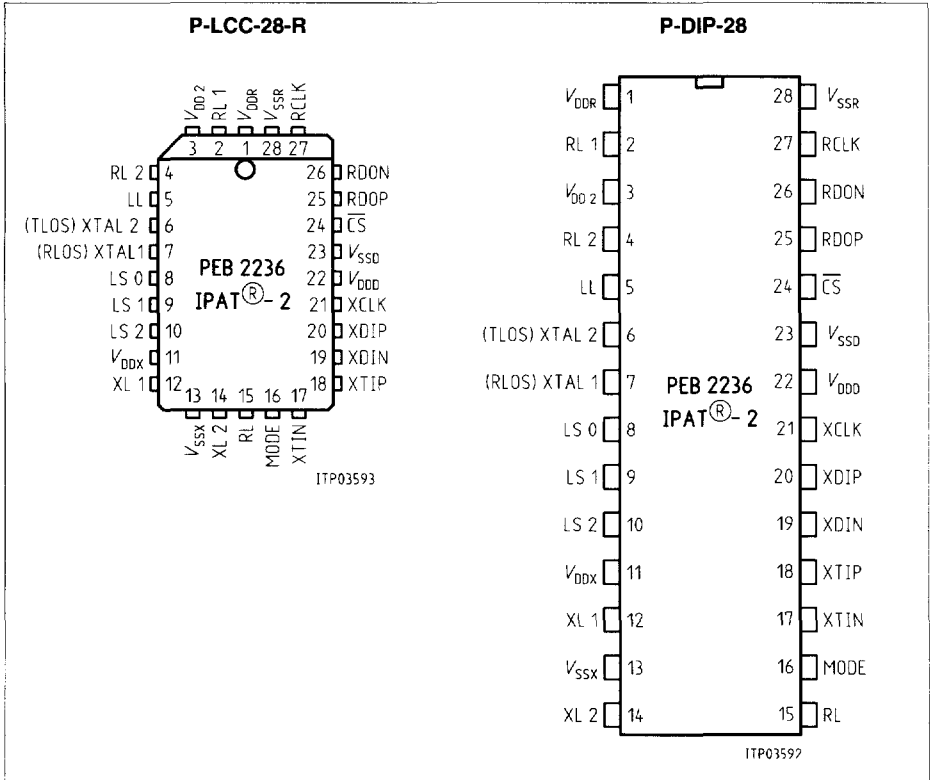
The IPAT-2 recovers clock and data using an adaptively controlled receiver threshold. It is transparent to ternary codes and shapes the output pulse following the AT&T Technical Advisory #34 or CCITT G.703. The jitter tolerance of the device meets the CCITT (I.431) recommendation and many other specifications by AT&T/BELLCORE. Diagnostic facilities are included.

Specially designed line interface circuits simplify the tedious task of protecting the device against overvoltage damage while still meeting the return loss requirements.

The IPAT-2 is suitable for use in a wide range of voice and data applications such as for connections of digital switches and PABX's to host computers, for implementations of primary ISDN subscriber loops as well as for terminal applications. The maximum range is determined by the maximum allowable attenuation.

In the T1 case the IPAT's power consumption is mainly determined by the line length and type of the cable.

Pin Configuration (top view)



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
1	V_{DDR}	I	Positive power supply for the receive subcircuits
2	RL1	I	Line receiver pin 1
3	V_{DD2}	O	Reference voltage output for tapping the input transformer
4	RL2	I	Line receiver pin 2
5	LL	I	Local loopback: A high level selects the device for the local loopback mode
6	XTAL2 /TLOS	I/O	Connecting the MODE pin to V_{DD} or the MODE pin is not connected these pins function as an input
7	XTAL1 /RLOS	I/O	Reference clock inputs: A 24704- or 32768-kHz crystal reference should be connected to these pins for T1 or CEPT applications, respectively. It is also possible to connect an external precision clock to XTAL1 leaving XTAL2 unconnected. The external reference must be provided at full CMOS levels. ----- Connecting the MODE pin to V_{SS} these pins function as an output. Transmitter loss of signal, active low Receiver loss of signal, active low
8	LS0	I	Line length select: determine to what extent the line output signals are preshaped prior to transmission
9	LS1	I	
10	LS2	I	
11	V_{DDX}	I	Positive power supply for transmit subcircuits
12	XL1	O	Line transmitter pin 1
13	V_{SSX}	I	Ground for transmit subcircuits
14	XL2	O	Line transmitter pin 2
15	RL	I	Remote loopback: A high level puts the device to the remote loopback mode
16	MODE	I	If the MODE pin is not connected or connected to V_{DD} a 24704- or 32768-kHz crystal reference should be connected to pin 6 and 7. If the MODE pin is connected to V_{SS} the pins 6 and 7 are outputs for TLOS and RLOS.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
17	XTIN	I	Positive and negative transmit test data inputs, active low, half or fully banded
18	XTIP	I	
19	XDIN	I	Positive and negative transmit data inputs, active low, half or fully banded
20	XDIP	I	
21	XCLK	I	Transmit Clock
22	V _{DDD}	I	Positive power supply for the digital subcircuits
23	V _{SSD}	I	Power ground supply for the digital subcircuits
24	\overline{CS}	I	Chip Select: A low level selects the PEB 2236 for a register write operation
25	RDOP	O	Receive data output positive and negative, fully banded, active low
26	RDON	O	
27	RCLK	O	Receive clock
28	V _{SSR}	I	Power ground supply for receive subcircuits

Logic Symbol and Wiring

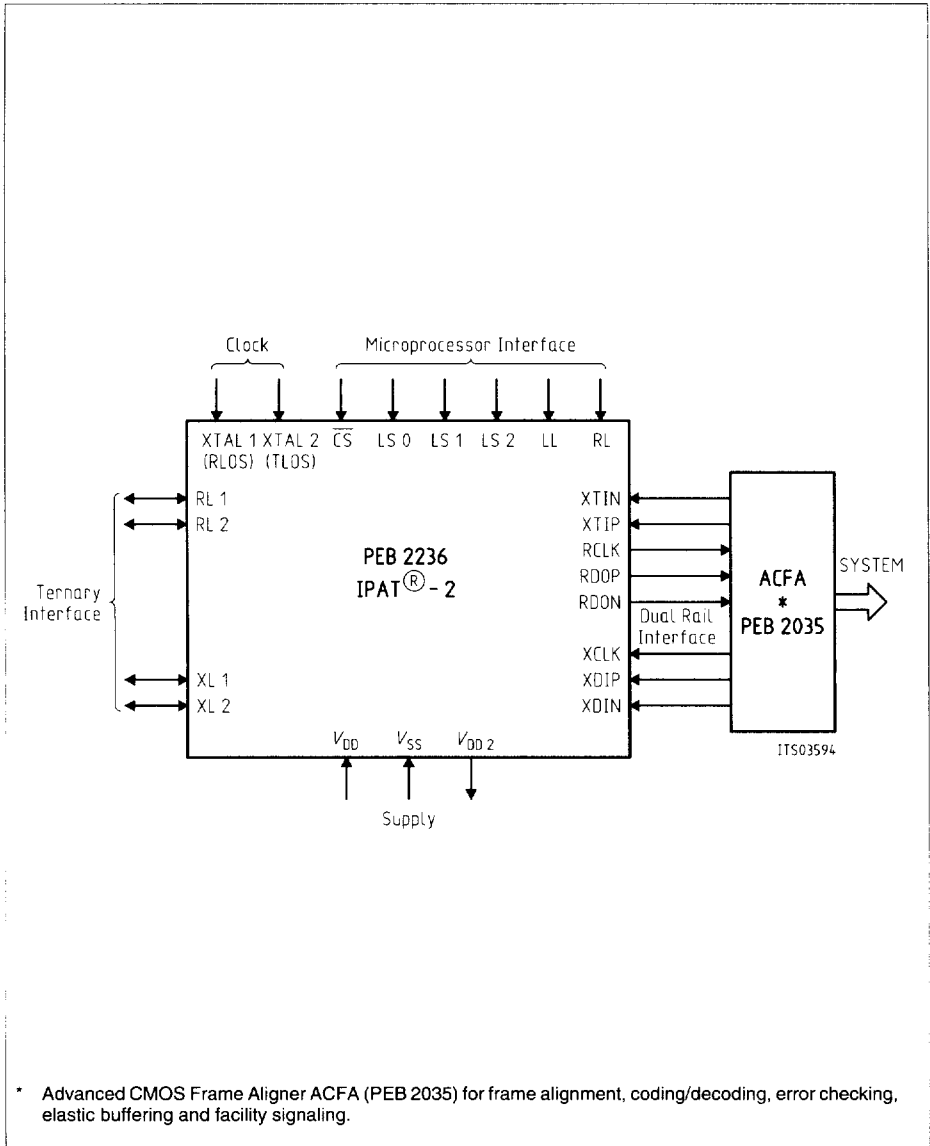


Figure 1
Logic Diagram of the IPAT[®]-2

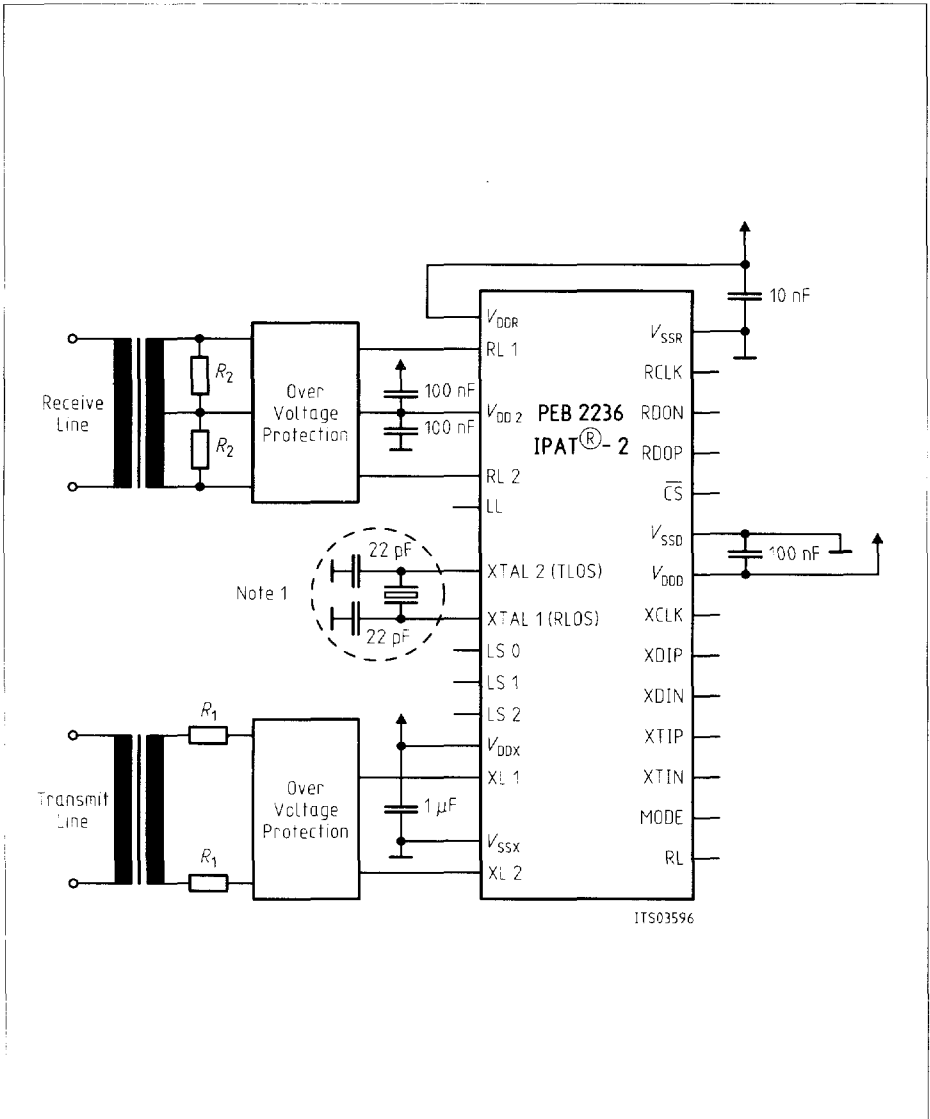


Figure 2
External Wiring of the IPAT[®]-2

Note 1: Connecting a crystal to the IPAT is optional. Switching the MODE pin to V_{SS} no crystal is required.

System Integration

Figure 3 shows the architecture of a primary access board with common channel signaling using four CMOS devices. It exhibits the following functions:

- Line Interface (PEB 2236)
- Clock and Data Recovery (PEB 2236)
- Coding/Decoding (PEB 2035)
- Framing (PEB 2035)
- Elastic Buffer (PEB 2035)
- Switch (PEB 2045)
- System Adaptation (PEB 2045)
- Data Link Signaling Handling (SAB 82525)
- μ P Interface (all devices)

Since the PEB 2045 is a switch for 256 output time slots and the SAB 82525 is actually a dual channel HDLC controller a quad primary access unit with a non-blocking switch requires a total of 11 devices,

- 4 IPAT-2 (PEB 2236)
- 4 ACFA (PEB 2035)
- 2 HSCX (SAB 82525)
- 1 MTSC (PEB 2045),

as shown in **figure 4**.

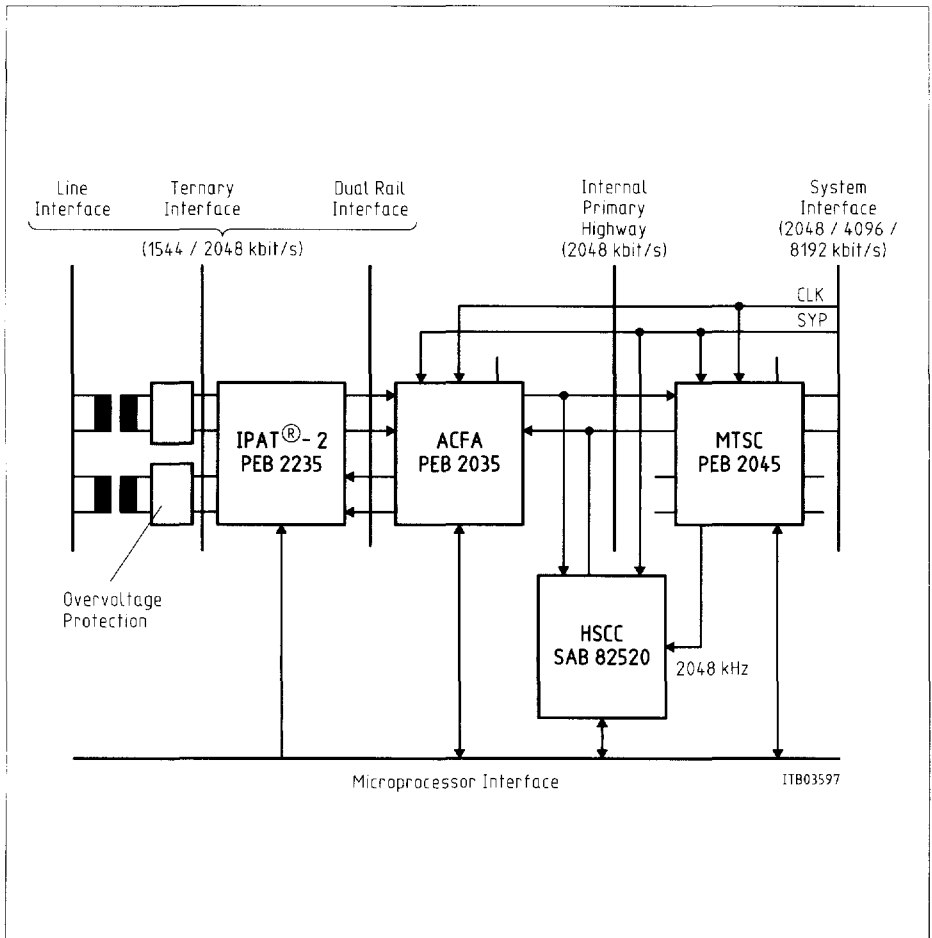


Figure 3
Architecture of a Primary Access Unit

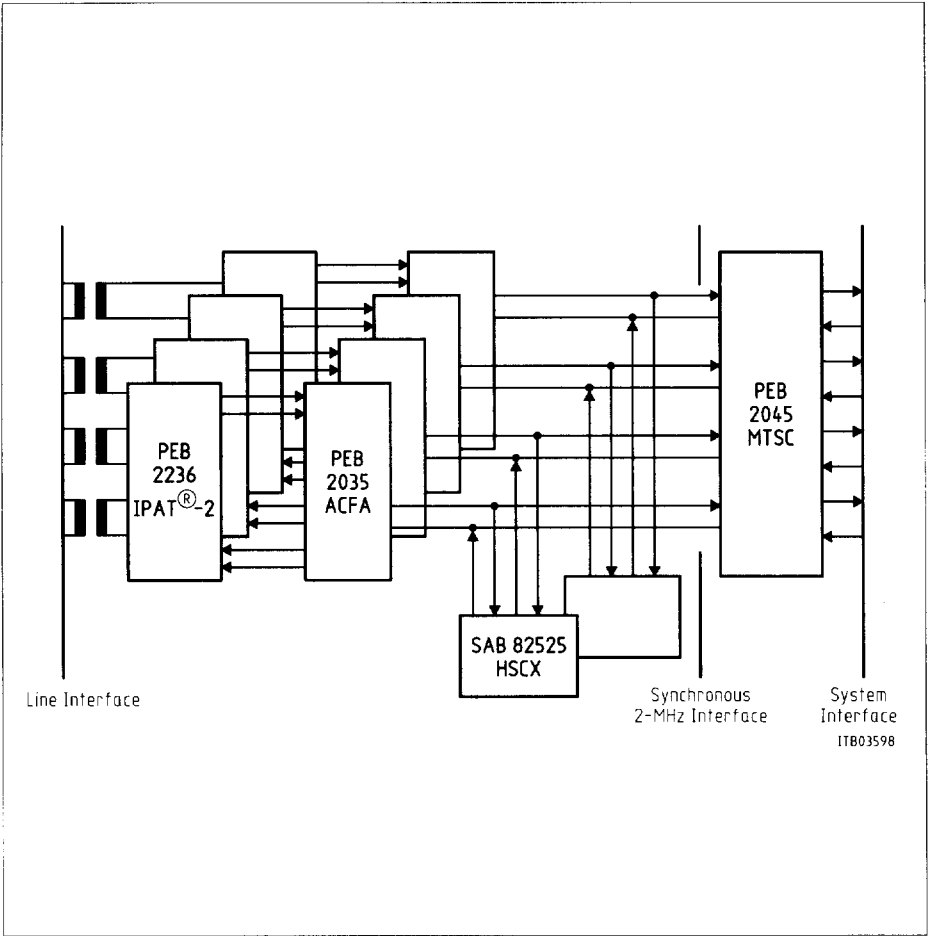


Figure 4
Quad Primary Access Unit

Functional Description

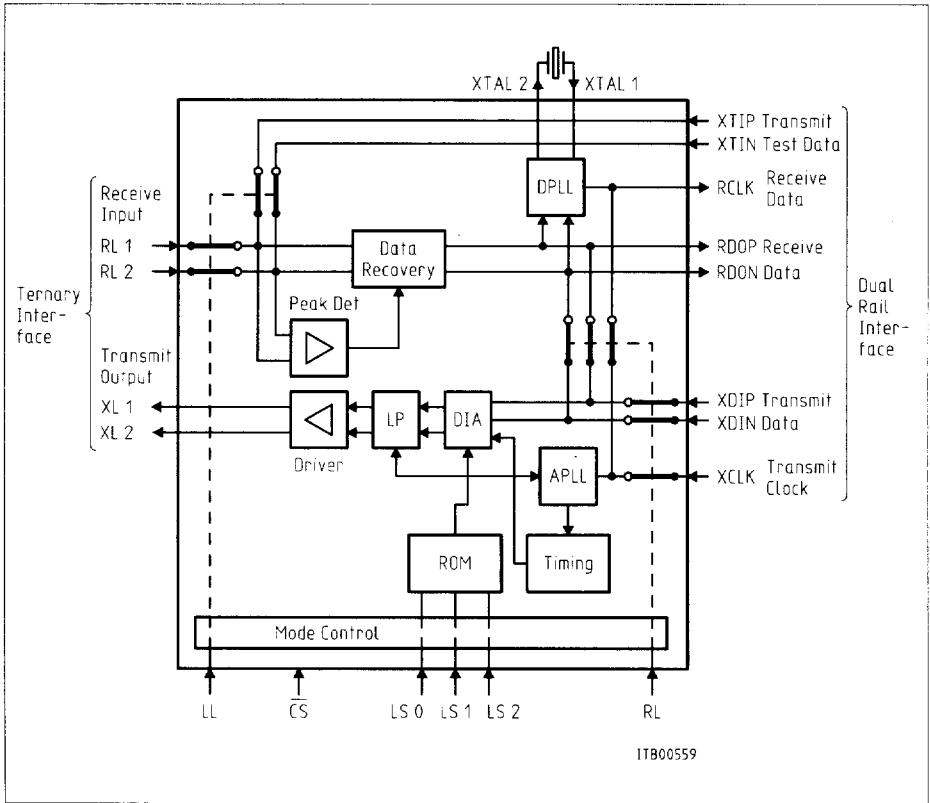


Figure 5
Functional Block Diagram of the IPAT®-2

Note: Connecting a crystal to the IPAT is optional. Switching the MODE pin to V_{SS} no crystal is required and XCLK is used as reference frequency for the receive APLL.

Receiver

Basic Functionality

The receiver recovers data from the ternary coded signal at the ternary interface and outputs it as 2 unipolar signals at the dual rail interface. One of the lines carries the positive pulses, the other the negative pulses of the ternary signal.

The signal at the ternary interface is received at both ends of a center-tapped transformer as shown in figure 6.

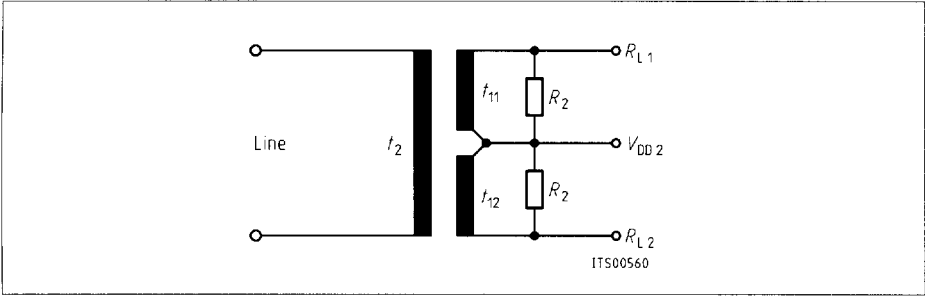


Figure 6
Receiver Configuration

The transformer is center-tapped at the IPAT-2 side. The recommended transmission factors for the different line characteristic impedances are listed in **table 1**.

Table 1
Recommended Receiver Configuration Values

Application	T1		CEPT	
Characteristic Impedances [Ω]	100	140 (ICOT)	120	75
$R_2 \pm (2.5\%)$ [Ω]	28.7	39.2	60	60
$t_2 : t_1 = t_2 : (t_{11} + t_{12})$	69 : 52 69 : (26 + 26)	69 : 52 69 : (26 + 26)	52 : 52 52 : (26 + 26)	41 : 52 41 : (26 + 26)

Wired in this way the receiver has a return loss

- $a_r > 12$ dB for $0.025 f_b \leq f \leq 0.05 f_b$,
- $a_r > 18$ dB for $0.05 f_b \leq f \leq 1.0 f_b$ and
- $a_r > 14$ dB for $1.0 f_b \leq f \leq 1.5 f_b$,

with f_b being 2048 kHz. Thus it complies with CCITT G.703.

The receiver is transparent to the logical 1's polarity and outputs positive logical 1's on RDOP and negative logical 1's on RDON. RDON and RDOP are active low and fully banded. The comparator threshold to detect logical 1's and logical 0's is automatically adjusted to be 45 % of the peak signal level.

Provided the noise is below $10 \mu V/\sqrt{Hz}$ the bit error rate will be less than 10^{-7} . The data is stable, and hence may be sampled at the falling edge of the recovered clock RCLK.

In the case of loss of signal indication and MODE pin not connected or connected to V_{DD} the receive clock RCLK is extracted from the reference clock at XTAL1 and XTAL2. In the other operating mode (MODE pin connected to V_{SS}) the receive clock is derived from the XCLK input.

PLL

An analog PLL extracts the receive clock RCLK from the data stream received at the RL1 and RL2 lines. If the MODE pin is not connected or connected to V_{DD} the PLL uses as a reference either a crystal at XTAL1 and XTAL2 or an external oscillator at XTAL1. If the MODE pin is connected to V_{SS} the PLL uses as a reference the XCLK. The IPAT-2 does not remove any jitter.

Input Jitter Tolerance

The IPAT-2 receiver's tolerance to input jitter complies to CCITT and AT&T requirements for CEPT and T1 application.

Figure 7 shows the curves of the different input jitter specifications stated above as well as the IPAT-2 performance for the various line codes used at the S1/S2 interfaces.

As can be seen in **figure 7**, the curve for the IPAT-2 at low frequencies describes a 20 dB/decade fall off, and at high frequencies are horizontal (at least 0.43 UI).

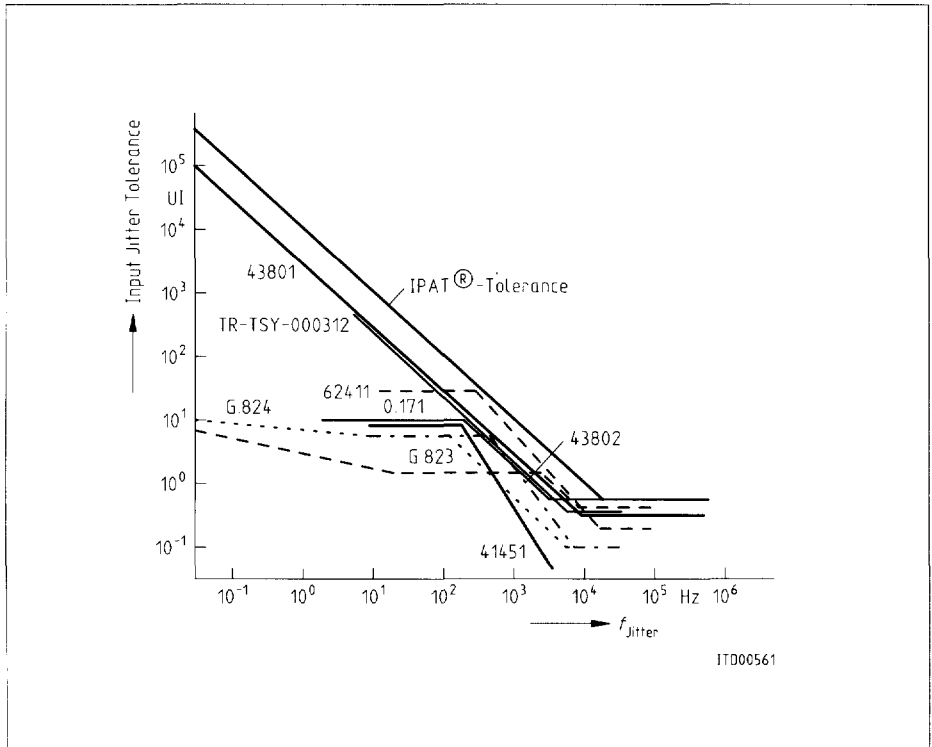


Figure 7
Comparison of Input Jitter Specification and IPAT[®]-2 Performance

Transmitter

Basic Functionality

The transmitter transforms unipolar data to ternary (alternate bipolar) return to zero signals of the appropriate shape. The unipolar data is provided at XDIP (positive pulses) and XDIN (negative pulses), synchronously with the transmit clock XCLK. XDIP and XDIN are active low and can be half or fully banded.

The transmitter includes a programmable pulse shaper to satisfy the requirements of the AT&T Technical Advisory #34 at the cross connect point for T1 applications. The pulse shaper is programmed via the line length selection pins LS0, LS1 and LS2. The pulse shape is formed using an analog PLL, which multiplies by four the transmit clock XCLK. This signal is used internally to generate the 4 segment/bit transmit pulse (CEPT: 2 segment/bit).

For T1 application the line length selection supports both low capacitance cable with a characteristic line capacitance of $C' \leq 40 \text{ nF/km} \approx 65 \text{ nF/mile}$ (e.g. MAT, ICOT) and higher capacitance cable with a characteristic line capacitance of $40 \text{ nF/km} \leq C' \leq 54 \text{ nF/km}$ ($65 \text{ nF/mile} \leq C' \leq 87 \text{ nF/mile}$) e.g. ABAM, PIC and PULP cables. This ensures that for various cable types the signal at the DSX-1 cross connect point complies with the pulse shape of the AT&T Technical Advisory #34.

The line length is selected programming the LS0, LS1 and LS2 pins as shown for typical values in **table 2**.

Table 2
Line Length Selection

LS2	LS1	LS0		PIC/PULP-Cable 24 AWG Range/m	ICOT-Cable Range/m*
0	0	0	CEPT	—	—
0	0	1	T1/G.703	0 – 50	0 – 80
0	1	0	T1	20 – 80	65 – 145
0	1	1	T1	60 – 130	130 – 210
1	0	0	T1	110 – 200	195 – 275
1	0	1	T1	140 – 230	260 – 340
1	1	0	T1	210 – 290	325 – 405
1	1	1	T1	270 – 320	390 – 470

* Note: For ICOT-cable the characteristic impedance is 140 Ω .

By selecting an all-zero code for LS0, LS1 and LS2 the IPAT-2 can be adapted for CEPT applications.

The pulse shape according to CCITT G.703 (1544-kbit/s interface) is achieved by using the same line length selection code as for the lowest T1 cable range. To switch the device into a low power dissipation mode, XDIP and XDIN should be held high.

The transmitter requires an external step up transformer to drive the line. The transmission factor and the source serial resistor values can be seen in **figure 8** and **table 3** for the various applications.

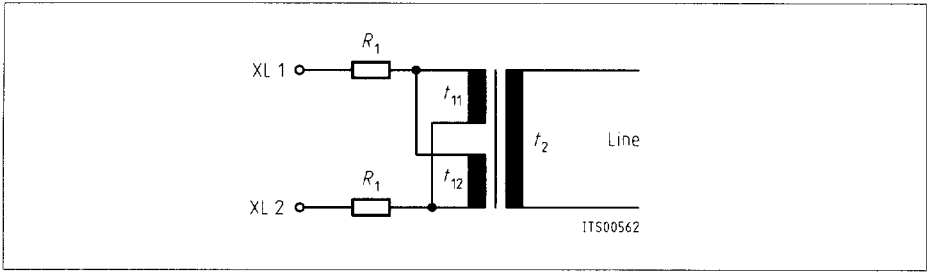


Figure 8
Transmitter Configuration

Table 3
Transmitter Configuration Values

Application	T1		CEPT	
Characteristic line impedances [Ω]	100	140 (ICOT)	120	75
$t_{11} : t_{12} = t_{12} : t_{2}$	26 : 69	26 : 69	26 : 52	26 : 41
$R_1 (\pm 2.5 \%) [\Omega]$	4.3	6	15	15

Wired in this way the transmitter has a return loss

- $a_r > 8 \text{ dB}$ for $0.025 f_b \leq f \leq 0.05 f_b$,
- $a_r > 14 \text{ dB}$ for $0.05 f_b \leq f \leq 1.0 f_b$ and
- $a_r > 10 \text{ dB}$ for $1.0 f_b \leq f \leq 1.5 f_b$,

with f_b being 2048 kHz (CEPT applications). A termination resistor of 120 Ω is assumed.

In T1 applications the return loss is higher than 10 dB.

Please note, that the transformer ratio at the receiver is half of that at the transmitter. The same type of transformer can thus be used at the receiver and at the transmitter. At the transmitter the two windings are connected in parallel, at the receiver in series. Thus, unbalances are avoided.

Output Jitter

In the absence of any input jitter the IPAT-2 generates an output jitter at most 0.014 UI in CEPT and 0.01 UI in T1 applications measured in the frequency range 20 Hz ... 185 kHz.

Local Loopback

The local loopback mode disconnects the receive lines RL1 and RL2 from the receiver. Instead of the signals coming from the line the data provided at XTIP and XTIN are routed through the receiver. The XDIN and XDIP signals continue to be transmitted on the line. The local loopback occurs in response to LL going high.

Remote Loopback

In the remote loopback mode the clock and data recovered from the line inputs RL1 and RL2 are routed back to the line outputs XL1 and XL2 via the transmitter. As in normal mode they are also output at RDOP, RDON and RCLK. XDIP and XDIN are disconnected from the transmitter.

The remote loopback mode is selected by a high RL signal.

Please keep in mind that the IPAT-2 is not capable of removing jitter. Therefore in remote loopback mode jitter is not reduced.

Microprocessor Interface

The IPAT-2 is fully controlled by five parallel data lines (LS0, LS1, LS2, LL and RL) and one control line (\overline{CS}). To adapt the device to a standard microprocessor interface the low state of \overline{CS} is decoded from the microprocessor address, \overline{CS} , \overline{WR} and ALE lines.

To hardwire the chip, \overline{CS} must be fixed to ground.

Receiver Loss of Signal Indication

In the case that the signal at the line receiver input (pins RL1, RL2) becomes smaller than $V_{IN} \leq 0.4 V_{OP}$ loss of signal is indicated. This voltage value corresponds to a line attenuation of about 12 dB in the CEPT case. This is performed by turning both signals RDOP, RDON after at least 32 bits simultaneously to 5 V, i.e. a logical 0 on both lines. The following ACFA processes this indication for the system. If the MODE pin is connected to V_{SS} the receiver reports additionally loss of signal by setting the RLOS (XTAL1) pin low.

Transmitter Loss of Signal Indication

If the MODE pin is connected to V_{SS} an early detection and easy isolation of non functioning links is possible because the IPAT-2 reports when the driver is no longer operational. The transmitter loss of signal indication (TLOS) is normally at a high logical level and goes to a low level if no signal is present at XL1 and XL2 for 32 clock cycles.

Operational Description

Reset

In order to work properly, the IPAT-2 needs to be started with a reset. There are three kinds of reset possible – hardware reset – software reset – and power-on reset.

– Power-On Reset

After the initial power up, the device should be reset after the power supply voltage has stabilized. The IPAT-2 is then initialized to the CEPT mode.

If the device should work in the T1 mode you have to give a hardware or software reset.

– Hardware Reset

To select this reset operation mode hardwiring the \overline{CS} pin to V_{SS} is recommended. Before giving a hardware reset the operational mode has to be selected (CEPT, T1) by setting the pins LS2, LS1, LS0 to 000 for CEPT-, to 001 for NTT-, or to 001 ... 111 for T1 application.

In the hardware mode, a reset is made by simultaneously setting both RL and LL to high ($\overline{CS} = 0$) for at least 1 μs . Reset will be initiate on the falling edge of RL and LL.

– Software Reset

This is done by simultaneously setting the pins RL and LL to logical 1 for at least 1 μs and releasing both lines thereafter simultaneously.

Besides the crystal frequency the selection of CEPT, T1 application is achieved by setting the pins LS2, LS1, LS0 simultaneously with the reset to 000 for CEPT application or to a T1 line length code (001 ... 111 see **table 2**). The logic level of the RL, LL, LS1, LS0 input parts are latched with the rising edge of the \overline{CS} . Refer to **figure 15**.

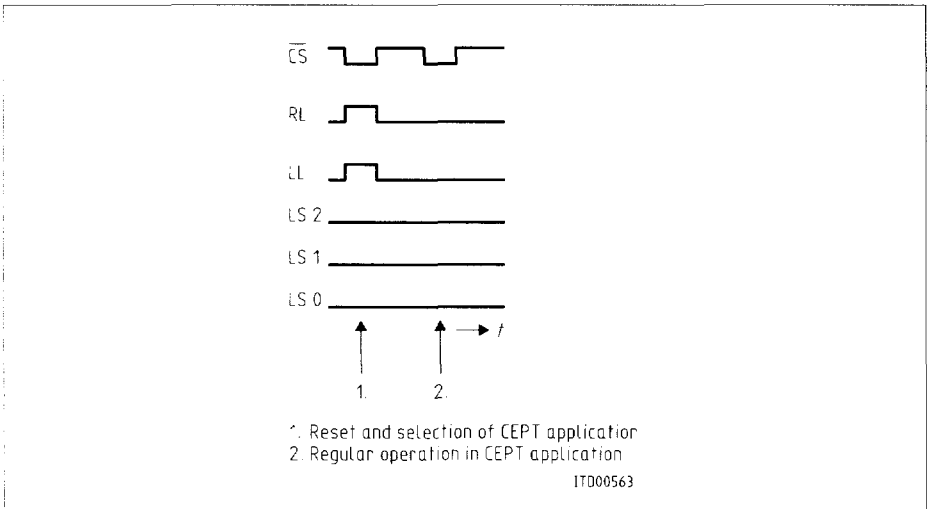


Figure 9
Timing of Software Programming for CEPT Applications

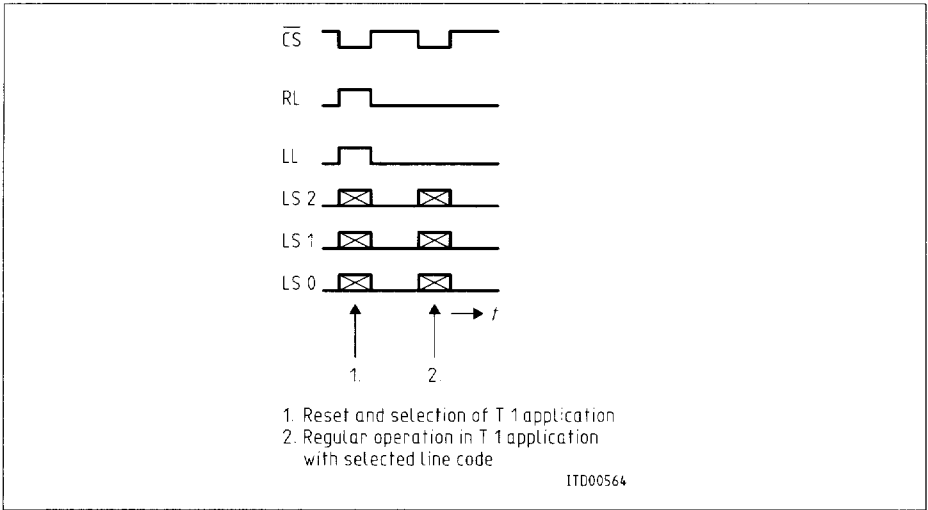


Figure 10
Timing of Software Programming for T1 Applications

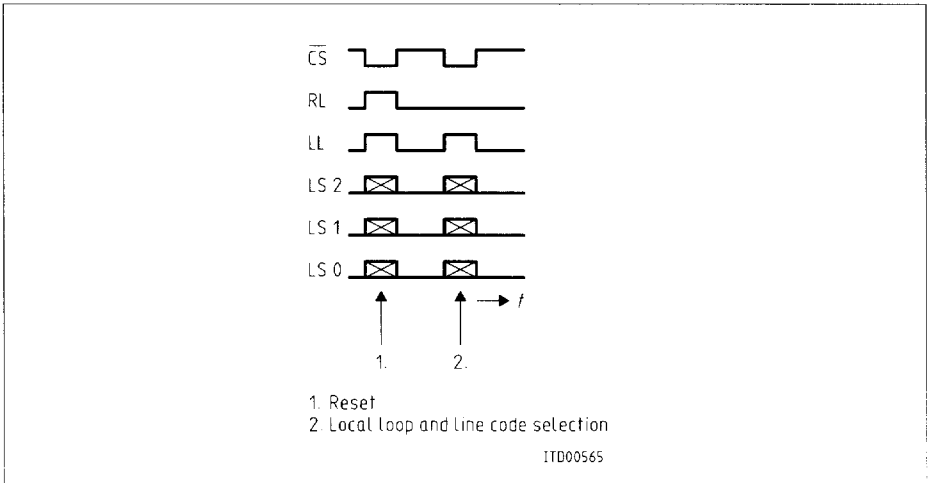


Figure 11
Timing of Software Programming for LL Operation at CEPT or T1 Applications

Electrical Specification**Absolute Maximum Ratings**

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	- 0.4 to $V_{DD} + 0.4$	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	- 65 to 125	°C

DC Characteristics

 $T_A = 0$ to 70 °C; $V_{DD} = 5$ V \pm 5 %, $V_{SS} = 0$ V

Parameter	Symbol	Limit Values		Unit	Test Condition	Pins
		min.	max.			
L-input voltage	V_{IL}	-0.4	0.8	V		All pins except RLx, XLx, XTALx, V_{DD2}
H-input voltage	V_{IH}	2.0	$V_{DD} + 0.4$	V		
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2$ mA	
H-output voltage	V_{OH}	2.4		V	$I_{OH} = -400$ μ A	
H-output voltage	V_{OH}	$V_{DD} - 0.5$		V	$I_{OH} = -100$ μ A	
Input leakage current	I_{LI}		10	μ A	0 V $< V_{IN} < V_{DD}$ to 0 V	
Output leakage current	I_{LO}				0 V $< V_{OUT} < V_{DD}$ to 0 V	
Peak voltage of a mark (CEPT)	V_{XCEPT}	2.7	3.3	V	wired according figure 8 and table 3	XL1, XL2
Peak voltage of a mark (T1)	V_{XT1}	1.8	3.4	V	T1 application: depending on line length	
Transmitter output impedance	R_x		0.3	Ω		
Transmitter output current	I_x		50 150	mA mA	CEPT application T1 application: depending on line length	
Receiver input peak voltage of a mark	V_R^*	0.4	2.5	V	BER 10^{-7} , wired according figure 6 and table 1	RL1, RL2
Receiver input threshold	V_{RTH}		45	%	of mark peak	
Voltage at V_{DD2}	V_{DD2}	2.4	2.6	V		XTAL1, XTAL2
L-input voltage	V_{XTALIL}	-0.4	1.0	V		
H-input voltage	V_{XTALIH}	4.0	$V_{DD} + 0.4$	V		
Input leakage current	I_{XTALI}		10	μ A	0 V $\leq V_{IN} \leq V_{DD}$ to 0 V	
Operational power supply current	I_{CC}	40 55	110 190	mA mA	CEPT application T1 application min. value for all zeros, max. value for all ones and max. line length for T1 appl.	

* measured against V_{DD2}

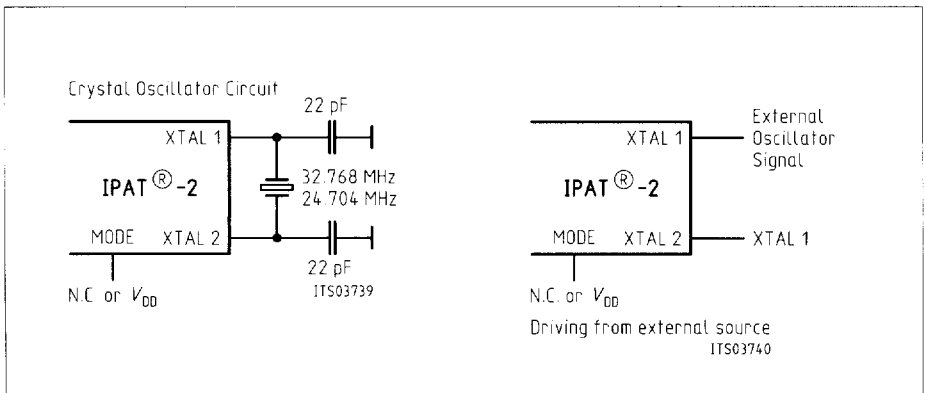
Capacitances

$T_A = 25\text{ }^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Limit Values		Unit	Pins
		min.	max.		
Input capacitance	C_{IN}		10	pF	all except RLx, XLx, XTALx
Output capacitance	C_{OUT}		15	pF	all except RLx, XLx, XTALx
Input capacitance	C_{IN}		7	pF	RLx
Output capacitance	C_{OUT}		20	pF	XLx
Load capacitance	C_{LD}		10	pF	XTALx

Recommended Oscillator Circuits

Figure 12
Oscillator Circuits



If no crystal is used XTAL1 has to be connected to an external precision clock source and XTAL2 left unconnected.

In CEPT applications, the oscillator circuit should provide a 32768-kHz clock, in T1 applications 24704 kHz.

If the MODE pin is connected to V_{SS} the XTAL1 and XTAL2 pins are outputs for TLOS and RLOS.

AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5$ V \pm 5 %

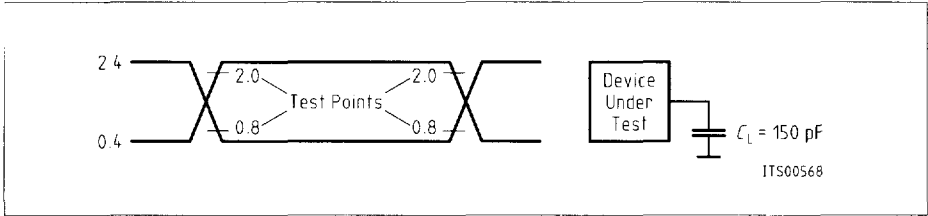


Figure 13
Input/Output Waveform for AC Tests

Except from the ternary and clock interface, inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown in **figure 15**.

Dual Rail Interface

RDOP, RDON, XDIP, XDIN, XTIP, XTIN are active low.

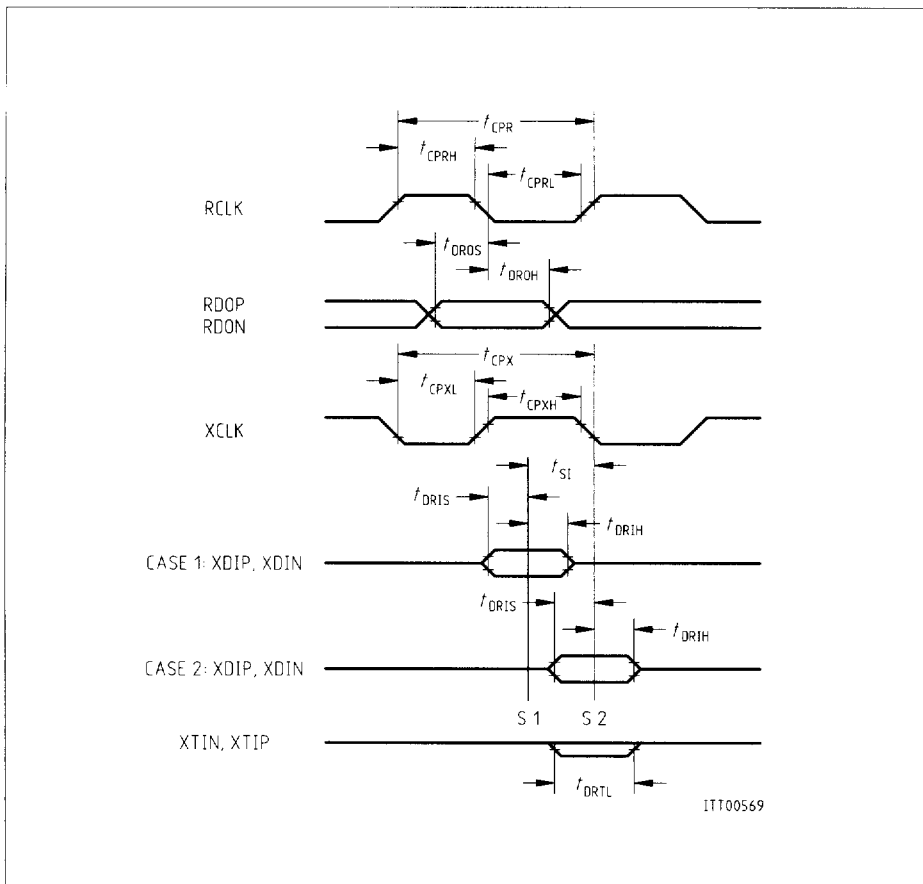


Figure 14
Timing of the Dual Rail Interface

Note: For the data XDIP, XDIN both cases are possible. The IPAT-2 detects a logical zero, if XDIP, XDIN is low for the sampling point S1 or S2!

Dual Rail Interface Timing Parameter Values

Parameter	Symbol	Limit Values				Unit
		PCM 30		PCM 24		
		min.	max.	min.	max.	
RCLK clock period	t_{CPR}	typ. 488		typ. 648		ns
RCLK clock period low	t_{CPRL}	200		260		ns
RCLK clock period high	t_{CPRH}	200		260		ns
Dual rail output setup	t_{DROS}	200		260		ns
Dual rail output hold	t_{DROH}	200		260		ns
XCLK clock period	t_{CPX}	typ. 488		typ. 648		ns
XCLK clock period low	t_{CPXL}	80	300	100	430	ns
XCLK clock period high	t_{CPXH}	125	350	170	500	ns
Sampling intervall	t_{SI}	55	67	75	87	ns
Dual rail input setup	t_{DRIS}	25		25		ns
Dual rail input hold	t_{DRIH}	25		25		ns
Dual rail test low	t_{DRTL}	170	300	220	400	ns

Microprocessor Interface

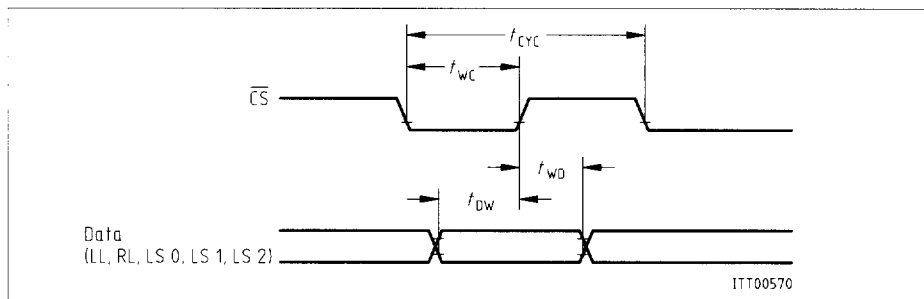


Figure 15
Timing of the Microprocessor Interface

Parameter	Symbol	Limit Values		Unit
		min.	max.	
\overline{CS} pulse width	t_{WC}	60	—	ns
Data set up time to \overline{CS}	t_{DW}	35	—	ns
Data hold time from \overline{CS}	t_{WD}	10	—	ns
Cycle Time	t_{CYC}	120		ns

XTAL Timing

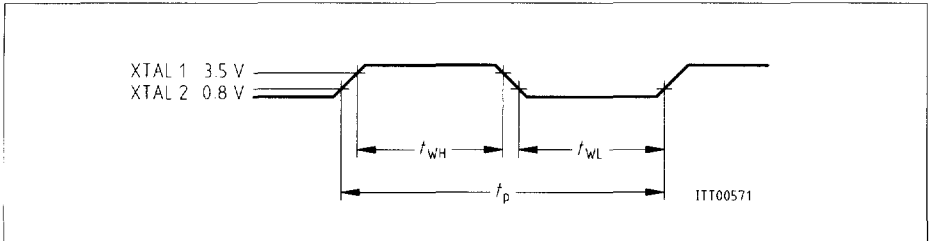


Figure 16
Timing of XTAL1/XTAL2

Clock Timing Parameter Values

Parameter	Symbol	Limit Values			Unit	Mode
		min.	typ.	max.		
Clock period of crystal/clock	t_P		30.5		ns	CEPT
	t_P		40.5		ns	T1
High phase of crystal/clock	t_{WH}	10			ns	CEPT
	t_{WH}	14			ns	T1
Low phase of crystal/clock	t_{WL}	10			ns	CEPT
	t_{WL}	14			ns	T1

Ternary Interface – Receiver

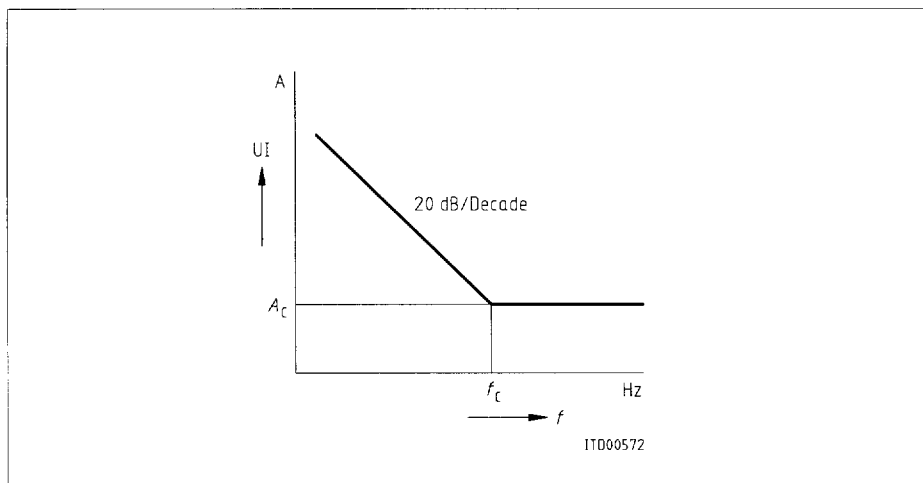


Figure 17
IPAT®-2 Receive Jitter Tolerance

Parameter	Symbol	Limit Values		Unit	Mode
		min.	max.		
Corner frequency	f_c	25		kHz	CEPT
	f_c	20		kHz	T1
Corner amplitude	A_c	0.43		UI	CEPT
	A_c	0.43		UI	T1

Ternary Interface – Transmitter

The IPAT-2 meets both CCITT and T1 pulse template requirements.

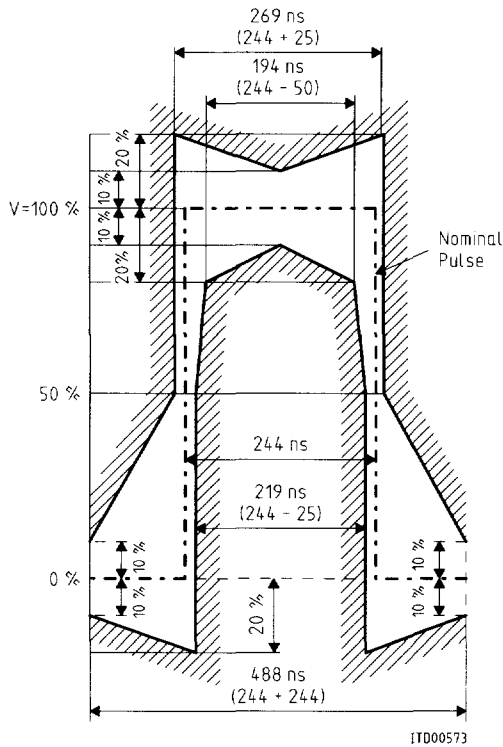


Figure 18
Pulse Template at the Transmitter Output for CEPT Applications

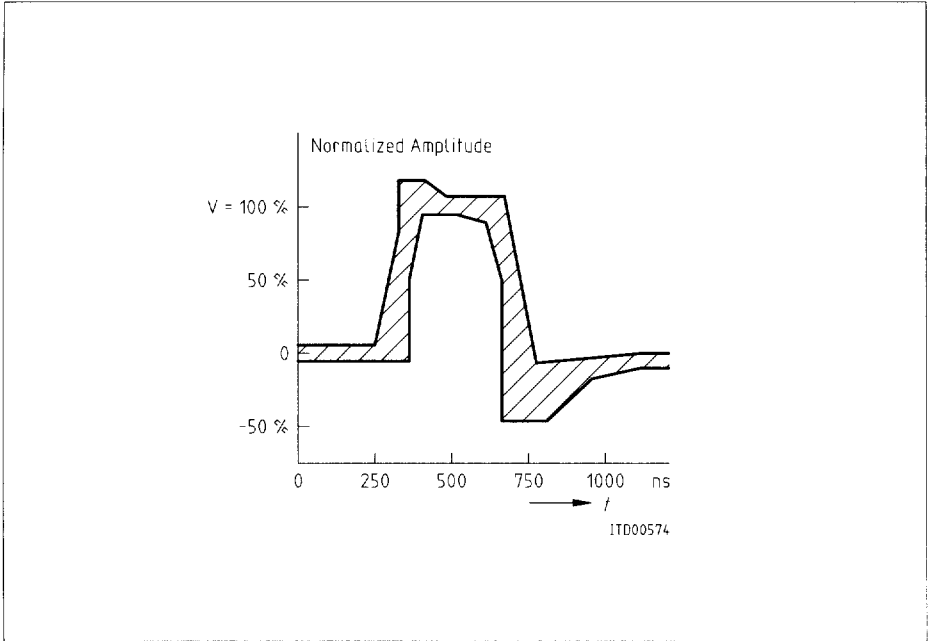


Figure 19
T1 Pulse Shape at the Cross Connect Point

Table 4
T1 Pulse Template Corner Points at the Cross Connect Point

Maximum Curve	Minimum Curve
(0, 0.05)	(0, - 0.05)
(250, 0.05)	(350, - 0.05)
(325, 0.80)	(350, 0.50)
(325, 1.15)	(400, 0.95)
(425, 1.15)	(500, 0.95)
(500, 1.05)	(600, 0.90)
(675, 1.05)	(650, 0.50)
(725, - 0.07)	(650, - 0.45)
(1100, 0.05)	(800, - 0.45)
(1250, 0.05)	(925, - 0.20)
	(1100, - 0.05)
	(1250, - 0.05)

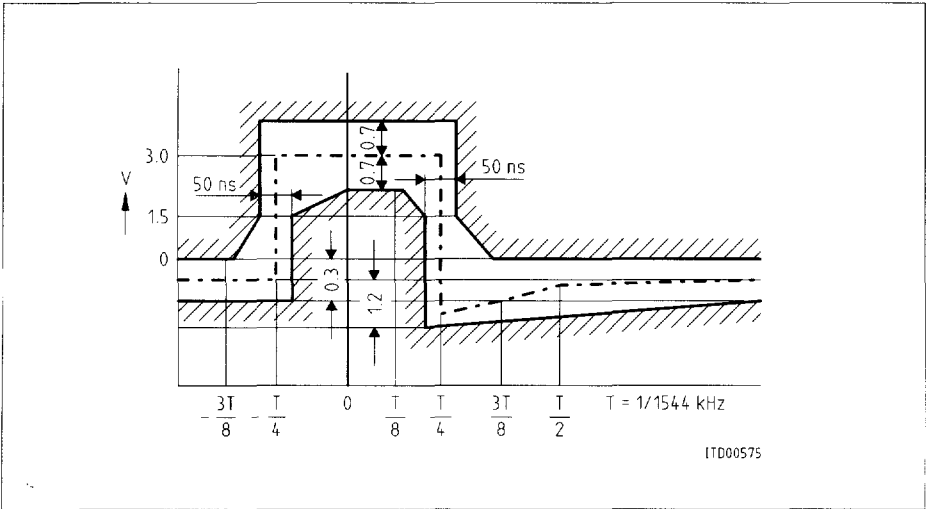


Figure 20
Pulse Shape According to CCITT G.703

Overvoltage Tolerance

To prevent the IPAT-2 from being damaged by overvoltage (i.e. from lightning), external devices like diodes or resistors have to be connected to one or both sides of the line interface transformers. Thus, overvoltage peaks are cut off. However, some residual overvoltage may remain.

The IPAT-2 simplifies the task of designing external protection circuits. Its transmitter exhibits a low line impedance so that reasonable external resistors can be connected to the line outputs. **Figure 8** with the element values of **table 3** shows how an overvoltage protection against residual overvoltages at the ternary interface can be accomplished. The solution shown also meets the stated return loss requirements.

A similar consideration applies to the receiver. The resistors R_2 of **figure 6** provide protection against residual overvoltages by attenuating voltages of both polarities across RL1 and RL2.

The maximum input current allowed to reach the IPAT-2 pins under overvoltage conditions is given as a function of the width of a rectangular input current pulse according to **figure 21**. **Figure 22** shows the curve of the maximum allowed input current across the pins RL1 and RL2, **figure 23** across the pins XL1 and XL2.

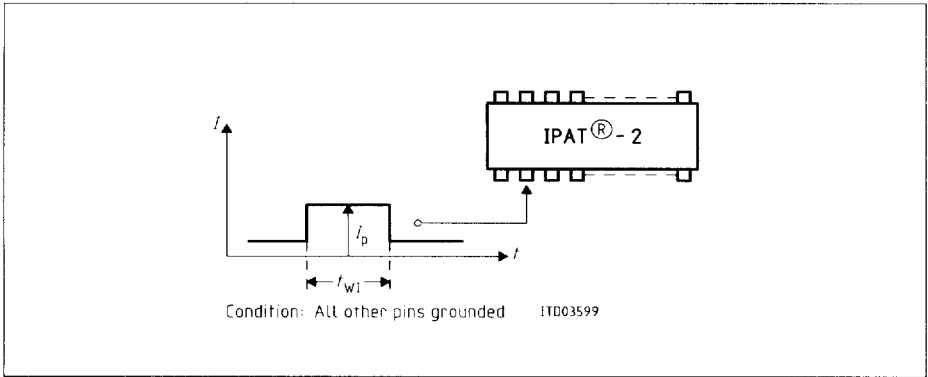


Figure 21
Measurement of Overvoltage Stress

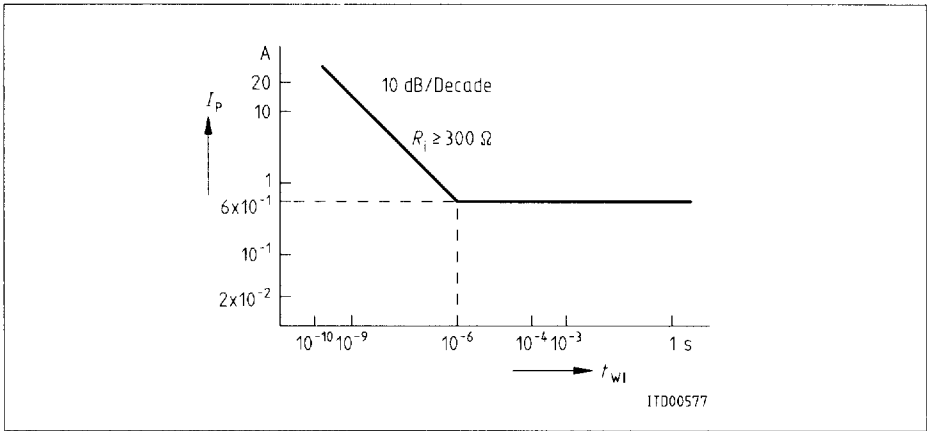


Figure 22
Tolerated Input Current at the RL1, RL2 Pins

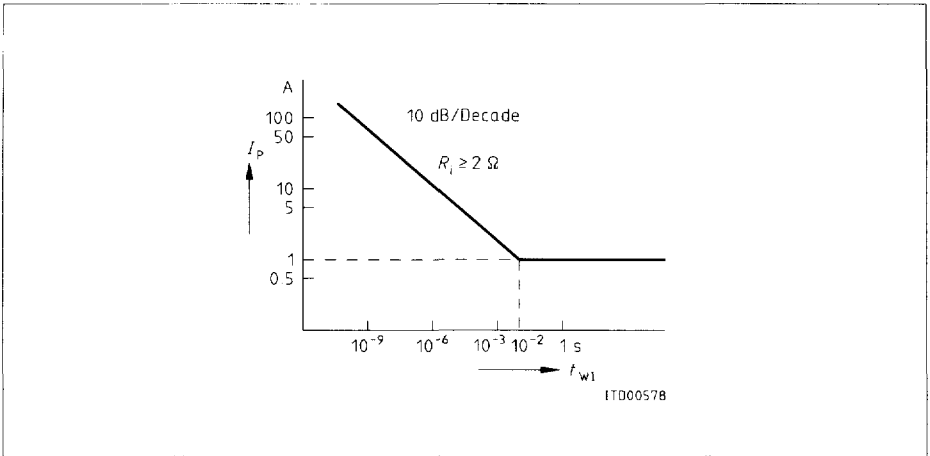


Figure 23
Tolerated Input Current at the XL1, XL2 Pins

Application Notes

The high transmitter output currents of up to 160 mA require a careful consideration of the on board power supply and ternary interface output line routing.

Modification List**IPAT®-2 Data Sheet 2/91**

Changes with respect to the IPAT Data Sheet 12/90

- Pinning:
The TEST Pin has been changed to a MODE Pin.
Connecting the MODE pin to V_{SS} , the pins XTAL1 and XTAL2 function as an output for TLOS and RLOS (XTAL2 → TLOS, XTAL1 → RLOS).
- Receiver PLL:
The receiver PLL has been changed from digital PLL to an analog PLL.
If the MODE pin is not connected or connected to V_{DD} the PLL uses as a reference either a crystal at XTAL1 and XTAL2 or an external oscillator at XTAL1.
If the MODE pin is connected to V_{SS} the PLL uses as a reference the XCLK. In this MODE the IPAT-2 doesn't need a crystal.
- Reset:
A POWER-ON RESET has been added.
- Loss of signal indication:
A transmitter (TLOS) and receiver (RLOS) loss of signal indication has been detected.

IPAT®-2 Data Sheet 11/91

Changes with respect to the IPAT-2 Data Sheet 2/91

- Loss of signal indication
In the case of loss of signal indication and MODE pin not connected to V_{DD} the receive clock RCLK is extracted from the reference clock XTAL1 and XTAL2.
- Transmitter and receiver configuration for ICOT cable
- Dual Rail Interface Timing Parameter Values