**DESCRIPTION**

This is a family of 1,048,576 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-5 or -6), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have CAS-before-RAS refresh, RAS-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 1Mx16 Fast Page Mode DRAM family is fabricated using Samsung’s advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

**FEATURES**

- **Part Identification**
  - KM416C1000C/C-L (5V, 4K Ref.)
  - KM416C1200C/C-L (5V, 1K Ref.)
  - KM416V1000C/C-L (3.3V, 4K Ref.)
  - KM416V1200C/C-L (3.3V, 1K Ref.)

- **Active Power Dissipation**
<table>
<thead>
<tr>
<th>Speed</th>
<th>3.3V</th>
<th>5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>-5</td>
<td>324</td>
<td>495</td>
</tr>
<tr>
<td>-6</td>
<td>288</td>
<td>440</td>
</tr>
</tbody>
</table>

- **Refresh Cycles**
<table>
<thead>
<tr>
<th>Part NO.</th>
<th>Vcc</th>
<th>Refresh cycle</th>
<th>Refresh period</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1000C</td>
<td>5V</td>
<td>4K</td>
<td>64ms</td>
</tr>
<tr>
<td>C1200C</td>
<td>5V</td>
<td>1K</td>
<td>16ms</td>
</tr>
<tr>
<td>V1000C</td>
<td>3.3V</td>
<td>4K</td>
<td>128ms</td>
</tr>
<tr>
<td>V1200C</td>
<td>3.3V</td>
<td>1K</td>
<td></td>
</tr>
</tbody>
</table>

- **Performance Range**
<table>
<thead>
<tr>
<th>Speed</th>
<th>tRAC</th>
<th>tCAC</th>
<th>tRC</th>
<th>tPC</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>-5</td>
<td>50ns</td>
<td>15ns</td>
<td>40ns</td>
<td>5V/3.3V</td>
<td></td>
</tr>
<tr>
<td>-6</td>
<td>60ns</td>
<td>110ns</td>
<td>40ns</td>
<td>5V/3.3V</td>
<td></td>
</tr>
</tbody>
</table>

- **Fast Page Mode operation**
- **2 CAS Byte/Word Read/Write operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden refresh capability**
- **Self-refresh capability (L-ver only)**
- **TTL(5V)/LVTTL(3.3V) compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **JEDEC Standard pinout**
- **Available in 42-pin SOJ 400mil and 50(44)-pin TSOP(II) 400mil packages**
- **Single +5V±10% power supply (5V product)**
- **Single +3.3V±0.3V power supply (3.3V product)**

**FUNCTIONAL BLOCK DIAGRAM**

**SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.**
**PIN CONFIGURATION**  (Top Views)

* **KM416C/V10(2)00CJ**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>+5V (Vcc)</td>
</tr>
<tr>
<td>2</td>
<td>DQ0</td>
</tr>
<tr>
<td>3</td>
<td>A0, A9</td>
</tr>
<tr>
<td>4</td>
<td>DQ2, A3</td>
</tr>
<tr>
<td>5</td>
<td>DQ3, A2</td>
</tr>
<tr>
<td>6</td>
<td>Vcc</td>
</tr>
<tr>
<td>10</td>
<td>DQ6, A1</td>
</tr>
<tr>
<td>11</td>
<td>DQ5, A0</td>
</tr>
<tr>
<td>12</td>
<td>N.C</td>
</tr>
<tr>
<td>13</td>
<td>W</td>
</tr>
<tr>
<td>14</td>
<td>RAS</td>
</tr>
<tr>
<td>15</td>
<td>*A11(N.C.)</td>
</tr>
<tr>
<td>16</td>
<td>*A10(N.C.)</td>
</tr>
<tr>
<td>21</td>
<td>Vcc</td>
</tr>
<tr>
<td>22</td>
<td>Vss</td>
</tr>
</tbody>
</table>

* **KM416C/V10(2)00CT**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>+5V (Vcc)</td>
</tr>
<tr>
<td>2</td>
<td>DQ0, A1</td>
</tr>
<tr>
<td>3</td>
<td>A0, A9</td>
</tr>
<tr>
<td>4</td>
<td>DQ2, A3</td>
</tr>
<tr>
<td>5</td>
<td>DQ3, A2</td>
</tr>
<tr>
<td>6</td>
<td>Vcc</td>
</tr>
<tr>
<td>10</td>
<td>DQ6, A1</td>
</tr>
<tr>
<td>11</td>
<td>DQ5, A0</td>
</tr>
<tr>
<td>12</td>
<td>N.C</td>
</tr>
<tr>
<td>13</td>
<td>W</td>
</tr>
<tr>
<td>14</td>
<td>RAS</td>
</tr>
<tr>
<td>15</td>
<td>*A11(N.C.)</td>
</tr>
<tr>
<td>16</td>
<td>*A10(N.C.)</td>
</tr>
<tr>
<td>21</td>
<td>Vcc</td>
</tr>
<tr>
<td>22</td>
<td>Vss</td>
</tr>
</tbody>
</table>

*A10 and A11 are N.C for KM416C/V1200C(5V/3.3V, 1K Ref. product)*

J : 400mil 42 SOJ
T : 400mil 50(44) TSOP II

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**Pin Name** | **Pin Function**
---|---
A0 - A11 | Address Inputs (4K Product)
A0 - A9 | Address Inputs (1K Product)
DQ0 - 15 | Data In/Out
Vss | Ground
RAS | Row Address Strobe
UCAS | Upper Column Address Strobe
LCAS | Lower Column Address Strobe
W | Read/Write Input
OE | Data Output Enable
Vcc | Power(+5V)
| Power(+3.3V)
N.C | No Connection
# ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage on any pin relative to Vss</td>
<td>Vin,</td>
<td>-0.5 to +4.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Vout</td>
<td>-1.0 to +7.0</td>
<td>V</td>
</tr>
<tr>
<td>Voltage on Vcc supply relative to Vss</td>
<td>Vcc</td>
<td>-0.5 to +4.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-1.0 to +7.0</td>
<td>V</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Pa</td>
<td>1</td>
<td>W</td>
</tr>
<tr>
<td>Short Circuit Output Current</td>
<td>Ios Address</td>
<td>50</td>
<td>mA</td>
</tr>
</tbody>
</table>

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# RECOMMENDED OPERATING CONDITIONS

Voltage referenced to Vss, TA = 0 to 70°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>3.3V</th>
<th>5V</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>Vcc</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
</tr>
<tr>
<td>Ground</td>
<td>Vss</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>Vih</td>
<td>2.0</td>
<td>-</td>
<td>Vcc+0.3*1</td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>Vil</td>
<td>-0.3*2</td>
<td>-</td>
<td>0.8</td>
</tr>
</tbody>
</table>

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc
*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss

# DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

<table>
<thead>
<tr>
<th>Max</th>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>Input Leakage Current (Any input 0 ≤ Vin ≤ Vin+0.3V, all other input pins not under test=0 Volt)</td>
<td>Ii(L)</td>
<td>-5</td>
<td>5</td>
<td>uA</td>
</tr>
<tr>
<td></td>
<td>Output Leakage Current (Data out is disabled, 0 ≤ Vouts ≤ Vcc)</td>
<td>Io(L)</td>
<td>-5</td>
<td>5</td>
<td>uA</td>
</tr>
<tr>
<td></td>
<td>Output High Voltage Level(Ioh=2mA)</td>
<td>Voh</td>
<td>2.4</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output Low Voltage Level(Iol=2mA)</td>
<td>Vol</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>5V</td>
<td>Input Leakage Current (Any input 0 ≤ Vin ≤ Vin+0.5V, all other input pins not under test=0 Volt)</td>
<td>Ii(L)</td>
<td>-5</td>
<td>5</td>
<td>uA</td>
</tr>
<tr>
<td></td>
<td>Output Leakage Current (Data out is disabled, 0 ≤ Vouts ≤ Vcc)</td>
<td>Io(L)</td>
<td>-5</td>
<td>5</td>
<td>uA</td>
</tr>
<tr>
<td></td>
<td>Output High Voltage Level(Ioh=5mA)</td>
<td>Voh</td>
<td>2.4</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output Low Voltage Level(Iol=4.2mA)</td>
<td>Vol</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
</tr>
</tbody>
</table>
### DC AND OPERATING CHARACTERISTICS (Continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Power</th>
<th>Speed</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icc1</td>
<td>Don’t care</td>
<td>-5</td>
<td>90</td>
<td>140</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-6</td>
<td>80</td>
<td>130</td>
</tr>
<tr>
<td>Icc2</td>
<td>Normal L</td>
<td>Don’t care</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>Don’t care</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Icc3</td>
<td>Don’t care</td>
<td>-5</td>
<td>90</td>
<td>140</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-6</td>
<td>80</td>
<td>130</td>
</tr>
<tr>
<td>Icc4</td>
<td>Don’t care</td>
<td>-5</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-6</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td>Icc5</td>
<td>Normal L</td>
<td>Don’t care</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>L</td>
<td>Don’t care</td>
<td>200</td>
</tr>
<tr>
<td>Icc6</td>
<td>Don’t care</td>
<td>-5</td>
<td>90</td>
<td>140</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-6</td>
<td>80</td>
<td>130</td>
</tr>
<tr>
<td>Icc7</td>
<td>L</td>
<td>Don’t care</td>
<td>300</td>
<td>200</td>
</tr>
<tr>
<td>Iccs</td>
<td>L</td>
<td>Don’t care</td>
<td>150</td>
<td>150</td>
</tr>
</tbody>
</table>

Icc1*: Operating Current (RAS and UCAS, LCAS cycling @trc=min.)
Icc2: Standby Current (RAS=UCAS=LCAS=W=VIH)
Icc3*: RAS-only Refresh Current (UCAS=LCAS=W=VIH, RAS cycling @trc=min.)
Icc4*: Fast Page Mode Current (RAS=VIIL, UCAS or LCAS, Address cycling @tpc=min.)
Icc5: Standby Current (RAS=UCAS=LCAS=W=VCC-0.2V)
Icc6*: CAS-Before-RAS Refresh Current (RAS, UCAS or LCAS cycling @trc=min.)
Icc7: Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(VIH)=Vcc-0.2V, Input low voltage(VIL)=0.2V, UCAS, LCAS=0.2V,
DQ=Don’t care, Trc=31.25us(4K/L-ver), 125us(1K/L-ver),
TRAS=Trasmin~300ns
Iccs: Self Refresh Current
RAS=UCAS=LCAS=VIIL, W=OE=A0 ~ A11=Vcc-0.2V or 0.2V,
DQ0 ~ DQ15=Vcc-0.2V, 0.2V or Open

*Note: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1, Icc3 and Iccs, address can be changed maximum once while RAS=VIIL. In Icc4, address can be changed maximum once within one fast page mode cycle time, tPC.*
### Capacitance

For the specified conditions of $25^\circ C$, $V_{CC}=5V$, or $3.3V$ and $f=1MHz$:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input capacitance [A0 – A11]</td>
<td>$C_{IN1}$</td>
<td>-</td>
<td>5</td>
<td>pF</td>
</tr>
<tr>
<td>Input capacitance [RAS, UCAS, LCAS, W, OE]</td>
<td>$C_{IN2}$</td>
<td>-</td>
<td>7</td>
<td>pF</td>
</tr>
<tr>
<td>Output capacitance [DQ0 - DQ15]</td>
<td>$C_{DQ}$</td>
<td>-</td>
<td>7</td>
<td>pF</td>
</tr>
</tbody>
</table>

### AC Characteristics

Test condition (5V device): $V_{CC}=5.0V\pm10\%$, $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$

Test condition (3.3V device): $V_{CC}=3.3V\pm0.3V$, $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>-5</th>
<th>-6</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random read or write cycle time</td>
<td>$t_{RC}$</td>
<td>90</td>
<td>110</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Read-modify-write cycle time</td>
<td>$t_{RWC}$</td>
<td>133</td>
<td>155</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Access time from RAS</td>
<td>$t_{RAC}$</td>
<td>50</td>
<td>60</td>
<td>ns</td>
<td>3,4,10</td>
</tr>
<tr>
<td>Access time from CAS</td>
<td>$t_{CAC}$</td>
<td>15</td>
<td>15</td>
<td>ns</td>
<td>3,4,5</td>
</tr>
<tr>
<td>Access time from column address</td>
<td>$t_{AA}$</td>
<td>25</td>
<td>30</td>
<td>ns</td>
<td>3,10</td>
</tr>
<tr>
<td>CAS to output in Low-Z</td>
<td>$t_{CLZ}$</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td>3</td>
</tr>
<tr>
<td>Output buffer turn-off delay</td>
<td>$t_{OFF}$</td>
<td>0</td>
<td>13</td>
<td>0</td>
<td>15</td>
</tr>
<tr>
<td>Transition time (rise and fall)</td>
<td>$t_{T}$</td>
<td>3</td>
<td>50</td>
<td>3</td>
<td>50</td>
</tr>
<tr>
<td>RAS precharge time</td>
<td>$t_{RP}$</td>
<td>30</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>RAS pulse width</td>
<td>$t_{RAS}$</td>
<td>50</td>
<td>10K</td>
<td>60</td>
<td>10K</td>
</tr>
<tr>
<td>RAS hold time</td>
<td>$t_{RSH}$</td>
<td>13</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CAS hold time</td>
<td>$t_{CSH}$</td>
<td>50</td>
<td>60</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CAS pulse width</td>
<td>$t_{CAS}$</td>
<td>13</td>
<td>10K</td>
<td>15</td>
<td>10K</td>
</tr>
<tr>
<td>RAS to CAS delay time</td>
<td>$t_{RCD}$</td>
<td>20</td>
<td>37</td>
<td>20</td>
<td>45</td>
</tr>
<tr>
<td>RAS to column address delay time</td>
<td>$t_{RAD}$</td>
<td>15</td>
<td>25</td>
<td>15</td>
<td>30</td>
</tr>
<tr>
<td>CAS to RAS precharge time</td>
<td>$t_{CRP}$</td>
<td>5</td>
<td>5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Row address set-up time</td>
<td>$t_{ASR}$</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Row address hold time</td>
<td>$t_{RAH}$</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Column address set-up time</td>
<td>$t_{ASC}$</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Column address hold time</td>
<td>$t_{CAH}$</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td>11</td>
</tr>
<tr>
<td>Column address to RAS lead time</td>
<td>$t_{RAL}$</td>
<td>25</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Read command set-up time</td>
<td>$t_{RCS}$</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Read command hold time referenced to CAS</td>
<td>$t_{RCH}$</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td>8</td>
</tr>
<tr>
<td>Read command hold time referenced to RAS</td>
<td>$t_{RRH}$</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td>8</td>
</tr>
<tr>
<td>Write command hold time</td>
<td>$t_{WCH}$</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Write command pulse width</td>
<td>$t_{WP}$</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Write command to RAS lead time</td>
<td>$t_{RWL}$</td>
<td>13</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Write command to CAS lead time</td>
<td>$t_{CWL}$</td>
<td>13</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
## AC CHARACTERISTICS (Continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>-5</th>
<th>-6</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data set-up time</td>
<td>$t_{DS}$</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td>9,17</td>
</tr>
<tr>
<td>Data hold time</td>
<td>$t_{DH}$</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td>9,17</td>
</tr>
<tr>
<td>Refresh period (1K, Normal)</td>
<td>$t_{REF}$</td>
<td>16</td>
<td>16</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Refresh period (4K, Normal)</td>
<td>$t_{REF}$</td>
<td>64</td>
<td>64</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Refresh period (L-ver)</td>
<td>$t_{REF}$</td>
<td>128</td>
<td>128</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Write command set-up time</td>
<td>$t_{WCS}$</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td>7</td>
</tr>
<tr>
<td>CAS to $W$ delay time</td>
<td>$t_{CWD}$</td>
<td>36</td>
<td>40</td>
<td></td>
<td>7,13</td>
</tr>
<tr>
<td>RAS to $W$ delay time</td>
<td>$t_{RWD}$</td>
<td>73</td>
<td>85</td>
<td>ns</td>
<td>7</td>
</tr>
<tr>
<td>Column address to $W$ delay time</td>
<td>$t_{AWD}$</td>
<td>48</td>
<td>55</td>
<td>ns</td>
<td>7</td>
</tr>
<tr>
<td>CAS precharge to $W$ delay time</td>
<td>$t_{CPWD}$</td>
<td>53</td>
<td>60</td>
<td>ns</td>
<td>7</td>
</tr>
<tr>
<td>CAS set-up time (CAS-before-RAS refresh)</td>
<td>$t_{CSR}$</td>
<td>5</td>
<td>5</td>
<td>ns</td>
<td>15</td>
</tr>
<tr>
<td>CAS hold time (CAS-before-RAS refresh)</td>
<td>$t_{CHR}$</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td>16</td>
</tr>
<tr>
<td>RAS to CAS precharge time</td>
<td>$t_{RPC}$</td>
<td>5</td>
<td>5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Access time from CAS precharge</td>
<td>$t_{CPA}$</td>
<td>30</td>
<td>35</td>
<td>ns</td>
<td>3</td>
</tr>
<tr>
<td>Fast Page mode cycle time</td>
<td>$t_{PC}$</td>
<td>35</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Fast Page read-modify-write cycle time</td>
<td>$t_{PRWC}$</td>
<td>76</td>
<td>80</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CAS precharge time (Fast Page cycle)</td>
<td>$t_{CP}$</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td>12</td>
</tr>
<tr>
<td>RAS pulse width (Fast Page cycle)</td>
<td>$t_{RASP}$</td>
<td>50</td>
<td>200K</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>RAS hold time from CAS precharge</td>
<td>$t_{RHCP}$</td>
<td>30</td>
<td>35</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$OE$ access time</td>
<td>$t_{OEA}$</td>
<td>13</td>
<td>15</td>
<td>ns</td>
<td>3</td>
</tr>
<tr>
<td>$OE$ to data delay</td>
<td>$t_{OED}$</td>
<td>13</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Output buffer turn off delay time from $OE$</td>
<td>$t_{OEZ}$</td>
<td>0</td>
<td>13</td>
<td>0</td>
<td>15</td>
</tr>
<tr>
<td>$OE$ command hold time</td>
<td>$t_{OEH}$</td>
<td>13</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>RAS pulse width (C-B-R self refresh)</td>
<td>$t_{RASS}$</td>
<td>100</td>
<td>100</td>
<td>us</td>
<td>18,19,20</td>
</tr>
<tr>
<td>RAS precharge time (C-B-R self refresh)</td>
<td>$t_{RPS}$</td>
<td>90</td>
<td>110</td>
<td>ns</td>
<td>18,19,20</td>
</tr>
<tr>
<td>CAS hold time (C-B-R self refresh)</td>
<td>$t_{CHS}$</td>
<td>-50</td>
<td>-50</td>
<td>ns</td>
<td>18,19,20</td>
</tr>
</tbody>
</table>
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 RAS-only refresh or CAS-before-RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. Vih(min) and Vil(max) are reference levels for measuring timing of input signals. Transition times are measured between Vih(min) and Vil(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only.
   If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to Vih or Vol.
7. twCS, twRD, tcWD, tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If twCS≥twCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tcWD≥tcWD(min), tAWD≥tAWD(min), tCPWD≥tCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to CAS falling edge in early write cycles and to W falling edge in OE controlled write cycle and read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only.
   If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tASC, tCAH are referenced to the earlier CAS falling edge.
12. tCP is specified from the later CAS rising edge in the previous cycle to the earlier CAS falling edge in the next cycle.

<table>
<thead>
<tr>
<th>KM416C/V10(2)00C/C-L Truth Table</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RAS</strong></td>
</tr>
<tr>
<td>--------</td>
</tr>
<tr>
<td>H</td>
</tr>
<tr>
<td>L</td>
</tr>
<tr>
<td>L</td>
</tr>
<tr>
<td>L</td>
</tr>
<tr>
<td>L</td>
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<tr>
<td>L</td>
</tr>
<tr>
<td>L</td>
</tr>
<tr>
<td>L</td>
</tr>
</tbody>
</table>
13. \( t_{CWD} \) is referenced to the later \( \overline{CAS} \) falling edge at word read-modify-write cycle.

14. \( t_{CWL} \) is specified from \( \overline{W} \) falling edge to the earlier \( \overline{CAS} \) rising edge.

15. \( t_{CSR} \) is referenced to the earlier \( \overline{CAS} \) falling edge before \( RAS \) transition low.

16. \( t_{CHR} \) is referenced to the later \( \overline{CAS} \) rising edge after \( RAS \) transition low.

17. \( t_{DS}, t_{DH} \) is independently specified for lower byte DQ(0-7), upper byte DQ(8-15)

18. If \( t_{RASS} \geq 100 \text{us} \), then \( \overline{RAS} \) precharge time must use \( t_{RPS} \) instead of \( t_{RP} \).

19. For \( RAS \)-only refresh and burst \( \overline{CAS} \)-before-\( RAS \) refresh mode, 4096(4K)/1024(1K) cycles of burst refresh must be executed within 64ms/16ms before and after self refresh, in order to meet refresh specification.

20. For distributed \( \overline{CAS} \)-before-\( RAS \) with 15.6us interval \( \overline{CAS} \)-before-\( RAS \) refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.
WORD READ CYCLE

- RAS: \( V_{IH} - V_{IL} \)
- UCAS: \( V_{IH} - V_{IL} \)
- LCAS: \( V_{IH} - V_{IL} \)
- A: \( V_{IH} - V_{IL} \)
- W: \( V_{IH} - V_{IL} \)
- OE: \( V_{IH} - V_{IL} \)
- DQ0 ~ DQ7: OPEN
- DQ8 ~ DQ15: OPEN

Don't care
Undefined
LOWER BYTE READ CYCLE

NOTE: D\textsubscript{IN} = OPEN
UPPER BYTE READ CYCLE

NOTE: Din = OPEN

- RAS
- UCAS
- LCAS
- A
- W
- OE
- DQ0 ~ DQ7
- DQ8 ~ DQ15

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE

VH - VIL

- RAS
- UCAS
- LCAS
- A
- W
- OE
WORD WRITE CYCLE (EARLY WRITE)

NOTE: DOUT = OPEN
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE: D_{out} = OPEN

- RAS
  - V_{IH} - V_{IL} -
  - t_{CRP}
- UCAS
  - V_{IH} - V_{IL} -
  - t_{CRP}
- LCAS
  - V_{IH} - V_{IL} -
  - t_{RAD}
- A
  - V_{IH} - V_{IL} -
  - t_{ASR} t_{TAS} t_{ASC}
- W
  - V_{IH} - V_{IL} -
  - t_{WCS} t_{TWCH} t_{WP}
- OE
  - V_{IH} - V_{IL} -
- DQ0 ~ DQ7
  - V_{IH} - V_{IL} -
  - t_{DS} t_{IDH}
- DQ8 ~ DQ15
  - V_{IH} - V_{IL} -

Legend:
- Don’t care
- Undefined
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE: DOUT = OPEN
WORD WRITE CYCLE (OE CONTROLLED WRITE)

NOTE: Dout = OPEN

Legend:
- Don't care
- Undefined

Diagram showing timing parameters for word write cycle with OE controlled write.
LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE: DOUT = OPEN

- RAS, UCAS, LCAS
- A, W
- OE
- DQ0 ~ DQ7
- DQ8 ~ DQ15

Legend:
- Don’t care
- Undefined
UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE: Dout = OPEN

[Diagram showing timing parameters such as trAS, trC, trP, trCD, trSH, tCAS, etc., and signal states like \( V_{IH} \), \( V_{IL} \), \( O_{EH} \), \( O_{ED} \), and data lines DQ0 to DQ15.]

Legend:
- Grey: Don’t care
- Black: Undefined
LOWER-BYTE READ - MODIFY - WRITE CYCLE

Don't care
Undefined
UPPER-BYTE READ - MODIFY - WRITE CYCLE

- RAS  \( V_{IH} - V_{IL} \) - \( t_{CRP} \) - \( t_{RCD} \) - \( t_{RAD} \) - \( t_{ASR} \) - \( t_{TRAS} \) - \( t_{RP} \)
- UCAS  \( V_{IH} - V_{IL} \) - \( t_{CRP} \) - \( t_{CAS} \)
- LCAS  \( V_{IH} - V_{IL} \) - \( t_{CRP} \) - \( t_{SH} \) - \( t_{ASH} \) - \( t_{CAS} \)

- \( V_{IH} - V_{IL} \) - \( t_{SH} \) - \( t_{WSH} \) - \( t_{RSH} \)
- AE  \( V_{IH} - V_{IL} \) - \( t_{OE} \) - \( t_{OEZ} \)

- \( DQ0 \sim DQ7 \)  \( V_{I/OH} - V_{I/OL} \) - \( t_{CLZ} \) - \( t_{CL} \) - \( t_{CAA} \)
- \( DQ8 \sim DQ15 \)  \( V_{I/OH} - V_{I/OL} \) - \( t_{OE} \) - \( t_{OEZ} \) - \( t_{DS} \) - \( t_{DH} \) - \( t_{DZ} \) - \( t_{D} \)

- Valid Data-Out
- Valid Data-In

Legend:
- Don’t care
- Undefined
FAST PAGE MODE WORD READ CYCLE
FAST PAGE MODE LOWER BYTE READ CYCLE
FAST PAGE MODE UPPER BYTE READ CYCLE
FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE: DOUT = OPEN
FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE: Dout = OPEN

Don't care
Undefined
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE: DOUT = OPEN

- **RAS**
  - **V_{IH}** -
  - **V_{IL}** -
- **UCAS**
  - **V_{IH}** -
  - **V_{IL}** -
- **LCAS**
  - **V_{IH}** -
  - **V_{IL}** -
- **A**
  - **V_{IH}** -
  - **V_{IL}** -
- **\overline{W}**
  - **V_{IH}** -
  - **V_{IL}** -
- **\overline{OE}**
  - **V_{IH}** -
  - **V_{IL}** -
- **DQ0 ~ DQ7**
  - **V_{IH}** -
  - **V_{IL}** -
- **DQ8 ~ DQ15**
  - **V_{IH}** -
  - **V_{IL}** -
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE
FAST PAGE MODE LOWER BYTE READ - MODIFY - WRITE CYCLE

- V_{IH} - V_{IL}
- RAS
- UCAS
- LCAS
- A
- W
- OE
- DQ0 ~ DQ7
- DQ8 ~ DQ15
- V_{IOH} - V_{IOL}
- DQ8 ~ DQ15
- V_{IOH} - V_{IOL}
- OPEN

- trCS
- tRCD
- tPRWC
- tCAS
- tCP
- tASR
- tCRP
- trSH
- trPC
- tr WL

- tAA
- tOEZ
- tOE
- tOA
- tPSW
- tOEZ
- tOE
- tOA
- tPSW

- tCLZ
- tCLZ
- VALID DATA-OUT
- VALID DATA-IN
- VALID DATA-OUT
- VALID DATA-IN

Don’t care
Undefined
RAS - ONLY REFRESH CYCLE

NOTE: W, OE, DIN = Don’t care

DOUT = OPEN

CAS - BEFORE - RAS REFRESH CYCLE

NOTE: OE, A = Don’t care

DQ0 ~ DQ7
V_{OH} - V_{OL}

DQ8 ~ DQ15
V_{OH} - V_{OL}

OPEN

Don’t care
Undefined
HIDDEN REFRESH CYCLE (READ)

Don’t care

Undefined
HIDDEN REFRESH CYCLE (WRITE)

NOTE: Dout = OPEN
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE: OE, A = Don't care

- RAS
  - \( V_{IH} \) - \( V_{IL} \)
  - \( \overline{RAS} \)

- UCAS
  - \( V_{IH} \) - \( V_{IL} \)

- LCAS
  - \( V_{IH} \) - \( V_{IL} \)

- DQ0 ~ DQ7
  - \( V_{OH} \) - \( V_{OL} \)
  - \( \text{OPEN} \)

- DQ8 ~ DQ15
  - \( V_{OH} \) - \( V_{OL} \)
  - \( \text{OPEN} \)

ICP, ICSR, TOFF, TRP, TRASS, TRPS, ICHS

Don't care
Undefined

CAR
OPEN
KM416C1000C, KM416C1200C
KM416V1000C, KM416V1200C

CMOS DRAM

PACKAGE DIMENSION

42 SOJ 400mil

Units: Inches (millimeters)

50(44) TSOP(II) 400mil

Units: Inches (millimeters)

SAMSUNG ELECTRONICS