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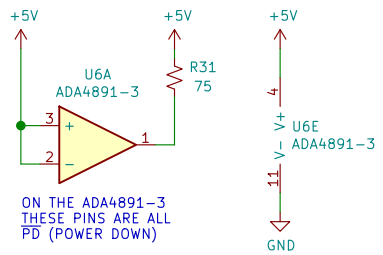
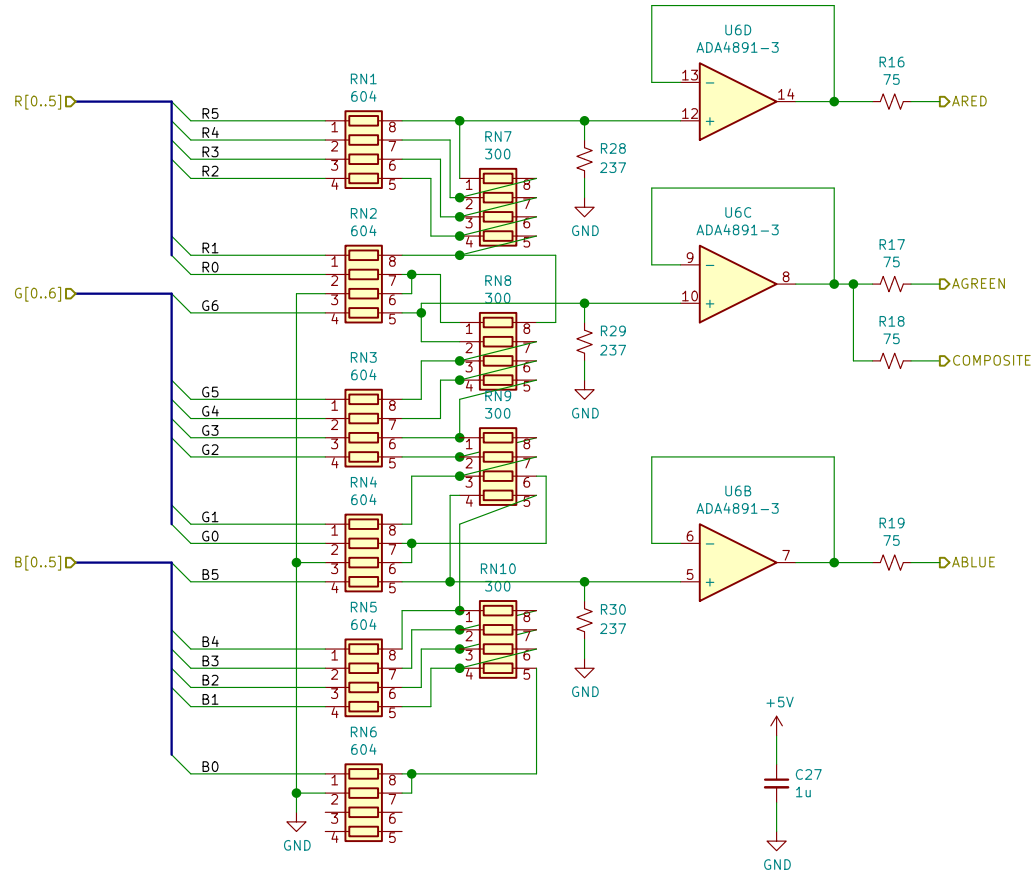
GRAPHICS GREMLIN
DESIGN BY @TubeTimeUS

Sheet: /Bus Interface/
File: bus_interface.sch

Title: ISA Bus Interface

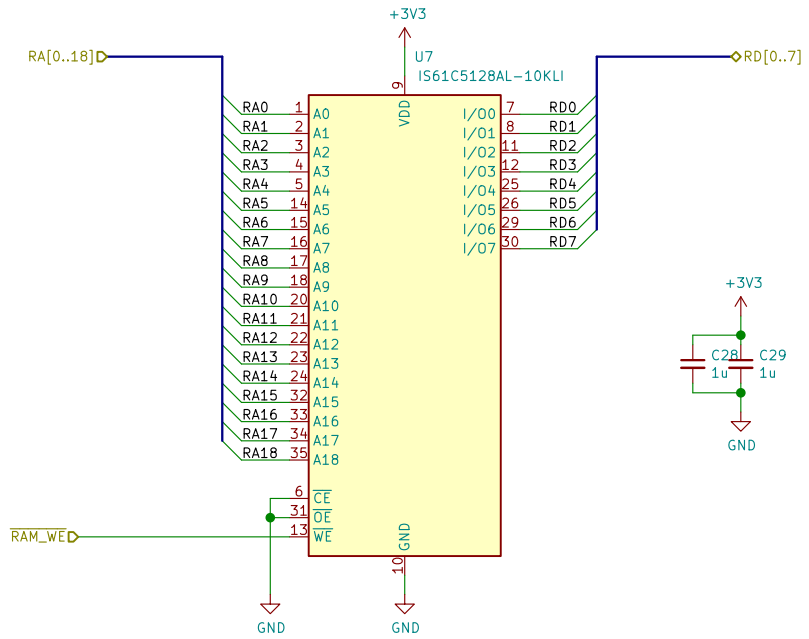
Size: A4 Date:
KiCad E.D.A. kicad (5.1.0)-1

Rev: 2
Id: 2/5



GRAPHICS GREMLIN DESIGN BY @TubeTimeUS		
Sheet: /vga_dac/ File: vga_dac.sch		
Title: Resistor Ladder DAC and Output Buffer		
Size: A4	Date:	Rev: 2
KiCad E.D.A. kicad (5.1.0)-1		Id: 3/5

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GRAPHICS GREMLIN

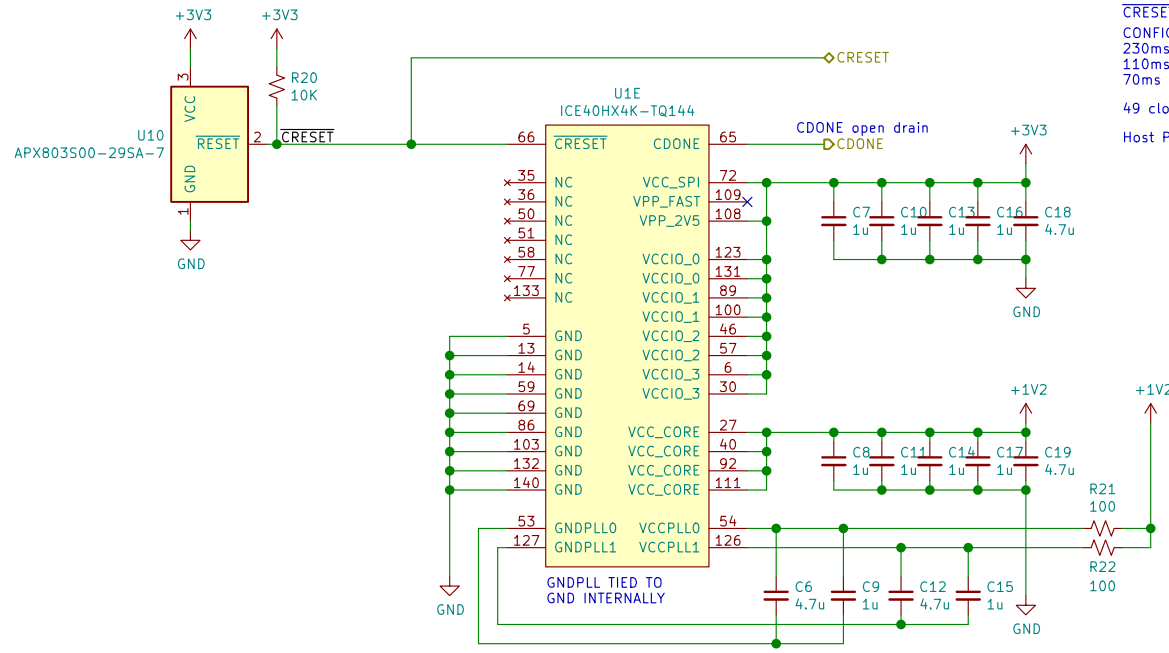
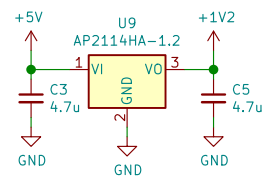
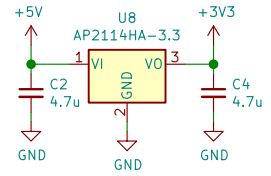
DESIGN BY @TubeTimeUS

Sheet: /RAM/
File: RAM.sch

Title: SRAM

Size: A4 Date:
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Rev: 2
Id: 4/5



MAX803 delay: 3.3ms max
 CRESET high to first MCLK edge: 1.2ms
 CONFIG TIME: MCLK Frequency:
 230ms (slow, default) 7.5MHz (slow, default)
 110ms (medium) 24MHz (medium)
 70ms (fast) 40MHz (high)
 49 clock cycles from CDONE going high to PIO going active
 Host PC reset pulse appears to be about 350ms min

0.4V/ms to 10V/ms ramp rate range
 1.2V: 0.12ms to 3ms
 3.3V: 0.33ms to 8.25ms

GRAPHICS GREMLIN
 DESIGN BY @TubeTimeUS

Sheet: /power/
 File: power.sch

Title: Power Regulators and Reset Circuit

Size: A4	Date:	Rev: 2
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