ICs for Communications
Signal Processing Codec Filter
SICOFI®, SICOFI®-2

User’s Manual 03.92
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OM®, IOM®, I2C® components convey a license under the Philips’ I2C patent to use the components in the I2C-system provided the system conforms to the I2C specifications defined by Philips. Copyright Philips 1983.
Introduction

The following chapters inform you about the technical data and programming of the Signal Processing Codec Filter SICOFI® / SICOFI®-2 PEB 2060/2260 and describe the hardware and software tools. Application notes show you how to use and work with the SICOFI family in a given application.

In order to get an overview of the architecture, the devices and the tools, we suggest to start having a look at the 'General Overview on Architectures and Devices' as well as 'Development Support Tools'.

Detailed descriptions can be found in the other chapters.

For more information on related products and quality issues we provide the information on literature.
1. Type-Designation Code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15*), edition 1988.

*) Available from Pro Electron
Avenue Louise, 430 (B.12)
B-1050 Bruxelles, Belgium

2. Mounting Instructions

Plastic Packages for Insertion

The pins of the packages are bent downwards by an angle of 90° and fit into holes on a grid of 2.54 mm and with diameters of between 0.7 and 0.9 mm. The dimension x is shown in the corresponding drawing of the package.

The bottom of the package will not touch the circuit board after insertion because the pins have shoulders just below the package (see figure 1).

After insertion of a package on a board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering.

Plastic packages are soldered on the board on the side facing away from the package.

The maximum permissible soldering temperature is 260 °C (max. 10 s) when using a solder bath, e.g. wave soldering, and 350 °C (max. 3 s) when using a soldering iron.

![Figure 1](image)

Plastic Packages (P-DSO and P-LCC) for Surface Mounting (SMD)

Reflow soldering: for a device temperature of 215 °C max. soldering time 2 x 40 s (typical figure for vapor-phase soldering)

Wave soldering: soldering temperature 260 °C, soldering time max. 10 s.

Soldering iron: the minimum thermal stress, based on experience, is at a soldering temperature of 350 °C (soldering time ≤ 3 s)
Storage and Pretreatment of SMD ICs
The components should be stored in a dry place. Some large and specially identified plastic ICs have to be processed in a dry condition. This is produced by dry packing or by means of a separate drying process shortly before they are processed (e.g. 16 h at 125 °C).

3 Processing Guidelines for ICs
Integrated circuits (ICs) are electrostatic-sensitive (ESS) devices. The demand for greater packing density has led to smaller structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.
MOS and CMOS devices generally have integrated protective circuits and it is virtually impossible for them to be destroyed by purely static electricity. On the other hand, there is acute danger from electrostatic discharges (ESD).
Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. Low-resistive discharges can produce peak powers amounting to kilowatts.
For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
   Means which are effective here are an increase in relative humidity to ≥ 60 % and the replacement of highly charging plastics by antistatic materials.

b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^9 \, \Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification
The packing of ESS devices is provided with the following label by the manufacturer:

Scope
The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.
Handling of Devices

1. ICs must be left in their containers until they are processed.

2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of $10^6$ to $10^9$ Ω/cm.

3. With humidity of > 50% a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 kΩ to 100 kΩ.

4. If conductive floors, \( R = 5 \times 10^4 \) to \( 10^7 \) Ω are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole \( (R \approx 10^5 \text{ to } 10^7 \Omega) \).

5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of \( 10^5 \) to \( 10^8 \) Ω.

6. When loading machines and production devices it is necessary to ensure that the devices do not come out of the transport magazine charged and that they are not damaged by touching metal, e.g. parts of a machine.

   Example 1) conductive (black) tubes.
   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person. Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2) anti-static (transparent) tubes.
   The devices cannot be destroyed in the tube by charged persons (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material \((\approx 10^6 \text{ to } 10^8 \Omega/cm)\) between the tube and the machine.

The use of metal tubes – especially of anodized aluminium – is not advisable because of the danger of low-resistance device discharge.
Storage
ESS devices should only be stored in identified locations provided for the purpose.
During storage the devices should remain in the packing in which they are supplied.
The storage temperature should not exceed 30 °C.

Transport
ESS devices in approved packing tubes should only be transported in suitable containers
of conductive or longterm anti-static-treated plastic or possibly unvarnished wood.
Containers of both high-charging plastic or very low-resistance materials are unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity
($R < 10^6 \Omega$). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming Inspection
In incoming inspection the above guidelines should be observed. Otherwise any right to
refund or replacement if devices fail inspection may be lost.

Material and Mounting

1. The drive belts of machines used for the processing of the devices, in as much as they
come into contact with them (e.g. bending and cutting machines, conveyor
belts), should be treated with anti-static spray (e.g. anti-static spray 100 from
Kontaktchemie). It is better, however, to avoid the contact completely.

2. If ESS devices have to be soldered or desoldered manually, soldering irons with
thyristor control may not be used. Siemens EMI-suppression capacitors of the type
B 81711-B31...–B36 have been proven very effective against line transients.

3. Circuit boards fitted and soldered with ESS devices are always to be considered as
endangered.
Electrical Tests and Application Circuit

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.

2. The sockets or integrated circuits must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works specifications state otherwise. Ensure that the test devices and power supplies do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.

3. When supplying bipolar integrated circuits with current, the negative voltage (\(-V_s\) or GND) has first to be connected. In general, an interruption of this potential during operation is not permissible.

4. Signal voltages may only be applied to the inputs of ICs when or better after the supply voltage is turned on. They must be disconnected when or better before the supply voltage is turned off.

5. Power supplies of integrated circuits are to be blocked as near as possible at the supply terminals of the IC. With bipolar ICs it is recommended to use a low-inductance electrolytic capacitor or at least a paralleled ceramic capacitor of 100 nF to 470 nF for example.
   
   Using ICs with high output currents, the necessary value of the electrolytic capacitor must be adapted to the test or application circuit. Transient behavior and dynamic output resistance of the power supplies, line inductances in the supply and load circuit and in particular inductive loads or motors have to be considered.
   
   When switching off line inductances of inductive loads, the stored power has to be consumed externally, unless otherwise specified (e.g. by an electrolytic capacitor, diodes, Z-diodes or the power supply). Also a switching off of the supply voltage prior to the load rejection should be taken into account.

6. ICs with low-pass character of the output stages (e.g. PNP drivers or PNP/NPN end-stages), normally need an additional external compensation at the output. This applies particularly to complex loads. The output of AF power amplifiers is compensated by the Boucherot element. In individual cases, bridge circuits only need a capacitance for bypassing the load. Depending on the application it is, however, also recommended to connect one capacitor from each output to ground.

7. Observe any notes and instructions in the respective data books.
Packing of Assembled PC Boards or Flatpack Units

The packing material should exhibit low volume conductivity:

\[ 10^5 \, \Omega/cm < \rho < 10^{10} \, \Omega/cm. \]

In most cases – especially with humidity of > 40 % – this requirement is fulfilled by a simple corrugated board.

Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

You should always ensure that different boards cannot touch.

In special cases it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example.

For this purpose a sheath of aluminium foil is recommended, although direct contact between the film and the PCB must be avoided.

Cardboard boxes with an aluminium-foil lining, such as those used for shipping our devices, are available from Laber of Munich.

Ultrasonic Cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

- sound frequency \( f > 40 \, \text{kHz} \)
- exposure \( t < 2 \, \text{min} \)
- alternating sound pressure \( p < 29 \, \text{kPa} \)
- sound power \( N < 0.5 \, \text{W/cm}^2/\text{liter} \)
4 Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25 \, ^\circ C$ and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

5 Quality Assurance

Quality Assurance System

The high quality and reliability of integrated circuits from Siemens are the results of carefully managed design and production which is systematically checked and controlled at each stage.

The procedures are subject to a quality assurance system; full details are given in the brochure “Quality Assurance – Integrated Circuits”.

Figure 1 and 2 show the most important stages of Quality Assurance (QA) system. QA departments independent of production and development are responsible for the selected measures, acceptance procedures and information feedback loops. Operating QA departments have state-of-the-art test and measuring equipment at their disposal, work according to approved methods of statistical quality control, and are provided with facilities for accelerate life and environmental tests used for both qualification and routine monitoring tests.

The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The QA department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives to ensure statistically that the PDA of released lots is less than the AQL agreed. Sampling inspection is performed in accordance with the inspection plans of DIN 40 080, as well as of the identical MIL-STD-105 or IEC 410.
Reliability

Measures Taken During Development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, e.g. specifying minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these designs standards.
In-Process Control During Production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged in a manner that the individual steps of the process can be reproduced continuously.

The decreasing failure rates reflect the persistent effort in this direction; in the course of the years they have been reduced considerably despite an immense rise in IC complexity.

Reliability Monitoring

The general course of the IC failure rate versus time is shown by a so-called "bathtub" curve. The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor $B$ for the life test can be obtained from the Arrhenius equation

$$B = \exp \left( \frac{E_A}{k} \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right)$$

where $T_2$ is the temperature at which the life test is performed, $T_1$ is the assumed operating temperature, and $k$ is the Boltzmann constant.

Important for factor $B$ is the activation energy $E_A$. It lies between 0.3 and 1.3 eV and differs considerably for the individual failure mechanisms.

For all Siemens ICs, the reliability data gained from life tests are converted to an operating temperature of $T_A = 55$ °C, assuming an average activation energy of 0.5 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method also considers failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "Quality Assurance-Integrated Circuits". Such tests are e.g. humidity test at 85 °C and 85 % relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.
1 General Exchange Architecture
1.1 Analog Line Cards

In a digital exchange system the subscriber line boards provide the link between the subscriber and the switching network. The basic functions of analog line boards are known under the acronym BORSHT (battery, overvoltage, ringing, supervision, hybrid, testing). Moreover, further important tasks are voice frequency band limitation, analog to digital conversion into time discrete digital equivalents, time-slot assignment on the PCM highways and handling of signaling and control information.

**Usual implementation** uses two PCM ports and one \( \mu \)P interface per subscriber line leading to a large amount of wiring and, thus, problems such as crosstalk and large board size.

**Usual implementation** is also characterized by fixed adjustment of line interface conditions although telephone line conditions vary considerably with national standards and even with subscriber line installations. Under adverse conditions telecommunication equipment must match the subscriber line and termination impedances while suppressing return echoes in the two- to four-wire hybrid network. Compensating for line attenuation is just as critical for balancing the voice signals in the transmission and reception paths.

To improve voice quality, subscriber line boards have to be matched to different line conditions by means of interchangeable discrete components. This approach is very costly regarding line board design and manufacturing. Furthermore, the reliability of a board filled with parts, wires and connections will decrease rapidly.

The subscriber line board architecture proposed by Siemens Semiconductor is geared to eliminate many of these line board trouble spots.
General Line Board Structure and Functions

General Line Card Function

<table>
<thead>
<tr>
<th>Component</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLIC (Subscriber</td>
<td>realisation of the BORSHT function</td>
</tr>
<tr>
<td>line interface</td>
<td>B battery feed</td>
</tr>
<tr>
<td>circuit)</td>
<td>O overvoltage protection</td>
</tr>
<tr>
<td>analog network Z</td>
<td>R ringing</td>
</tr>
<tr>
<td>R, X, B, G</td>
<td>S supervision</td>
</tr>
<tr>
<td>CODEC/Filter</td>
<td>H hybrid</td>
</tr>
<tr>
<td>PCM</td>
<td>T testing</td>
</tr>
<tr>
<td></td>
<td>matching of input and line impedance</td>
</tr>
<tr>
<td></td>
<td>frequency response correction</td>
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<tr>
<td></td>
<td>hybrid balancing</td>
</tr>
<tr>
<td></td>
<td>gain adjustment</td>
</tr>
<tr>
<td></td>
<td>coding, A/D and D/A conversion according to A-law and µ-law, voice</td>
</tr>
<tr>
<td></td>
<td>band limitation according to CCITT and LSSGR</td>
</tr>
<tr>
<td></td>
<td>time-slot assignment, PCM data rate</td>
</tr>
</tbody>
</table>
1.2 Optimized Line Board Architecture

The Siemens Semiconductor concept is characterized by a centralized PCM interface controller device providing the variable Time-Slot Assignment (TSA), the communication with up to 64 subscriber line devices such as signal processing codec/filter (SICOFI®) or ISDN devices via the SLD (Subscriber Line Data) or IOM®-2 (ISDN Oriented Modular) interface, and the interface with a microprocessor.

As a characteristic architectural feature, for test, monitoring and control purposes, the device permits efficient switching of data streams between all these interfaces and, therefore, ensures transparency between the PCM channels and control or signaling data. This opens up attractive possibilities such as common-channel signaling and microprocessor access to PCM data.

The use of the signal processing codec/filter (SICOFI) avoids the analog network which has to be matched to different requirements by interchanging its discrete components. Based on Digital Signal Processing (DSP) methods the SICOFI allows the complete control of the line conditions by software.

The all-over flexibility of the unique device concept gives the user the capability for designing a standard line card which can be customized for each application under software control. The SLD/IOM-2 architecture leads to a highly modular line board configuration with low wiring, reduced board area and, depending only on the SLIC to be used, very few discrete elements.

---

Siemens ICs for Analog Subscriber Lines
1.3 The SLD/IOM®-2 Interface

The SLD bus is used by the PBC/PIC to interface with the subscriber line devices. A Serial Interface Port (SIP) is used for the transfer of all digital voice and data, feature control and signaling information between the individual subscriber line devices, the PCM highways and the control backplane. The SLD approach provides a common interface for analog or digital per-line components. Through the PBC/PIC, which is the key device in the SLD architecture, the PCM data is transparently switched onto the PCM highways. The PBC will make analog and digital subscriber line boards plug-compatible in a line equipment rack.

There are three leads connecting each subscriber line device and the PBC/PIC: two common clock signals shared among all devices, and a unique bidirectional data lead for each of the eight SIP lines. The Direction signal (DIR) is an 8-kHz clock output from the PBC (master) that serves as a frame sync to the subscriber line devices (slave) as well as a transfer indicator. The data are transferred at a 512-kHz rate, clocked by the Subscriber Clock (SCLK). When DIR is high (first half of the SLD 125 µs frame), four bytes of digital data are transmitted on the SLD bus from the PBC/PIC to the slave (receive direction). During the second half of the frame when DIR is low, four bytes of data are transferred from the slave back to the PBC/PIC (transmit direction).

Channel A and B are 64-kbit/s channels reserved for voice or data to be routed to and from the PCM highways. In an application where one SICOFI is connected to a SIP, voice is received on channel A and transmitted on channel A and B. For a three-party conference, channel B is the third-party voice channel. If two SICOFIs are connected to one SIP, channel A is assigned to one and channel B to the other SICOFI. Conferencing is not possible in this configuration. With digital subscriber line devices the two bytes can be used to carry 64-kbit/s data channels. The third and sixth byte locations are used to transmit and receive control information for programming the slave devices. The last byte in each direction is reserved for signaling data.
Because of the unique requirements of ISDN systems, Siemens developed an interchip interface especially for these applications. As part of their joint definition of ISDN components, the "Group of Four" (ALCATEL, Siemens, Plessey and ITALTEL systems houses) adapted this Siemens Semiconductor interface and suggested some compatible additional features. The resulting IOM-2 interface has become the standard for interchip communication in ISDN terminals, terminal adaptors, network terminations, transmission repeaters and line cards for digital exchange systems.

The IOM-2 interface is a four wire interface with: a bit clock, a frame clock and one data line per direction. It has a flexible data clock. In this way, data transmission requirements are optimized for different applications.
On line cards, a 4096-kHz clock has been selected so that up to eight IOM channels and thus, eight ISDN or 16 analog subscribers can be multiplexed over a single IOM-2 bus. The channel structure of the IOM-2 interface is as follows:

- The first two octets constitute the two 64 kbit/s B channels.
- The third octet is the MONITOR channel. It is used for the exchange of data between devices using the IOM-2 MONITOR channel protocol.
- The fourth octet (control channel) contains
  - two bits for the 16 kbit/s D channel
  - a four-bit command/indication channel, in ISDN applications or
  - a six bit command/indication channel for analog subscriber applications
  - two bits MR and MX for supporting the MONITOR channel protocol.

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**Multiplexed Frame Structure of the IOM®-2 Interface**

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<td>PEB 2054</td>
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<td>SLICOFI®</td>
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<td>DD</td>
<td></td>
<td>ELIC®</td>
</tr>
<tr>
<td>PEB 3065</td>
<td></td>
<td></td>
<td></td>
<td>PEB 20550</td>
</tr>
</tbody>
</table>

FSC: Frame Synchronization  
DCL: Data Clock  
DU: Data Upstream  
DD: Data Downstream
2 Device Overview

2.1 PCM Interface Controller (PBC/PIC/EPIC®)

The key device in the SLD architecture is the Peripheral Board Controller (PBC) PEB 2050. Basically the PBC is a highly intelligent multiplexer/demultiplexer chip which performs the variable time-slot assignment for up to 16 PCM channels and handles the data streams for control and signaling. It constitutes the interface between the subscriber line devices such as codec filter or ISDN communication controller, the PCM lines, the central control unit and the optional onboard microprocessor.

Due to the importance of reliability in system design, the PBC provides a backplane interface with two fully redundant PCM highways. For the exchange of information between a central control unit and the PBC working as a "slave" in a point-to-multipoint configuration, the device supports a subset of the CCITT’s High Level Data Link Control (HDLC) communications protocol so that it can respond to certain HDLC frames without microprocessor intervention or software supervision.

The hardwired implementation of the physical level of the HDLC protocol (e.g. cyclic redundancy check) and of parts of this logical level (e.g. evaluation of HDLC commands and preparation of response packets) in the on-chip HDLC controller permits very high data rates of up to 4 Mbaud via the serial link to the central processor. By using a local standard microprocessor, such as the SAB 8051, it is possible to expand the range of the HDLC protocol to the full X.25 level, while still maintaining procedure handling, buffering and distribution of data packets hardwired in the PBC. Furthermore, the PBC is able, in conjunction with a microprocessor, to take over the "primary" function of a high speed HDLC communication link.

The PBC communicates with the subscriber line devices via a three-wire subscriber line data (SLD) bus based on a ping-pong type of protocol. The SLD bus ensures reduced line board wiring.

To cover a broad range of applications the PBC is adaptable to all standard commercial PCM systems (with 24, 32, 48, 64 channels per frame). Independently of the system clock used, the circuit computes all timing signals required for the standardized SLD bus, thus decoupling the subscriber line devices from the system clock. The PBC is an excellent example of the efficient realization of standard functions through the use of hardwired logic in order to increase realtime processing and speed without loss of flexibility.

A further device for interfacing subscriber line devices with PCM lines is the PCM Interface Controller (PIC) PEB 2052. This CMOS device performs the Time-Slot Assignment (TSA) and the PCM interface functions. It is pin and software-compatible to the PBC PEB 2050, but leaves out the HDLC controller and the hardwired Last Look Logic.
The **Extended PCM Interface Controller (EPIC) PEB 2055** is intended to be used as central PCM processor in the IOM architecture. The CMOS device can be programmed to operate at different data rates between 128 and 8192 kbit/s. The system interface consists of up to four duplex ports with a tristate indication signal for each output line. The configurable interface can be selected to incorporate either four duplex (IOM) or eight bidirectional I/O ports (SLD).

The EPIC can therefore be programmed to communicate either with SLD or with IOM (ISDN Oriented Modular) and IOM®-2 compatible devices. In both cases the device handles the layer-1 functions of buffering the C/I and MONITOR channels for IOM-compatible devices and the feature control and signaling channels for SLD compatible devices. The EPIC can handle up to 32 ISDN subscribers with their 2B + D channel structure or 64 analog subscribers in IOM configuration or up to 16 subscribers in SLD configuration. Since its interfaces can operate at different data rates, the EPIC is an ideal device for data rate adaptation.

Moreover, the EPIC is one of the fundamental building blocks for networks with either central, decentralized or mixed signaling and packet data handling architectures.

The EPIC-2 PEB 2056 is a smaller version of the EPIC. The functions that are performed remain essentially the same but the EPIC-2 PEB 2056 has been optimized for time-slot assignment and switching functions on line cards with up to 8 ISDN or 16 analog subscriber lines.

Siemens Semiconductor therefore offers the optimal solution of PCM Interface Controller for every application.

- **PBC PEB 2050**: for up to eight ISDN and 16 analog subscribers. Especially suitable for powerful PABX.
- **PIC PEB 2052**: for up to eight ISDN and 16 analog subscribers. Ideal for price sensitive systems, e.g. small PABX and public exchanges (CO).
- **EPIC PEB 2055**: for up to 32 ISDN and 64 analog subscribers. Suitable as the central PCM processor in IOM architectures.
- **EPIC-2 PEB 2056**: for up to 8 ISDN or 16 analog subscribers in IOM architectures.

### 2.2 Signal Processing Codec/Filter (SICOFI®/SICOFI®-2)

The Codec/Filter used in the advantageous analog line board architecture is the programmable Signal Processing Codec Filter (SICOFI) PEB 2060, fabricated in advanced CMOS technology. Based on Digital Signal Processing (DSP) methods, in addition to the standard functions of PCM coding and voice-band limitation that any codec filter features, the SICOFI provides a variety of user-programmable filters for impedance matching, 2/4-wire hybrid balancing, analog and digital gain adjustment as well as frequency response correction.
A sophisticated level of performance can therefore be achieved under complete software control. The use of external components or trimming procedures is completely avoided.

For impedance adjustments, the related filter implements a feedback loop to modify the SLIC’s termination impedance. It can handle complex impedances, resulting in optimized return loss for almost all subscriber line conditions. In a similar manner, the hybrid balance filter can be programmed for optimal balance between the transmit and receive side and for minimum echoes.

For accurate adjustment of the gain in receive and transmit directions, four independently programmable filters can vary the level of the analog voice signal in a range of ± 22 dB.

Similar to the level control, the SICOFI contains digital filters in receive and transmit directions, which allow modification of the frequency response characteristics. Further features attractive for the realization of flexible exchange systems are selectable A/µ law coding, three-party conference support, supply voltage supervision, hardware and software reset, power-down mode and on-chip reference voltage. Different loopback modes enable both the line board and the total system to be tested during operation. The SICOFI can hook up directly to virtually any commercial SLIC, because of its flexible signaling interface consisting of ten ports. Three are dedicated to the status of voice transmissions and three to receptions. The remaining four can be programmed individually as either transmit or receive ports.

Due to the fact that the SICOFI needs extended control information, a message-oriented protocol is used for byte transfer via the SLD bus. Two bits in each control byte are used to define three different classes of commands, which contain information about the configuration of the SICOFI, the coefficient exchange and the number of subsequently transmitted data bytes. Per frame and direction, one control byte is transferred between the SICOFI and the PBC. With the appropriate commands, data can be written into or read back from the SICOFI. Selection of one of the two SICOFIs connected to one SLD port is accomplished by an address bit in the feature control byte. For programming the device the information usually is transferred via the HDLC link to the PBC, but all programming can also be done by means of an on-board microprocessor.

There are numerous good reasons why, the world over, major attention is given to digital signal processing methods. Compared to analog filtering, digital processing does not need precision elements, allows much higher accuracy along with precisely predictable transmission behavior including noise. It makes the device less sensitive to parameter fluctuations such as drift with temperature or aging and, moreover, it provides excellent power supply rejection, better testability and crosstalk behavior of the circuit.
In addition, the DSP technique allows a better and easier shrinking of the device and the implementation of codec/filter functions for two and more subscribers on one chip, which is not economic or completely impossible with switched capacitor methods. The next development stage has produced a Dual Channel Codec Filter (SICOFI-2) PEB 2260 that performs the functions of the SICOFI-1 PEB 2060 for two subscribers in one chip.

The sharing of the same digital signal processor part allows a reduced die size per line and leads to reduced line-card costs.

Moreover the CMOS device can be programmed to communicate either with SLD (PBC/PIC) or with IOM-2 (EPIC) compatible PCM interface controller.

As shown with the SICOFI the DSP approach, in a cost-saving and programmable manner, allows the realization of new functions which would be very expensive or impractical in the analog domain.

### Optimized Board Controller Concept

<table>
<thead>
<tr>
<th>Circuit Interface</th>
<th>Controller</th>
<th>Max. Subscriber</th>
<th>Highways</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLD</td>
<td>PEB 2050 (PCB) with HDLC controller</td>
<td>16 analog or 8 ISDN</td>
<td>2 PCM (4 Mbit/s) 1 HDLC</td>
</tr>
<tr>
<td>SLD</td>
<td>PEB 2052 (PIC) low cost PBC for analog line cards with SICOFI</td>
<td>16 analog or 8 ISDN</td>
<td>2 PCM (4 Mbit/s)</td>
</tr>
<tr>
<td>IOM-2/ (SLD)</td>
<td>PEB 2055 (EPIC-1) key device for mixed ISDN/Analog systems</td>
<td>64 analog or 32 ISDN</td>
<td>4 PCM (8 Mbit/s)</td>
</tr>
<tr>
<td>IOM-2</td>
<td>PEB 2056 (EPIC-2) low cost EPIC</td>
<td>16 analog or 8 ISDN</td>
<td>2 PCM (4 Mbit/s)</td>
</tr>
</tbody>
</table>
Optimal Solutions for Every Application
Mixed Use of ISDN and Analog Subscribers with EPIC®
3 Advantages of Siemens Semiconductor Analog Line Card Concept

- Advanced Signal Processing Codec Filter SICOFI family based on DSP technique.
- Matching to different line conditions under complete software control (global line-card solution).
- Modular architecture (IOM-2/SLD compatible).
- Reduced line card wiring, per line structure avoids cross wiring.
- Optimized board controller family.
- Cost optimized design/high volume production.
- Effective application support tools (hardware/software).
Features

- Single chip codec and filter
- Band limitation according to all CCITT and AT & T recommendations
- Digital Signal Processing techniques
- Digital voice transmission
  - PCM encoded (A-law or µ-law)
  - linear (16 bit 2’s complement)
- Programmable digital filters for
  - impedance matching
  - transhybrid balancing
  - gain
  - frequency response correction
- Configurable three pin serial interface
  - 512-kHz-SLD-Bus (e.g. to PEB 2050/52)
  - burst mode with bit rates up to 4 Mbit/s
- Programmable signaling interface to peripherals (e.g. SLIC)
- High performance A/D and D/A conversion
- Programmable analog gain
- Advanced test capabilities
  - three digital loop back modes
  - two analog loop back modes
  - on chip tone generation
- No trimming or adjustments
- No external components
- Variable clock selection
- Signaling expansion possible
- Prepared for three-party conferencing
- Advanced low power 2µCMOS technology
- Power supply + / − 5 V
- Meets or exceeds CCITT and LSSGR recommendations

<table>
<thead>
<tr>
<th>Type</th>
<th>Version</th>
<th>Ordering Code</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>PEB 2060-N</td>
<td>V 4.4</td>
<td>Q67100-H8393</td>
<td>P-LCC-28-R (SMD)</td>
</tr>
<tr>
<td>PEB 2060-P</td>
<td>V 4.4</td>
<td>Q67100-Z170</td>
<td>P-DIP-22</td>
</tr>
</tbody>
</table>
General Description

The Signal Processing Codec Filter (SICOFI) PEB 2060 is a fully integrated PCM codec (coder/decoder) and transmit/receive filter fabricated in advanced CMOS technology for applications in digital telecommunication systems. Based on a digital filter concept, the PEB 2060 provides improved transmission performance and high flexibility. The digital signal processing approach supports software controlled adjustment of the analog behavior, including attractive features such as programmable transhybrid balancing, impedance matching, gain and frequency response correction.

Pin Configuration

(top view)
### Pin Definitions and Functions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Input (I)</th>
<th>Output (O)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-LCC-28-R</td>
<td>P-DIP-22</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>I</td>
<td></td>
<td>+ 5 V power supply</td>
</tr>
<tr>
<td>6</td>
<td>V&lt;sub&gt;ss&lt;/sub&gt;</td>
<td>I</td>
<td></td>
<td>– 5 V power supply</td>
</tr>
<tr>
<td>5</td>
<td>GNDA</td>
<td>I</td>
<td></td>
<td>Ground analog, not internally connected to GNDD. All analog signals are referred to this pin</td>
</tr>
<tr>
<td>7</td>
<td>GNDD</td>
<td>I</td>
<td></td>
<td>Ground digital, not internally connected to GNDA. All digital signals are referred to this pin</td>
</tr>
<tr>
<td>28</td>
<td>VIN</td>
<td>I</td>
<td></td>
<td>Analog voice input to transmit path</td>
</tr>
<tr>
<td>3</td>
<td>VOUT</td>
<td>O</td>
<td></td>
<td>Analog voice output of the received digital voice</td>
</tr>
<tr>
<td>16</td>
<td>SCLK</td>
<td>I</td>
<td></td>
<td>Slave clock</td>
</tr>
<tr>
<td>13</td>
<td>DIR</td>
<td>I</td>
<td></td>
<td>Frame synchronisation signal (direction signal)</td>
</tr>
<tr>
<td>21</td>
<td>SIP</td>
<td>I/O</td>
<td></td>
<td>Serial interface port, bidirectional serial data port</td>
</tr>
<tr>
<td>12</td>
<td>RS</td>
<td></td>
<td></td>
<td>Reset input, RS forces the SICOFI to power down mode and initializes the configuration registers</td>
</tr>
<tr>
<td>23</td>
<td>TEST</td>
<td>I</td>
<td></td>
<td>Test input, normally connected to GNDD</td>
</tr>
<tr>
<td>14</td>
<td>PLL</td>
<td>I</td>
<td></td>
<td>Clock selection (see Appendix A)</td>
</tr>
<tr>
<td>24</td>
<td>SI1</td>
<td>I</td>
<td></td>
<td>Signaling inputs. Data present at SI is sampled and transmitted via the serial interface</td>
</tr>
<tr>
<td>26</td>
<td>SI2</td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>SI3</td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>SO1</td>
<td>O</td>
<td></td>
<td>Signaling outputs. Data received via the serial interface is latched and fed to these outputs</td>
</tr>
<tr>
<td>9</td>
<td>SO2</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>SO3</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>SA</td>
<td>I/O</td>
<td></td>
<td>Programmable I/O signaling pins. Each of these pins may be declared input individually with adequate SICOFI status settings. If 2 SICOFIs are connected to 1 serial interface, pin SA (high/low) assigns voice, control and signaling bytes</td>
</tr>
<tr>
<td>19</td>
<td>SB</td>
<td>I/O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>SC</td>
<td>I/O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>SD</td>
<td>I/O</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SICOFI® Principles

The SICOFI codec filter solution is a highly digital approach utilizing the advantages of digital signal processing such as excellent performance, high flexibility, easy testing, no sensitivity to fabrication and temperature variations, no problems with crosstalk and power supply rejection.

SICOFI® Signal Flow Graph

Transmit Direction

The analog input signal is A/D converted, digitally filtered and transmitted either PCM-encoded or linear. Antialiasing is done with a 2nd order Sallen-Key prefilter (PREFI). The A/D Converter (ADC) is a modified slopeadaptive interpolative sigmadelta modulator with a sampling rate of 128 kHz. Digital downsampling to 8 kHz is done by subsequent decimation filters D1 and D2 together with the PCM bandpass filter (BP).

Receive Direction

The digital input signal is received PCM-encoded or linear, digitally filtered and D/A converted to generate the analog output signal. Digital interpolation up to 128 kHz is done by the PCM lowpass filter (LP) and the interpolation filters I1 and I2. The D/A Converter (DAC) output is fed to the 2nd order Sallen-Key postfilter (POFI).

Programmable Functions

The high flexibility of the SICOFI is based on a variety of user programmable filters, which are analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.
The SICOFI bridges the gap between analog and digital voice signal transmission in modern telecommunication systems. High performance oversampling Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) provide the conversion accuracy required. An analog antialiasing prefilter (PREFI) and smoothing postfilter (POFI) is included. The dedicated on chip Digital Signal Processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM companding. The three pin serial SLD-Bus interface handles digital voice transmission and SICOFI feature control. Specific filter programming is done by downloading coefficients to the coefficient ram (CRAM). The ten pin parallel Signaling Interface provides for a powerful per line SLIC control.
Serial Line Data Interface (SLD Interface)

The exchange of data on the SLD-Bus is based on a bidirectional, bitserial interface consisting of three pins: SIP, DIR and SCLK.

Data is written or read out on the Serial Interface Port SIP under control of the frame synchronization signal DIR with a period of 125 µs\(^1\). The interface clock frequency supplied at the Slave CLock pin SCLK is 512 kHz\(^1\). The rate of the serial data stream on the SIP pin is 512 kbit/s, that is 64 bits per each 8 kHz frame\(^2\).

Starting with the rising edge of DIR, four bytes of information are transferred on the SLD-Bus to the SICOFI, followed by four bytes from the SICOFI to the SLD-Bus. Bit 7 (MSB) is the first bit transferred and bit 0 (LSB) is the last one of each byte.

---

\(^1\) for applications with other clock rates see Appendix A

---

Byte Sequence and Timing at Serial Interface Port SIP
Programming

A message-orientated byte transfer is used, due to the fact that the SICOFI needs extended control information. One control byte per frame and direction is transferred. With the appropriate received commands, data can be written to the SICOFI or read from the SICOFI onto the SLD-bus.

Data transfer to the SICOFI starts with a write command, followed by up to 8 bytes of data. The SICOFI responds to a read command with the requested information, starting at the next transmission period. If no status modification or data exchange is required a NOP byte is transferred (see Programming Procedure).

Control Bytes

The 8-bit control bytes consist of either commands, status information or data. There are three different classes of SICOFI commands:

**NOP**  NO OPERATION:
No status modification or data exchange

**SOP**  STATUS OPERATION:
SICOFI status setting/monitoring

**COP**  COEFFICIENT OPERATION:
Filter coefficient setting/monitoring

The class of command is selected by Bit 2 and 3 of the control byte as shown below. Due to the extended SICOFI feature control facilities, SOP- and COP-commands contain additional information.

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>COP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>0</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

X ... don't care

**NOP Command**

If no status modification of the SICOFI or control data exchange is required, a No Operation Byte NOP is transferred.

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
SOP Command

To modify or evaluate the SICOFI status, the contents of up to four configuration registers CR1, CR2, CR3 and CR4 may be transferred to or from the SICOFI. This is done by a SOP-Command (Status Operation Command).

<table>
<thead>
<tr>
<th>BIT</th>
<th>AD</th>
<th>R/W</th>
<th>PU</th>
<th>TR</th>
<th>0</th>
<th>1</th>
<th>LSEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**AD**  
Address Information  
AD = 0  A-SICOFI addressed  
AD = 1  B-SICOFI addressed  
This bit is evaluated if two SICOFIs are connected to one SLD-port.  
A SICOFI is accessed, if AD is consistent with the level at pin SA  
(see Signaling Byte, Programming Procedure).

**R/W**  
Read/Write Information  
R/W = 0  Write to SICOFI  
R/W = 1  Read from SICOFI  
Enables reading from the SICOFI or writing information to the SICOFI.

**PU**  
Power Up/ Power Down (see also CR3)  
PU = 1  sets the SICOFI to power-up mode (operating)  
PU = 0  resets the SICOFI to power-down (standby mode)

**TR**  
Three Party Conference  
TR = 1  The received voice bytes of channel A and channel B are added (A + B).  
The result is filtered, D/A converted and transferred to analog output VOUT (see also CR3).

**LSEL**  
Length Select Information, identifies the number of subsequent data bytes (see also Programming Procedure)  
LSEL = 0 0  no byte following  
LSEL = 1 1  CR1 is following  
LSEL = 1 0  CR2 and CR1 are following  
LSEL = 0 1  CR4, CR3, CR2 and CR1 are following  
in this case the PU and TR bits are not overwritten.
CR1 Configuration Register 1

This configuration register is used for enabling/disabling the programmable digital filters (DB ... RG) and for accessing testmodes (TM1).

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RZ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TM1</th>
<th>TEST MODES</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>No test mode</td>
</tr>
<tr>
<td>0 0 1</td>
<td>Analog loop back via Z-filter ((H(Z) = 1)^1)</td>
</tr>
<tr>
<td>0 1 0</td>
<td>Disable highpass filter (part of bandpass BP)</td>
</tr>
<tr>
<td>0 1 1</td>
<td>Cut off receive path</td>
</tr>
<tr>
<td>1 0 0</td>
<td>Initialize data ram with 0x0000</td>
</tr>
<tr>
<td>1 1 0</td>
<td>Digital loop back via B-filter ((H(B) = 1)^2)</td>
</tr>
<tr>
<td>1 1 1</td>
<td>Digital loop back via PCM-register(^3)</td>
</tr>
</tbody>
</table>

Other codes are reserved for future use.

---

1) Output of the interpolation filter I1 is set to 0.
   Value of transfer function of the Z-filter is 1 (not programmable).

2) Output of the low pass decimation filter D2 is set to 0.
   Value of transfer function of the B-filter is 1 (not programmable).

3) PCM in = PCM out. This testmode is also available in standby mode.
CR2 Configuration Register 2

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>C</td>
<td>B</td>
<td>A</td>
<td>EL</td>
<td>AM</td>
<td>µ/A</td>
<td>PCS</td>
<td></td>
</tr>
</tbody>
</table>

The first four bits D ... A in this register, program the four bidirectional signaling pins SD ... SA. With two SICOFIs on one SLD-port only pin SD can be used, pin SA is always input in this case and indicates the address of the SICOFI.
SA = 0 : A-SICOFI, SA = 1 : B-SICOFI (see also bit AD in SOP-command).

- **D** Signaling
  - D = 0 SD is output
  - D = 1 SD is input

- **C** Signaling
  - C = 0 SC is output
  - C = 1 SC is input

- **B** Signaling
  - B = 0 SB is output
  - B = 1 SB is input

- **A** Signaling
  - A = 0 SA is output
  - A = 1 SA is input

- **EL** Expansion Logic
  - EL = 0 No expansion logic
  - EL = 1 Expansion logic provided

Signaling expansion logic is only possible with one SICOFI on port (see also Signaling Byte).

- **AM** Address Mode
  - AM = 0 Two SICOFIs on SLD port
  - AM = 1 One SICOFI on SLD port

The SICOFI access to the SLD-Bus voice channel is controlled by AM and TR.

<table>
<thead>
<tr>
<th>AM</th>
<th>TR</th>
<th>SICOFI A</th>
<th>SICOFI B</th>
<th>SICOFI A</th>
<th>SICOFI B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>channel A</td>
<td>channel B</td>
<td>channel A</td>
<td>channel B</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>channel B</td>
<td>channel A</td>
<td>channel B</td>
<td>channel A</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>channel A</td>
<td>------</td>
<td>channel A, B¹</td>
<td>------</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>channel A + B²</td>
<td>------</td>
<td>channel A, B¹</td>
<td>------</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>µ/A</th>
<th>PCM-law</th>
<th>µ/A = 0</th>
<th>A-law</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>µ/A = 1</td>
<td>µ-law (µ255 PCM)</td>
<td></td>
</tr>
</tbody>
</table>

**PCS**

- **B-Filter**
  - PCS = 0 Programmed coefficients
  - PCS = 1 Fixed coefficients

¹) The SICOFI transmits the same byte in channel A and B.
²) Three Party Conference.
CR3 Configuration Register 3

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AGR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LIO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**AGX** Analog Gain Control Transmit-Path

- **AGX** = 0 0 0 dB
- **AGX** = 0 1 6.03 dB amplification
- **AGX** = 1 0 12.06 dB amplification
- **AGX** = 1 1 14 dB amplification

**AGR** Analog Gain Control Receive-Path

- **AGR** = 0 0 0 dB
- **AGR** = 0 1 6.03 dB attenuation
- **AGR** = 1 0 12.06 dB attenuation
- **AGR** = 1 1 14 dB attenuation

**PU** Power Up / Power Down

- **PU** = 0 Power Down (standby)
- **PU** = 1 Power Up (operating)

**TR** Three Party Conference/Reverse Operating Mode (see CR2)

**LIO** Linear Operating Mode (see Serial Interface)

- **LIO** = 0 0 PCM mode
- **LIO** = 0 1 Linear mode 1
- **LIO** = 1 0 Linear mode 2

(Change of linear mode becomes valid in the next DIR-cycle).

---

1) The bits PU and TR may also be overwritten by a SOP Command with LSEL ≠ 0 1 (PU and TR are part of the SOP Command).

With LSEL = 0 1, the bits PU and TR in the SOP Command are ignored.

2) Subsequent to a SOP/COP-read Command the control and signaling information is transmitted instead of linear voice.
CR4 Configuration Register 4

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TM3</td>
<td>0</td>
<td>0</td>
<td>TM4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TEST MODES**

<table>
<thead>
<tr>
<th>TM3</th>
<th>TEST MODES</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>No test mode</td>
</tr>
<tr>
<td>0 0 1</td>
<td>Additional + 6 dB digital gain in transmit direction (GX)</td>
</tr>
<tr>
<td>0 1 1</td>
<td>Additional + 12 dB digital gain in transmit direction (GX)</td>
</tr>
<tr>
<td>1 0 0</td>
<td>Enable on chip tone generation¹)</td>
</tr>
<tr>
<td>1 1 0</td>
<td>Far analog loop back²)</td>
</tr>
</tbody>
</table>

Other codes are reserved for future use.

---

¹) With the R-filter disabled a 2 kHz, 0 dBm0 sinusoidal signal is fed to the input of the receive Lowpass Filter LP (other frequencies see Appendix B).

²) The output of the X-filter is fed to the input of the R-filter (8 kHz, 16 bit linear).
COP Command

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD</td>
<td>R/W</td>
<td>CODE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

With a COP Command coefficients for the programmable filters can be written to the SICOFI coefficient ram or transmitted on the SLD-bus for verification.

**AD**
- Address AD = 0 A-SICOFI addressed
- Information AD = 1 B-SICOFI addressed

This bit is evaluated with two SICOFIs on one SLD-port only. With two SICOFIs on port, a SICOFI is identified, if AD is consistent with the level at pin SA (see Signaling Byte, Programming Procedure).

**R/W**
- Read/Write R/W = 0 Write to SICOFI
- Information R/W = 1 Read from SICOFI

This bit indicates whether filter coefficients are written to the SICOFI or read from the SICOFI.

**CODE**

<table>
<thead>
<tr>
<th>CODE</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 1 1</td>
<td>B-Filter coefficients part 1</td>
<td>(followed by 8 bytes of data)</td>
</tr>
<tr>
<td>0 0 1 0 1 1</td>
<td>B-Filter coefficients part 2</td>
<td>(followed by 8 bytes of data)</td>
</tr>
<tr>
<td>0 1 0 0 1 1</td>
<td>Z-Filter coefficients</td>
<td>(followed by 8 bytes of data)</td>
</tr>
<tr>
<td>0 1 1 0 0 0</td>
<td>B-Filter delay coefficients</td>
<td>(followed by 4 bytes of data)</td>
</tr>
<tr>
<td>1 0 0 0 1 1</td>
<td>X-Filter coefficients</td>
<td>(followed by 8 bytes of data)</td>
</tr>
<tr>
<td>1 0 1 0 1 1</td>
<td>R-Filter coefficients</td>
<td>(followed by 8 bytes of data)</td>
</tr>
<tr>
<td>1 1 0 0 0 0</td>
<td>GX- and GR-Filter coefficients *)</td>
<td>(followed by 4 bytes of data)</td>
</tr>
</tbody>
</table>

Other codes are reserved for future use.

*) In the range – 8 dB to 8 dB gain adjustment is possible in steps ≤ 0.25 dB
**Signaling Byte**

The signaling interface of the SICOIFI consists of 10 pins.

3 transmit signaling inputs: SI1, SI2 and SI3

3 receive signaling outputs: SO1, SO2 and SO3

4 bidirectional programmable signaling pins: SA, SB, SC and SD

Data present at SI1 … SI3 and possibly at some or all of SA … SD (if programmed as inputs) are sampled and transferred serially on SIP onto the SLD-bus. Data received serially on SIP from the SLD-Bus are latched and fed to SO1 … SO3 and possibly to some of SA … SD if programmed as output.

The signaling field format is generally:

**in receive direction:**

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SO1</td>
<td>SO2</td>
<td>SO3</td>
<td>SD</td>
<td>SC</td>
<td>SB</td>
<td>SA</td>
<td>SEL</td>
</tr>
</tbody>
</table>

**in transmit direction:**

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SI1</td>
<td>SI2</td>
<td>SI3</td>
<td>SD</td>
<td>SC</td>
<td>SB</td>
<td>SA</td>
<td>SEL</td>
</tr>
</tbody>
</table>

where SEL is the signaling expansion bit if EL = 1 in CR2.

For the different cases possible, the signaling byte format at SIP is

<table>
<thead>
<tr>
<th>Bit Case</th>
<th>Receive Signaling Byte</th>
<th>Transmit Signaling Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Bit</td>
<td>7</td>
</tr>
<tr>
<td>1</td>
<td>SO1</td>
<td>SO2</td>
</tr>
<tr>
<td>2</td>
<td>SO1</td>
<td>SO2</td>
</tr>
<tr>
<td>3</td>
<td>SO1</td>
<td>SO2</td>
</tr>
<tr>
<td>4</td>
<td>SO1</td>
<td>SO2</td>
</tr>
<tr>
<td>5 A-SIC</td>
<td>SO1</td>
<td>SO2</td>
</tr>
<tr>
<td>B-SIC</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>6 A-SIC</td>
<td>SO1</td>
<td>SO2</td>
</tr>
<tr>
<td>B-SIC</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Z … high impedance, X … don’t care
Cases

1. One SICOFI is connected to one SLD port, EL = 0 (no signaling expansion logic provided); SA … SD are programmed as transmit signaling inputs.

2. One SICOFI connected to one SLD port, EL = 1 (signaling expansion logic provided); SA … SD are programmed as transmit signaling inputs.

3. One SICOFI is connected to one SLD port; EL = 0 (no signaling expansion logic provided); SA … SD are programmed as receive signaling outputs.

4. One SICOFI is connected to one SLD port; EL = 1 (signaling expansion logic provided); SA … SD are programmed as receive signaling outputs.

   If a signaling expansion logic is provided (see case 2 and 4), the signaling bits SA … SD which are programmed as signaling inputs or outputs can be used as additional expansion bits in receive or transmit direction, respectively. As far as SICOFI is concerned, SIP is in a high-impedance (Z) state or "don't care" (Y) state while these bits are transferred.

5. Two SICOFIs are connected to one SLD port; SD is programmed as transmit signaling input.

6. Two SICOFIs are connected to one SLD port; SD is programmed as receive signaling output.

   If two SICOFIs are connected to one SLD port, no signaling expansion logic is possible. SA is programmed as input automatically, and defines the addressed SICOFI:

   \[
   \begin{align*}
   \text{SA} = 0 & : \text{A-SICOFI} \\
   \text{SA} = 1 & : \text{B-SICOFI}.
   \end{align*}
   \]

SB and SC are not usable with two SICOFIs on one SLD port.
## Programming Procedure

The following table shows some control byte sequences. If the SICOFI has to be configured completely during initialization, up to 60 bytes will be transferred.

<table>
<thead>
<tr>
<th>DIR</th>
<th>Receive</th>
<th>Transmit</th>
<th>Receive</th>
<th>Transmit</th>
<th>Receive</th>
<th>Transmit</th>
<th>Receive</th>
<th>Transmit</th>
<th>Receive</th>
<th>Transmit</th>
<th>Receive</th>
</tr>
</thead>
<tbody>
<tr>
<td>ITD02445</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**DIR**

- **No Operation**
  - LSEL = 00: |NOP|NOP|NOP|NOP|NOP|NOP|NOP|NOP|NOP|
  - LSEL = 11: SOP|NOP|CR1|NOP|
  - LSEL = 10: SOP|NOP|CR2|NOP|CR1|NOP|
  - LSEL = 01: SOP|NOP|CR4|NOP|CR3|NOP|CR2|NOP|CR1|NOP|

**SOP Read**

- LSEL = 00: |SOP|NOP|
- LSEL = 11: SOP|CR1|
- LSEL = 10: SOP|CR2|X|CR1|
- LSEL = 01: SOP|CR4|X|CR3|X|CR2|X|CR1|

**COP Write**

- 4 Bytes: |COP|NOP|DB4|NOP|DB3|NOP|DB2|NOP|DB1|NOP|
- 8 Bytes: |COP|NOP|DB8|NOP|DB7|NOP|DB1|NOP|DB1|NOP|

**COP Read**

- 4 Bytes: |COP|DB4|X|DB3|DB1|X|CR2|X|CR1|
- 8 Bytes: |COP|DB8|X|DB7|DB1|X|CR2|X|CR1|

X ... don't care

DB1, DB2 ... DB8 ... coefficient Data Byte 1 ... 8
Operating Modes

Basic Setting

Upon initial application of $V_{DD}$ or resetting pin RS to "1" while operating, the SICOFI enters a basic setting mode. Basic setting means, that the SICOFI configuration registers CR1 … CR4 are initialized. All CR1 bits are set to "0" (all programmable filters are disabled except the B-Filter where fixed coefficients are used, no test mode); CR2 is set to "1" (SA … SD are inputs, signaling expansion logic is provided, one SICOFI on SLD-port, μ-law chosen and fixed B-Filter coefficients used). All CR3 and CR4 bits are reset to "0" (no additional amplification or attenuation, no linear mode, power down, no test mode). Receive signaling registers are cleared. SIP is in high-impedance state, the analog output VOUT and the receive signaling outputs SO1 … SO3 are forced to ground.

The serial interface is active to receive commands starting with the next 8-kHz SLD-Bus frame. The serial interface port SIP remains in high-impedance state until CR2 has been defined. If two SICOFIs are connected to one SLD port, both SICOFI's get the same SOP and CR2 information during initialization. The subsequent CR1 byte is assigned to the addressed SICOFI only. If the two SICOFI's need different CR2 information, the SOP-CR2 sequence has to be provided once again (each SICOFI knows its address now).

If any voltage is applied to any input before initial application of $V_{DD}$, the SICOFI may not enter the Basic Setting Mode. In this case it is necessary either to reset the SICOFI via the RS Pin or to initialize the configuration registers CR1, CR2, CR3, CR4.

Standby Mode

Upon reception of a SOP command to load CR2 from the basic setting, the SICOFI enters the standby mode (basic setting replaced by individual CR2). Being in the operating mode, the SICOFI is reset to standby mode with a Power-Up bit $PU = 0$ (in CR3 or in the SOP-command directly). The serial interface is active to receive and transmit new commands and data.

Operating Mode

From the standby mode, the operating mode is entered upon recognition of a Power-Up bit $PU = 1$ (in CR3 or in the SOP-command directly).
Transmission Characteristics

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing: B; impedance matching: Z; frequency-response correction: X, R) needs a complete knowledge of the SICOFLs analog environment. Unless otherwise stated, the transmission characteristics are guaranteed within the test condition below.

\[ T_A = 0 \, ^\circ\text{C} \text{ to } 70 \, ^\circ\text{C}; \ V_{DD} = 5 \, \text{V} \pm 5 \, \text{V}; \ V_{SS} = -5 \, \text{V} \pm 5 \, \text{V}; \ GNDA = GNDD = 0 \, \text{V} \]
\[ R_L > 10 \, \text{k}\Omega; \ C_L < 50 \, \text{pF}; \ H(Z) = H(B) = 0; \ H(X) = H(R) = 1; \]
\[ GX = 0 \text{ to } 8 \, \text{dB}; \ GR = 0 \text{ to } -8 \, \text{dB}; \ AGR = 0, 6.03, 12.06, 14 \, \text{dB}; \ AGX = 0, -6.03, -12.06, -14 \, \text{dB}; \]
\[ f = 1000 \, \text{Hz}; \ 0 \, \text{dBm0}; \ \text{A-law or } \mu\text{-law}; \]

A 0 dBm0 signal is equivalent to 1.5763 [1.5710] Vrms. A 3.14 [3.17] dBm0 signal is equivalent to 2.263 Vrms which corresponds to the overload point of 3.2 V (A-law, [\mu\text{-law}]).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (either value)(^1)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain absolute (AGR = AGX = 0)</td>
<td>G</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_A = 25 , ^\circ\text{C}, \ V_{DD} = 5 , \text{V}, \ V_{SS} = -5 , \text{V} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_A = 0\text{ to }70 , ^\circ\text{C}, \ V_{DD} = 5 , \text{V} \pm 5 % , \ V_{SS} = -5 , \text{V} \pm 5 % )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain absolute (AGR = 0 to 14 dB, AGX = 0 to 14 dB)</td>
<td>G</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_A = 0\text{ to }70 , ^\circ\text{C}, \ V_{DD} = 5 , \text{V} \pm 5 % , \ V_{SS} = -5 , \text{V} \pm 5 % )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total harmonic distortion, 0 dBm0; ( f = 300 , \text{Hz} \text{ to } 3400 , \text{Hz} )</td>
<td>THD</td>
<td>-50</td>
<td>-44</td>
</tr>
<tr>
<td>Intermodulation ( 2/1 - j/2^2 )</td>
<td>IMD</td>
<td>-42</td>
<td>-56</td>
</tr>
<tr>
<td></td>
<td>( 2/1 - j/2^3 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Crosstalk 0 dBm0; ( f = 300 , \text{Hz} \text{ to } 3400 , \text{Hz} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transmit to receive</td>
<td>CT(_{XR})</td>
<td>-85</td>
<td>-80</td>
</tr>
<tr>
<td>Receive to transmit</td>
<td>CT(_{RX})</td>
<td>-85</td>
<td>-80</td>
</tr>
<tr>
<td>Idle channel noise, transmit, psophometric, A-law</td>
<td>( V_{IN} = 0 , \text{V} )</td>
<td>( N_{TP} )</td>
<td>-67.4</td>
</tr>
<tr>
<td>transmit, C-message, ( \mu\text{-law} )</td>
<td>( V_{IN} = 0 , \text{V} )</td>
<td>( N_{TC} )</td>
<td>17.5</td>
</tr>
<tr>
<td>receive, psophometric, A-law</td>
<td>idle code + 0</td>
<td>( N_{RP} )</td>
<td>-82</td>
</tr>
<tr>
<td>receive, C-message, ( \mu\text{-law} )</td>
<td>idle code + 0</td>
<td>( N_{RC} )</td>
<td>8</td>
</tr>
</tbody>
</table>

\(^1\) \( R_L = 300 \, \Omega \) causes an additional attenuation in the range between -0.1 to 0 dB.

\(^2\) Equal input levels in the range between -4 dBm0 and -21 dBm0; different frequencies in the range between 300 Hz and 3400 Hz.

\(^3\) Input level -9 dBm0, frequency range 300 Hz to 3400 Hz and -23 dBm0, 50 Hz.
Attenuation Distortion

Attenuation deviations stay within the limits in the figures below.

**Receive:** Reference frequency 1 kHz, input signal level 0 dBm0

**Transmit:** Reference frequency 1 kHz, input signal level 0 dBm0
Group Delay

Maximum delays for operating the SICOFI with $H(B) = H(Z) = 0$ and $H(R) = H(X) = 1$, including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group delay deviations stay within the limits in the figures below.

**Group Delay Absolute Values:** Input signal level 0 dBm0

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmit Delay</td>
<td>$D_{XA}$</td>
<td>300 $\mu$s</td>
<td>$f = 1.4$ kHz</td>
<td></td>
</tr>
<tr>
<td>Receive Delay</td>
<td>$D_{RA}$</td>
<td>240 $\mu$s</td>
<td>$f = 300$ Hz</td>
<td></td>
</tr>
</tbody>
</table>

**Group Delay Distortion:** Input signal level 0 dBm0, reference frequency = 1.4 kHz
Out-of-Band Signals at Analog Input
With an out-of-band sine wave signal with frequency $f$ and level A applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below level A.

Out-of-Band Signals at Analog Output
With a 0 dBm0 sine wave of frequency $f$ applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.
Gain Tracking (Receive and Transmit)

The gain deviations stay within the limits in the figures below

**Gain Tracking**: Measured with noise signal according to CCITT recommendations, reference level is $-10 \text{ dBm}_0$, $AGX = AGR = 0$

**Gain Tracking**: Measured with sine wave in the range 700 to 1100 Hz, reference level is $-10 \text{ dBm}_0$, $AGX = AGR = 0$
Total Distortion
The signal-to-distortion ratio exceeds the limits in the following figures.

**Receive:** Measured with noise signal according to CCITT recommendations

**Transmit:** Measured with noise signal according to CCITT recommendations
The signal to distortion ratio exceeds the limits in the following figures.

**Receive & Transmit:** Measured with sine wave in the range 700 to 1100 Hz excluding submultiples of 8 kHz

**Signal to Total Distortion CCITT Noise Signal Digital-Digital (A-law and μ-law)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Input Level</th>
<th>Unit</th>
<th>Total Distortion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Loop Back via B-Filter or Digital Loop Back via Analog port</td>
<td>0</td>
<td>dBm0</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>−30</td>
<td>dBm0</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>−40</td>
<td>dBm0</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>−45</td>
<td>dBm0</td>
<td>20</td>
</tr>
</tbody>
</table>

**Parameter:**

- Total Distortion
  - CB: 30 dB, 48 dB
  - PN: 20 dB, 31 dB

**Signal to Noise (S/N) (A-law and μ-law)**

**Digital Loop Back via B-Filter or Digital Loop Back via Analog port**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Input Level</th>
<th>Unit</th>
<th>Total Distortion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Loop Back via B-Filter or Digital Loop Back via Analog port</td>
<td>0</td>
<td>dBm0</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>−30</td>
<td>dBm0</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>−40</td>
<td>dBm0</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>−45</td>
<td>dBm0</td>
<td>20</td>
</tr>
</tbody>
</table>
Transhybrid Loss

The quality of transhybrid-balancing is very sensitive to deviations in gain and group delay – deviations inherent to the SICOFI A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP’s etc.)

The SICOFI transhybrid loss is measured in the following way: A sine wave signal with level 0 dBm0 and a frequency in the range of 300 – 3400 Hz is applied to the digital input. The resulting analog output signal at pin VOUT is directly connected to VIN, e.g. with the SICOFI testmode "Digital Loop Back via Analog Port" (see CR4). The programmable filters R, GR, X, GX and Z are disabled, the balancing filter B is enabled with coefficients optimized for this configuration ($V_{OUT} = V_{IN}$).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below.

B-filter coefficients recommended for transhybrid loss measurement with $V_{OUT} = V_{IN}$

<table>
<thead>
<tr>
<th>COP-Write</th>
<th>Coefficients</th>
</tr>
</thead>
<tbody>
<tr>
<td>B-filter part 1</td>
<td>(83) FD 29 FB 38 A1 A0 3C 42</td>
</tr>
<tr>
<td>B-filter part 2</td>
<td>(8B) 00 AF 62 2B CF D1 CA A4</td>
</tr>
<tr>
<td>B-filter delay</td>
<td>(98) 19 19 11 19</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transhybrid loss at 500 Hz</td>
<td>$THL_{500}$</td>
<td>33 min. 45 typ.</td>
<td>dB</td>
<td>$T_A = 25 ^\circ C$, $V_{DD} = 5 \text{ V}$, $V_{SS} = -5 \text{ V}$, $AGR = AGX = 0 \text{ dB}$</td>
</tr>
<tr>
<td>Transhybrid loss at 2500 Hz</td>
<td>$THL_{2500}$</td>
<td>29 min. 40 typ.</td>
<td>dB</td>
<td>$T_A = 0$ to $70 ^\circ C$, $V_{DD} = 5 \text{ V} \pm 5 %$, $V_{SS} = 5 \text{ V} \pm 5 %$, $AGR = AGX = 0 \text{ dB}$</td>
</tr>
<tr>
<td>Transhybrid loss at 3000 Hz</td>
<td>$THL_{3000}$</td>
<td>27 min. 35 typ.</td>
<td>dB</td>
<td>$T_A = 0$ to $70 ^\circ C$, $V_{DD} = 5 \text{ V} \pm 5 %$, $V_{SS} = -5 \text{ V} \pm 5 %$, $AGR = AGX = 6.03$, 12.06, 14.00 dB</td>
</tr>
</tbody>
</table>

 zag
### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ referred to GNDD</td>
<td>$V_{DD}$</td>
<td>±0.3 5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{SS}$ referred to GNDD</td>
<td>$V_{SS}$</td>
<td>±5.5 0.3</td>
<td>V</td>
</tr>
<tr>
<td>GNDA to GNDD</td>
<td></td>
<td>±0.6 0.6</td>
<td>V</td>
</tr>
<tr>
<td>Analog input and output voltage referred to $V_{DD} = 5, \text{V}$, $V_{SS} = -5, \text{V}$</td>
<td>$V_{IN}$</td>
<td>±10.3 0.3</td>
<td>V</td>
</tr>
<tr>
<td>referred to $V_{DD} = 5, \text{V}$, $V_{SS} = 0, \text{V}$</td>
<td>$V_{IN}$</td>
<td>±0.3 10.3</td>
<td>V</td>
</tr>
<tr>
<td>All digital input voltages referred to GNDD = 0 V, $V_{DD} = 5, \text{V}$</td>
<td>$V_{IN}$</td>
<td>±0.3 5.3</td>
<td>V</td>
</tr>
<tr>
<td>referred to $V_{DD} = 5, \text{V}$, GNDD = 0 V</td>
<td>$V_{IN}$</td>
<td>±5.3 0.3</td>
<td>V</td>
</tr>
<tr>
<td>DC input and output current at any input or output pin</td>
<td>$I_{DC}$</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{slg}$</td>
<td>±60 125</td>
<td>°C</td>
</tr>
<tr>
<td>Ambient temperature under bias</td>
<td>$T_{A}$</td>
<td>±10 80</td>
<td>°C</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>$P_D$</td>
<td>1</td>
<td>W</td>
</tr>
</tbody>
</table>

### Operating Range

$T_A = 0$ to 70 °C; $V_{DD} = 5\, \text{V} \pm 5\%$; $V_{SS} = -5\, \text{V} \pm 5\%$; GNDD = 0 V; GNDA = 0 V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ supply current stand by operating</td>
<td>$I_{DD}$</td>
<td>2.1 8</td>
<td>mA</td>
<td>1 kHz 80 mVrms ripple</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 12</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{SS}$ supply current stand by operating</td>
<td>$I_{SS}$</td>
<td>1.7 5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 8</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Power supply rejection (of either supply/direction)</td>
<td>$PSRR$</td>
<td>30 44</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Power dissipation stand by Power dissipation operating</td>
<td>$P_{Ds}$</td>
<td>20 70</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$P_{Do}$</td>
<td>37 105</td>
<td>mW</td>
<td></td>
</tr>
</tbody>
</table>
### Electrical Characteristics

#### Digital Interface

$T_A = 0 \text{ to } 70 \, ^\circ\mathrm{C}; \, V_{\text{DD}} = 5 \, \text{V} \pm 5\% ; \, V_{\text{SS}} = -5 \, \text{V} \pm 5\% ; \, GNDD = 0 \, \text{V} ; \, GNDA = 0 \, \text{V}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>L-input voltage</td>
<td>$V_{IL}$</td>
<td>$–0.3$</td>
<td>$0.8$</td>
<td>V</td>
</tr>
<tr>
<td>H-input voltage</td>
<td>$V_{IH}$</td>
<td>$2.0$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>L-output voltage</td>
<td>$V_{OL}$</td>
<td>$0.45$</td>
<td></td>
<td>V $I_0 = –2 , \text{mA}$</td>
</tr>
<tr>
<td>H-output voltage</td>
<td>$V_{OH}$</td>
<td>$2.4$</td>
<td></td>
<td>V $I_0 = 400 , \mu\text{A}$</td>
</tr>
<tr>
<td>Input leakage current</td>
<td>$I_{IL}$</td>
<td>$±1$</td>
<td></td>
<td>$–0.3 \leq V_{\text{IN}} \leq V_{\text{DD}}$</td>
</tr>
</tbody>
</table>

#### Analog Interface

$T_A = 0 \text{ to } 70 \, ^\circ\mathrm{C}; \, V_{\text{DD}} = 5 \, \text{V} \pm 5\% ; \, V_{\text{SS}} = -5 \, \text{V} \pm 5\% ; \, GNDD = 0 \, \text{V} ; \, GNDA = 0 \, \text{V}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog input resistance</td>
<td>$R_I$</td>
<td>$10$</td>
<td></td>
<td>MΩ</td>
</tr>
<tr>
<td>Analog output resistance</td>
<td>$R_O$</td>
<td>$10$</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>$V_{IO}$</td>
<td>$±50$</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Output offset voltage</td>
<td>$V_{OO}$</td>
<td>$±50$</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>$V_{IR}$</td>
<td>$±3.2$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output voltage range</td>
<td>$V_{OR}$</td>
<td>$±3.1$</td>
<td></td>
<td>V $R_L \geq 300 , \Omega$; $C_L \leq 50 , \text{pF}$</td>
</tr>
</tbody>
</table>
SIP Interface Timing (SLD-Bus)

Switching Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Period SCLK</td>
<td>$t_{SCLK}$</td>
<td>1/512 kHz</td>
<td></td>
</tr>
<tr>
<td>Duty cycle</td>
<td></td>
<td>20 50 80</td>
<td>%</td>
</tr>
<tr>
<td>Period DIR</td>
<td>$t_{DIR}$</td>
<td>125</td>
<td>µs</td>
</tr>
<tr>
<td>DIR setup time</td>
<td>$t_{DIR \times S}$</td>
<td>20 0 – 80</td>
<td>ns</td>
</tr>
<tr>
<td>DIR hold time</td>
<td>$t_{DIR \times H}$</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>SIP data in setup time</td>
<td>$t_{DIN \times S}$</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>SIP data in hold time</td>
<td>$t_{DIN \times H}$</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>SIP data out delay</td>
<td>$t_{dOUT}$</td>
<td>150 250</td>
<td>ns</td>
</tr>
<tr>
<td>SIP data out high impedance delay vs. SCLK</td>
<td>$t_{dHZ}$</td>
<td>50 70</td>
<td>ns</td>
</tr>
</tbody>
</table>
Signaling Interface Timing

Switching Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay signaling out vs. SCLK</td>
<td>$t_{dSIGOUT}$</td>
<td>250</td>
<td>350</td>
</tr>
<tr>
<td>Delay signaling high impedance vs. SCLK</td>
<td>$t_{dSIGZ}$</td>
<td>150</td>
<td>200</td>
</tr>
<tr>
<td>SIG in setup time</td>
<td>$t_{SIGIN \times S}$</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>SIG in hold time</td>
<td>$t_{SIGIN \times H}$</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Reset pulse width</td>
<td>$t_{RES}$</td>
<td>500</td>
<td></td>
</tr>
</tbody>
</table>

1) Pins SO1 ... SO3; Pins SA ... SD as output
2) Pins SI1 ... SI3; Pins SA ... SD as input
3) SICOFI is ready to accept SOP/COP commands in the next DIR Cycle. Spikes shorter than 244 ns will be ignored.
Appendix A

Specific Interface Types

The SICOFI can be used with three different SLD-bus type interfaces. A specific interface type is selected with three pins: TEST, SI3 and PLL.

<table>
<thead>
<tr>
<th>TEST</th>
<th>SI3</th>
<th>PLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

1) SLD-Bus Interface

<table>
<thead>
<tr>
<th>TEST</th>
<th>SI3</th>
<th>PLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

1) SI3 cannot be used as Signaling Pin

2) SLD-Bus Interface with Variable Clock Frequencies

1) 4096-kHz Masterclock MCLK is generated from 512-kHz SCLK by on chip PLL
2) Maximum MCLK-frequency = 8 MHz
3) Burst Mode Interface

<table>
<thead>
<tr>
<th>TEST</th>
<th>SI3 (^1)</th>
<th>PLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\(^1\) SI3 cannot be used as Signaling Pin

Maximum MCLK-frequency = 8 MHz
In burst-mode 8- or 16-bit bursts are received or transmitted, depending on the linear mode selected (see field LIO in CR3).

**Detail A**

A … voice A  C … control  
B … voice B  S … signaling  
MSB … bit 15-8 of linear in- or output  
LSB … bit 7-0 of linear in- or output
Appendix B

On Chip Tone Generation

By setting field TM3 in CR4 to '100' the on-chip tone generator is activated with a fixed frequency of 2 kHz. The frequency $f_{\text{TONE}}$ may be programmed via the R-filter coefficients (R-filter enabled) in the range of 0 to 4 kHz. The gain may be adjusted with the programmable GR-filter.

The trapezoidal tone generation algorithm used, provides for a harmonic distortion better than 27 dB.

Calculation of the R-filter Coefficients:

$$f_{\text{TONE}} = 8192 \times \text{INC} / f_{\text{MCLK}} \text{ with } f_{\text{MCLK}}, f_{\text{TONE}} \text{ [kHz]}$$

$$\text{INC} = (1 + S_{R1} \times 2^{-\text{EXP}R1}) \times (1 + S_{R2} \times 2^{-\text{EXP}R2}) \times (1 + S_{R3} \times 2^{-\text{EXP}R3}) \times (\ldots (1 + S_{R9} \times 2^{-\text{EXP}R9})\ldots)$$

$S \ldots \text{SIGN}, \text{EXP} \ldots \text{EXPONENT}$

$$A_{1} := \text{INC}$$

FOR $i := 1$ TO 9 DO

$$\text{FIND } S_{i}, \text{EXP}_{i}: \text{FOR } (|A_{i} - S_{i} \times 2^{-\text{EXP}i}|) = \text{MIN}; S_{i} \in (-1, 1), \text{EXP}_{i} \in (0 \ldots 7)$$

$$A_{i+1} := (A_{i} / S_{i} \times 2^{-\text{EXP}i}) - 1$$

$$R_{i} := [( -S_{i} +1)/2), \text{BIN} (\text{EXP}_{i})] \text{ (to be transferred to the SICOFI)}$$

NEXT $i$

Programming Byte Sequence for Selected Frequencies

<table>
<thead>
<tr>
<th>Coefficients</th>
<th>2000</th>
<th>1000</th>
<th>800</th>
<th>697</th>
<th>770</th>
<th>852</th>
<th>941</th>
<th>1209</th>
<th>1336</th>
<th>1477</th>
<th>1633</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>R1</td>
<td>X</td>
<td>00</td>
<td>10</td>
<td>10</td>
<td>20</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>00</td>
</tr>
<tr>
<td>R3</td>
<td>R2</td>
<td>8F</td>
<td>8F</td>
<td>AA</td>
<td>A1</td>
<td>CA</td>
<td>3B</td>
<td>CC</td>
<td>B2</td>
<td>22</td>
<td>D1</td>
</tr>
<tr>
<td>R5</td>
<td>R4</td>
<td>8F</td>
<td>8F</td>
<td>AA</td>
<td>2B</td>
<td>32</td>
<td>C1</td>
<td>BB</td>
<td>22</td>
<td>A1</td>
<td>C1</td>
</tr>
<tr>
<td>R7</td>
<td>R6</td>
<td>8F</td>
<td>8F</td>
<td>AA</td>
<td>4B</td>
<td>2D</td>
<td>BB</td>
<td>12</td>
<td>5F</td>
<td>5F</td>
<td>BB</td>
</tr>
<tr>
<td>R9</td>
<td>R8</td>
<td>8F</td>
<td>8F</td>
<td>AA</td>
<td>B1</td>
<td>B3</td>
<td>12</td>
<td>DA</td>
<td>8F</td>
<td>1B</td>
<td>12</td>
</tr>
</tbody>
</table>

$^1$ 2B for SICOFI A, AB for SICOFI B.
Dual Channel Codec Filter (SICOFI®-2)

PEB 2260
PEF 2260

Features

● Dual channel single chip codec and filter
● Band limitation according to all CCITT and AT&T recommendations
● Digital signal processing techniques
● PCM encoded digital voice transmission (A-law or µ-law)
● Programmable digital filters for
  – impedance matching
  – transhybrid balancing
  – gain
  – frequency response correction
● Two digital Interfaces
  – three pin serial SLD Interface (e.g. to PEB 2050/52)
  – four pin serial IOM®-2 Interface with two different clock-frequencies and time-slot assignment (e.g. to PEB 2055/56)
● Programmable signaling interface to peripherals (e.g. SLIC)
● High performance A/D and D/A conversion
● Programmable analog gain adjustment
● Advanced test capabilities
  – three digital loop back modes
  – two analog loop back modes
  – two programmable tone generators
● No trimming or adjustments
● No external components
● Advanced low power 2µCMOS technology
● Power supply + / – 5 V
● Meets or exceeds CCITT and LSSGR recommendations
● Two types are available:
  – PEB 2260 with standard temperature range 0...70°C
  – PEF 2260 with extended temperature range -40...85°C

<table>
<thead>
<tr>
<th>Type</th>
<th>Version</th>
<th>Ordering Code</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>PEB 2260-N</td>
<td>V 2.0</td>
<td>Q67100-H6191</td>
<td>P-LCC-28-R (SMD)</td>
</tr>
<tr>
<td>PEF 2260-N</td>
<td>V 2.0</td>
<td>Q67100-H6261</td>
<td>P-LCC-28-R (SMD)</td>
</tr>
</tbody>
</table>
General Description

The Dual Channel Codec Filter PEB 2260 (SICOFI®-2) is a fully integrated PCM codec and filter fabricated in low power 2µCMOS technology for applications in digital communication systems. Based on an advanced digital filter concept, the PEB 2260 provides excellent transmission performance and high flexibility. The digital signal processing approach includes attractive programmable features such as transhybrid balancing, impedance matching, gain and frequency response correction.

Pin Configuration for SLD Mode
(top view)

Pin Configuration for IOM®-2 Mode
(top view)
### Pin Definitions and Functions for SLD Interface Mode

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Input (I)</th>
<th>Output (O)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>$V_{dd}$</td>
<td>I</td>
<td></td>
<td>+5 V power supply</td>
</tr>
<tr>
<td>8</td>
<td>$V_{ss}$</td>
<td>I</td>
<td></td>
<td>–5 V power supply</td>
</tr>
<tr>
<td>24</td>
<td>GNDD</td>
<td>I</td>
<td></td>
<td>Ground digital. Not internally connected to GNDA or GNDB. All digital signals are referred to this pin</td>
</tr>
<tr>
<td>1</td>
<td>GNDA</td>
<td>I</td>
<td></td>
<td>Ground analog channel A. Not internally connected to GNDD or GNDB. All channel A analog signals are referred to this pin</td>
</tr>
<tr>
<td>15</td>
<td>GNDB</td>
<td>I</td>
<td></td>
<td>Ground analog channel B. Not internally connected to GNDD or GNDA. All channel B analog signals are referred to this pin</td>
</tr>
<tr>
<td>27</td>
<td>VINA</td>
<td>I</td>
<td></td>
<td>Channel A analog voice input</td>
</tr>
<tr>
<td>3</td>
<td>VOUTA</td>
<td>O</td>
<td></td>
<td>Channel A analog voice output</td>
</tr>
<tr>
<td>17</td>
<td>VINB</td>
<td>I</td>
<td></td>
<td>Channel B analog voice input</td>
</tr>
<tr>
<td>13</td>
<td>VOUTB</td>
<td>O</td>
<td></td>
<td>Channel B analog voice output</td>
</tr>
<tr>
<td>25</td>
<td>MODE</td>
<td>I</td>
<td></td>
<td>Operating mode selection, SLD or IOM-2 Interface: connected to ‘0’ for SLD interface mode</td>
</tr>
<tr>
<td>21</td>
<td>SCLK</td>
<td>I</td>
<td></td>
<td>Slave clock, 512 kHz</td>
</tr>
<tr>
<td>20</td>
<td>DIR</td>
<td>I</td>
<td></td>
<td>Direction Signal, 8-kHz frame synchronisation</td>
</tr>
<tr>
<td>19</td>
<td>SIP</td>
<td>I/O</td>
<td></td>
<td>Serial interface port, bidirectional serial data port</td>
</tr>
<tr>
<td>23</td>
<td>RS</td>
<td>I</td>
<td></td>
<td>Reset input, RS forces the SICOFI-2 to basic setting mode</td>
</tr>
<tr>
<td>2</td>
<td>SI1A</td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>SI2A</td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>SI3A</td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>SI1B</td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>SI2B</td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>SI3B</td>
<td>I</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Signaling inputs: data present at SI1A ... SI3B are sampled and transmitted via the serial interface
### Pin Definitions and Functions for SLD Interface Mode (continued)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Input (I)</th>
<th>Output (O)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>SO1A</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>SO2A</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>SO3A</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>SO1B</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>SO2B</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>SO3B</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>SBA</td>
<td>I/O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>SBB</td>
<td>I/O</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Bidirectional signaling pins: SBA, SBB pins may be programmed as input or output individually with adequate SICOFI-2 status settings.*

*Signaling outputs: data received via the serial interface are latched and fed to SO1A ... SO3B.*

### Pin Definitions and Functions for IOM®2 Interface Mode

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Input (I)</th>
<th>Output (O)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>(V_{DD})</td>
<td>I</td>
<td></td>
<td>+ 5 V power supply</td>
</tr>
<tr>
<td>8</td>
<td>(V_{SS})</td>
<td>I</td>
<td></td>
<td>– 5 V power supply</td>
</tr>
<tr>
<td>24</td>
<td>GNDD</td>
<td>I</td>
<td></td>
<td>Ground digital. Not internally connected to GNDA or GNDB. All digital signals are referred to this pin</td>
</tr>
<tr>
<td>1</td>
<td>GNDA</td>
<td>I</td>
<td></td>
<td>Ground analog channel A. Not internally connected to GNDD or GNDB. All channel A analog signals are referred to this pin</td>
</tr>
<tr>
<td>15</td>
<td>GNDB</td>
<td>I</td>
<td></td>
<td>Ground analog channel B. Not internally connected to GNDD or GNDA. All channel B analog signals are referred to this pin</td>
</tr>
<tr>
<td>27</td>
<td>VINA</td>
<td>I</td>
<td></td>
<td>Channel A analog voice input</td>
</tr>
<tr>
<td>3</td>
<td>VOUTA</td>
<td>O</td>
<td></td>
<td>Channel A analog voice output</td>
</tr>
<tr>
<td>17</td>
<td>VINB</td>
<td>I</td>
<td></td>
<td>Channel B analog voice input</td>
</tr>
<tr>
<td>13</td>
<td>VOUTB</td>
<td>O</td>
<td></td>
<td>Channel B analog voice output</td>
</tr>
<tr>
<td>25</td>
<td>MODE</td>
<td>I</td>
<td></td>
<td>Operating mode selection, SLD or IOM-2 Interface: connected to '1' for IOM-2 interface mode</td>
</tr>
</tbody>
</table>
Pin Definitions and Functions for IOM®2 Interface Mode (continued)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Input (I)</th>
<th>Output (O)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>DCL</td>
<td>I</td>
<td></td>
<td>Data clock, 512 kHz or 4096 kHz</td>
</tr>
<tr>
<td>20</td>
<td>FSC</td>
<td>I</td>
<td></td>
<td>Frame synchronisation clock, 8 kHz</td>
</tr>
<tr>
<td>19</td>
<td>DU</td>
<td>O</td>
<td></td>
<td>Data upstream</td>
</tr>
<tr>
<td>18</td>
<td>DD</td>
<td>I</td>
<td></td>
<td>Data downstream</td>
</tr>
<tr>
<td>23</td>
<td>RS</td>
<td>I</td>
<td></td>
<td>Reset input, RS forces the SICOFI-2 to basic setting mode</td>
</tr>
<tr>
<td>28</td>
<td>I1A</td>
<td>I</td>
<td></td>
<td>Indication inputs: data present at I1A ... I1B are sampled and transmitted via the serial interface</td>
</tr>
<tr>
<td>16</td>
<td>I1B</td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>C1A</td>
<td>O</td>
<td></td>
<td>Command outputs: data received via the serial interface are latched and fed to C1A ... C3A and C1B ... C2B</td>
</tr>
<tr>
<td>6</td>
<td>C2A</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>C3A</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>C1B</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>C2B</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>CI1A</td>
<td>I/O</td>
<td></td>
<td>Bidirectional command/indication pins: CI1A ... CI2B may be programmed as input or output individually with adequate SICOFI-2 status settings</td>
</tr>
<tr>
<td>4</td>
<td>CI2A</td>
<td>I/O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>CI1B</td>
<td>I/O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>CI2B</td>
<td>I/O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>TS1</td>
<td>I</td>
<td></td>
<td>Time-slot selection pins 1 ... 2 with ternary logic</td>
</tr>
<tr>
<td>9</td>
<td>TS2</td>
<td>I</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SICOFI®-2 Principles

The SICOFI-2 codec filter solution is a highly digital approach utilizing the advantages of digital signal processing such as excellent performance, high flexibility, easy testing, no sensitivity to fabrication and temperature variations, no problems with crosstalk and power supply rejection.

SICOFI®-2 Signal Flow Graph (for either channel)

Transmit Direction

The analog input signal is A/D converted, digitally filtered and transmitted PCM-encoded. Antialiasing is done with a 2\(^{nd}\) order Sallen-Key prefilter (PREFI). The A/D Converter (ADC) is a modified slopeadaptive interpolative sigma-delta modulator with a sampling rate of 128 kHz. Digital downsampling to 8 kHz is done by subsequent decimation filters D1 and D2 together with the transmit PCM lowpass filter (LPX).

Receive Direction

The digital input signal is received PCM-encoded, digitally filtered and D/A converted to generate the analog output signal. Digital interpolation up to 128 kHz is done by the receive PCM lowpass filter (LPR) and the interpolation filters I1 and I2. The D/A Converter (DAC) output is fed to the 2\(^{nd}\) order Sallen-Key postfilter (POFI).

Programmable Functions

The high flexibility of the SICOFI-2 is based on a variety of user programmable filters, which are analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.
The SICOFI-2 bridges the gap between analog and digital voice signal transmission in modern telecommunication systems.

High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) provide the conversion accuracy required. Analog antialiasing prefilters (PREFI) and smoothing postfilters (POFI) are included. The dedicated on chip Digital Signal Processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM companding. The SLD or IOM-2 Interface handles digital voice transmission, SICOFI-2 feature control and access to the SICOFI-2 signaling pins. Specific filter programming is done by downloading coefficients to the coefficient ram (CRAM).
SICOFI®-2 Digital Interfaces

The SICOFI-2 digital interface section consists of a serial interface bus which can be configured to be compatible to SLD or the IOM-2 standard (with two different data clock frequencies), and a powerful signaling interface.

Selecting between the IOM-2 and SLD interfacing mode is simply performed by strapping the MODE pin.

\[
\begin{align*}
\text{MODE} &= '0' : \text{SLD Interface} \\
\text{MODE} &= '1' : \text{IOM-2 Interface}
\end{align*}
\]

For better understanding, pin names are quoted with their interface specific name. E.g. pin SIP/DU: SIP for SLD interface mode, DU for IOM-2 interface mode.

SLD Interface

The SLD serial interface consists of a bidirectional pin SIP, a data clock input SCLK, and a synchronization input DIR. Data bits are loaded or read out by the serial interface pin SIP. Bits are clocked in at the falling edge and clocked out at the rising edge of the slave clock pin SCLK (512 kHz). DIR and SCLK inputs must be phase locked. A SLD frame lasts 125 µs and consists of 32 bits transferred to the SICOFI-2 followed by 32 bits transferred from the SICOFI-2 to the SLD bus. The SLD interface thus provides a full duplex 256 kbit/s communication channel. This channel is subdivided in two 64 kbit/s voice/data channels, a 64 kbit/s feature control channel and an other 64 kbit/s signaling channel per direction. Bytes in all channels are serialized MSB first.

![Diagram of SICOFI-2 digital interfaces](image-url)

**ITD00448**
IOM®-2 Interface

The IOM-2 interface consists of two data lines and two clock lines. DU (data upstream) carries data from the SICOFI-2 to a master device. DD (data downstream) carries data from the master device to the SICOFI-2. A 8 kHz FSC (frame synchronization clock) signal as well as a 512 kHz or 4096 kHz DCL (data clock) signal is supplied. The SICOFI-2 implements all functions for analogue devices as described in the IOM-2 specification.

IOM®-2 Interface, DCL = 512 kHz (one channel per frame)

IOM®-2 Interface, DCL = 4096 kHz (eight channels per frame)
Detail A

Detail B
With a DCL frequency of 4096 kHz assignment of 8 time slots is possible. The IOM-2 operating mode and time-slot selection is set completely by pin-strapping of two pins TS1 and TS2, which work with ternary logic (– 5 V [N], 0 V [0] and + 5 V [P]).

<table>
<thead>
<tr>
<th>TS2</th>
<th>TS1</th>
<th>IOM-2 Operating Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>N</td>
<td>IOM-2, DCL = 512 kHz</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>IOM-2, DCL = 4096 kHz, time slot 0</td>
</tr>
<tr>
<td>N</td>
<td>0</td>
<td>IOM-2, DCL = 4096 kHz, time slot 1</td>
</tr>
<tr>
<td>0</td>
<td>P</td>
<td>IOM-2, DCL = 4096 kHz, time slot 2</td>
</tr>
<tr>
<td>N</td>
<td>P</td>
<td>IOM-2, DCL = 4096 kHz, time slot 3</td>
</tr>
<tr>
<td>P</td>
<td>0</td>
<td>IOM-2, DCL = 4096 kHz, time slot 4</td>
</tr>
<tr>
<td>0</td>
<td>N</td>
<td>IOM-2, DCL = 4096 kHz, time slot 5</td>
</tr>
<tr>
<td>P</td>
<td>P</td>
<td>IOM-2, DCL = 4096 kHz, time slot 6</td>
</tr>
<tr>
<td>P</td>
<td>N</td>
<td>IOM-2, DCL = 4096 kHz, time slot 7</td>
</tr>
</tbody>
</table>

**IOM®-2 MONITOR Channel Data Structure**

The MONITOR channel is used for the transfer of maintenance information between two functional blocks. By use of two MONITOR control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure.

The messages transmitted in the MONITOR channel may have different kinds of data structures. Therefore, the first byte of the message is used to indicate the structure of the following data.

Messages to and from the SICOFI-2 are started with the following byte:

```
BIT 7 6 5 4 3 2 1 0
1 0 0 0 0 0 0 1
```

Thus providing information for two analog lines, the SICOFI-2 is one device on one IOM-2 channel. MONITOR data for a specific analog channel is selected by the SICOFI-2 specific command following.

For more details on IOM-2 MONITOR channel data structure, and an IOM-2 specific identification command see Appendix B.
Programming

A message oriented byte transfer is used, due to the fact that the SICOFI-2 needs extended control information. With the appropriate commands, data can be written to the SICOFI-2 or read from the SICOFI-2 via the SLD or via the IOM-2 interface monitor channel.

Data transfer to the SICOFI-2 starts with a write command, followed by up to 8 bytes of data. The SICOFI-2 responds to a read command with the requested information, that is up to 8 bytes of data. (see Programming procedure).

The same command structure is used both in SLD and IOM-2 interface mode. If the SICOFI-2 is operating in IOM-2 interface mode, any new command sequence starts with a SICOFI-2 specific address-byte. The following command is the same in SLD and IOM-2 mode. If the command requests an answer, in SLD mode the SICOFI-2 will start immediately (next transmission period) with the requested data. In IOM-2 mode the SICOFI-2 specific address byte will be sent first, followed by the requested data.

Attention: In IOM-2 mode, each byte on the monitor channel, is sent twice at least.

Example for a programming sequence in SLD and IOM-2 interface mode:

<table>
<thead>
<tr>
<th>SLD Interface</th>
<th>IOM-2 Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receive</td>
<td>Transmit</td>
</tr>
<tr>
<td>SOP-Write</td>
<td>CR2 CR1</td>
</tr>
<tr>
<td>CR2</td>
<td>Address</td>
</tr>
<tr>
<td>CR1</td>
<td>CR1</td>
</tr>
<tr>
<td>SOP-Read</td>
<td>CR2 CR1</td>
</tr>
</tbody>
</table>
Control Bytes

The 8-bit control bytes consist of either commands, status information or data. There are three different classes of SICOFI-2 commands:

- **NOP**: NO OPERATION: no status modification or data exchange
- **SOP**: STATUS OPERATION: SICOFI-2 status setting/monitoring
- **COP**: COEFFICIENT OPERATION: filter coefficient setting/monitoring

The class of command is selected by bit 3 and 2 of the control byte as shown below.

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>COP</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

X ... don't care

Due to the extended SICOFI-2 feature control facilities, SOP and COP commands contain additional information for programming and verifying the SICOFI-2.

Programmable Devices

- 3 configuration registers per channel: CR1, CR2, CR3
- 1 coefficient ram per channel: CRAM
- 1 common configuration register: CR4 is only available in IOM-2 mode

The contents of CR4 is valid for both channels

To obtain more clarity, bit fields containing different informations for SLD and IOM-2 interface are high lighted in subsequent chapters.
**NOP Command**

If no status modification of the SICOFI-2 is required, a no operation byte NOP may be transferred.

**NOP receive**, not useful in IOM-2 interface mode

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**NOP transmit**, only available in SLD interface mode

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>PDA</td>
<td>PDB</td>
<td>VERSION</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**PDA**

PDA = 1 if channel A is in power-down mode
PDA = 0 if channel A is in power-up mode

**PDB**

PDB = 1 if channel B is in power-down mode
PDB = 0 if channel B is in power-up mode

**VERSION**

Four bit SICOFI-2 version identification

VERSION = 1111 for PEB2260 V1.X, V2.0
SOP Command

To modify or evaluate the SICOFI-2 status, the contents of up to three (four) configuration registers CR1, CR2, CR3 (and CR4) may be transferred to or from the SICOFI-2. This is done by a SOP-Command (status operation command). In SLD interface mode three configuration registers per channel are accessible. If the SICOFI-2 is operating with IOM-2 interface an additional fourth configuration register (CR4) can be written or read.

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD</td>
<td>R/W</td>
<td>PU</td>
<td>RST</td>
<td>0</td>
<td>1</td>
<td>LSEL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AD  Address Information
- AD = 0 channel A is addressed with this command
- AD = 1 channel B is addressed with this command

R/W  Read/Write Information: Enables reading from the SICOFI-2 or writing information to the SICOFI-2.
- R/W = 0 Write to SICOFI-2
- R/W = 1 Read from SICOFI-2

PU  Power Up/Power Down
- PU = 1 sets the assigned channel (see bit AD) of SICOFI-2 to power-up mode (operating)
- PU = 0 resets the assigned channel of SICOFI-2 to power-down (standby mode)

RST  Reset SICOFI-2
- RST = 1 forces SICOFI-2 to enter the Basic Setting Mode (see Operating Modes).

LSEL  Length select information (see also Programming Procedure)
This two bit field identifies the number of subsequent data bytes
- LSEL = 0 0 no byte following
- LSEL = 1 1 CR1 is following
- LSEL = 1 0 CR2 and CR1 are following
- ⇒ LSEL = 0 1 CR3, CR2 and CR1 are following in SLD interface mode
- ⇒ CR4*, CR3, CR2, CR1 are following in IOM-2 interface mode

*) Commands concerning CR4 are independent of bit AD in SOP command.

Semiconductor Group  77
CR1 Configuration Register 1

Configuration register CR1 defines the basic SICOFI-2 settings, which are:
enabling/disabling the programmable digital filters, programming of signaling pins, and
selection of the PCM companding characteristics.

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SB/C3A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LAW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

B
- Enable B - filter
  - B = 0: B - filter disabled, H(B) = 0
  - B = 1: B - filter enabled

Z
- Enable Z - filter
  - Z = 0: Z - filter disabled, H(Z) = 0
  - Z = 1: Z - filter enabled

X
- Enable X - filter
  - X = 0: X - filter disabled, H(X) = 1
  - X = 1: X - filter enabled

R
- Enable R - filter
  - R = 0: R - filter disabled, H(R) = 1
  - R = 1: R - filter enabled

GR
- Enable GR - filter
  - GR = 0: GR - filter disabled, H(GR) = 1
  - GR = 1: GR - filter enabled

GX
- Enable GX - filter
  - GX = 0: GX - filter disabled, H(GX) = 1
  - GX = 1: GX - filter enabled

SB/C3A
- SLD Interface mode: program bidirectional signaling pin SBA or SBB
  - SB = 0: programmable signaling pin SBx is input
  - SB = 1: programmable signaling pin SBx is output

SB/C3A
- IOM-2 interface mode: operation mode of pin C3A
  - C3A = 0: pin C3A is programmed as command output
  - C3A = 1: pin C3A is detector select output (see CR4)

LAW
- PCM - Law selection
  - LAW = 0: A - law
  - LAW = 1: μ - law (μ255 PCM)

---

1) Setting bit C3A to ‘1’ for either channel forces pin C3A to be detector select output.
CR2 Configuration Register 2

Configuration register CR2 sets analog gain control and enables two on-chip tone-generators. In IOM-2 operating mode two bidirectional command/indication pins are controlled.

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AGX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TG2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TG1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0/CI1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>O/CI2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**AGR**
Analog gain control receive-path

- AGR  =  0 0 0 dB
- AGR  =  0 1 6 dB attenuation
- AGR  =  1 0 11.95 dB attenuation
- AGR  =  1 1 13.9 dB attenuation

**AGX**
Analog gain control transmit-path

- AGX  =  0 0 0 dB
- AGX  =  0 1 6 dB amplification
- AGX  =  1 0 11.95 dB amplification
- AGX  =  1 1 13.9 dB amplification

**TG2**
Enable on chip tone generation 2

With the R-filter disabled a 1 kHz, –6 dBm0 sinusoidal signal is fed to the input of the receive lowpass filter LP. Frequency and gain can be set, by programming the R and GR-filter.

- TG2  =  0 On chip tone generator 2 disabled
- TG2  =  1 On chip tone generator 2 enabled

**TG1**
Enable on chip tone generation 1

With the R-filter disabled a 2 kHz, –6 dBm0 sinusoidal signal is fed to the input of the receive lowpass filter LP. Frequency and gain can be set, by programming the R and GR-filter.

- TG1  =  0 On chip tone generator 1 disabled
- TG1  =  1 On chip tone generator 1 enabled

**0/CI1**
SLD Interface mode: this bit is reserved for future use and has to be set to '0'

**0/CI2**
SLD Interface mode: this bit is reserved for future use and has to be set to '0'

### IOM-2 Interface mode: Command/indication pin CI1A or CI1B

- CI1  =  0 Programmable signaling pin CI1x is indication input
- CI1  =  1 Programmable signaling pin CI1x is command output

### IOM-2 Interface mode: Command/indication pin CI2A or CI2B

- CI1  =  0 Programmable signaling pin CI2x is indication input
- CI1  =  1 Programmable signaling pin CI2x is command output
CR3 Configuration Register 3

This register is for accessing testmodes only

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DHP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>COR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ALB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DLB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SWP**  
Swap channels\(^1\)

- **SWP = 0**  
  VOUTA and VINA are assigned to SLD/IOM-2 channel A
  VOUTB and VINB are assigned to SLD/IOM-2 channel B
- **SWP = 1**  
  VOUTA and VINA are assigned to SLD/IOM-2 channel B
  VOUTB and VINB are assigned to SLD/IOM-2 channel A

**DHP**  
Disable transmit highpass

- **DHP = 0**  
  Highpass enabled
- **DHP = 1**  
  Highpass disabled

**COR**  
Cut off receive path (analog voice output VOUTA or VOUTB is set to ‘0’)  

- **COR = 0**  
  Receivepath enabled
- **COR = 1**  
  Analog voice output is set to ‘0’

**DTS**  
Disable transmit signaling\(^1\)

- **DTS = 0**  
  Transmission of signaling/indication data (on SIP/DU) is enabled
- **DTS = 1**  
  Transmission of signaling/indication data (on SIP/DU) is disabled.  
  SIP/DU is in high impedance state.

**ALB**  
Analog loop back\(^2\)

- **ALB = 0 0**  
  No analog loop back established
- **ALB = 0 1**  
  Analog loop back via Z-filter. H(Z) = 1 if Z-filter is disabled
- **ALB = 1 1**  
  Far analog loop back (via 8 kHz, 16 bit linear)

**DLB**  
Digital loop back

- **DLB = 0 0**  
  No digital loop back established
- **DLB = 0 1**  
  Digital loop back via PCM-register (via 8 kHz, PCM)
- **DLB = 1 0**  
  Digital loop back via B-filter (via 16 kHz), H(B) = 1 if B-filter is disabled
- **DLB = 1 1**  
  Digital loop back via analog port (VIN = VOUT)

---

\(^1\) Setting bits SWP, DTS to ‘1’ for either channel enables the function.

\(^2\) All other codes are reserved for future use.
CR4 Configuration Register 4 (available in IOM®-2 interface mode only)

Register CR4 configures the data-upstream command/indication channel. The content of CR4 is valid for both channels A and B.

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>T</td>
</tr>
</tbody>
</table>

Upstream Update Interval N

To restrict the rate of upstream C/I-bit changes, persistence checking of the status information from the SLIC may be applied.

New status information will be transmitted upstream, after it has been stable for N milliseconds. N is programmable in the range of 1 to 15 ms in steps of 1 ms, with N = 0 the persistence checking is disabled.

<table>
<thead>
<tr>
<th>Field N</th>
<th>Update Interval Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>Persistance checking is disabled</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>Upstream transmission after 1 ms</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>Upstream transmission after 2 ms</td>
</tr>
<tr>
<td>. . . .</td>
<td>.</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>Upstream transmission after 14 ms</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>Upstream transmission after 15 ms</td>
</tr>
</tbody>
</table>
Detector Select Sampling Interval T

SLICs with multiplexed loop- and ground-key-status, which have a single status output pin for carrying the loop- and ground-key-status information, need a special detector select input.

*) Connection available with 512-kHz IOM®-2 Interface only
SICOFI-2 pin C3A can be programmed as detector select output in CR1. This command output pin is normally set to logical '0', such that the SLIC outputs loop status, which is passed to C/I-bits 1 and 4 via indication pins I1A and I1B. Every T microseconds, the detector select output changes to logical '1' for a time of 15.63 µs. During this time the ground key status is read from the SLIC and transferred upstream using C/I-bits 2 and 5 via indication pins I1A and I1B. The time interval T is programmable from 250 µs to 1.875 ms in 125 µs steps. It is possible to program the output to be permanently logical '0' or '1'.

<table>
<thead>
<tr>
<th>Field T</th>
<th>Time Interval T Between Detector Select High States</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>Detector select output C3A is programmed to '0' permanently</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>Time interval T is 250 µs</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>Time interval T is 375 µs</td>
</tr>
<tr>
<td>. . . .</td>
<td>.</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>Time interval T is 1.875 ms</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>Detector select output C3A is programmed to '1' permanently</td>
</tr>
</tbody>
</table>
COP Command

With a COP Command coefficients for the programmable filters can be written to the SICOFI-2 coefficient ram or transmitted on the SLD or IOM-2 interface for verification

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CODE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AD  Address information
AD  =  0   channel A is addressed with this command
AD  =  1   channel B is addressed with this command

R/W  Read/write information
This bit indicates whether filter coefficients are written to the SICOFI-2 or read from the SICOFI-2.
R/W  =  0   Write to SICOFI-2
R/W  =  1   Read from SICOFI-2

<table>
<thead>
<tr>
<th>CODE</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 1 1</td>
<td>B-Filter coefficients part 1 (followed by 8 bytes of data)</td>
</tr>
<tr>
<td>0 0 1 0 1 1</td>
<td>B-Filter coefficients part 2 (followed by 8 bytes of data)</td>
</tr>
<tr>
<td>0 1 0 0 1 1</td>
<td>Z-Filter coefficients (followed by 8 bytes of data)</td>
</tr>
<tr>
<td>0 1 1 0 0 0</td>
<td>B-Filter delay coefficients (followed by 4 bytes of data)</td>
</tr>
<tr>
<td>1 0 0 0 1 1</td>
<td>X-Filter coefficients (followed by 8 bytes of data)</td>
</tr>
<tr>
<td>1 0 1 0 1 1</td>
<td>R-Filter coefficients (followed by 8 bytes of data)</td>
</tr>
<tr>
<td>1 1 0 0 0 0</td>
<td>GX-Filter coefficients (followed by 4 bytes of data)</td>
</tr>
<tr>
<td>1 1 1 0 1 0</td>
<td>GR-Filter coefficients (followed by 2 bytes of data)</td>
</tr>
</tbody>
</table>

All other codes are reserved for future use.

*) In the range of 0 to 8 dB (0 to – 8 dB) gain adjustment is possible in steps ≤ 0.25 dB
SLIC Interface

The connection between SICOFI-2 and a SLIC is performed by the SICOFI-2 signaling and command/indication pins.
In SLD interface mode, the receive signaling byte is transferred to the signaling output pins. Data present at signaling input pins are transferred to the transmit signaling byte. Operating the SICOFI-2 with IOM-2 interface, data received from the downstream C/I byte are transferred to command output pins (C, C/I). Data on input pins (I, C/I) are transferred to the upstream C/I-byte.

SLD Interface Signaling Byte

The SICOFI-2 offers a 7 pin parallel signaling interface per channel.
Channel A: SI1A, SI2A, SI3A signaling input pins
SO1A, SO2A, SO3A signaling output pins
SBA programmable bidirectional signaling pin.
Channel B: SI1B, SI2B, SI3B signaling input pins
SO1B, SO2B, SO3B signaling output pins
SBB programmable bidirectional signaling pin.

Data present at SI1A ... SI3B and SBA, SBB (if programmed as input) are sampled and transferred to the SLD bus. Data received from the SLD bus are latched and fed to SO1A ... SO3B and SBA, SBB (if programmed as output).

Signaling byte format in receive direction:

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SBB1)</td>
<td>SO3B</td>
<td>SO2B</td>
<td>SO1B</td>
<td>SBA1)</td>
<td>SO3A</td>
<td>SO2A</td>
<td>SO1A</td>
</tr>
</tbody>
</table>

Signaling byte format in transmit direction:

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SBB2)</td>
<td>SI3B</td>
<td>SI2B</td>
<td>SI1B</td>
<td>SBA2)</td>
<td>SI3A</td>
<td>SI2A</td>
<td>SI1A</td>
</tr>
</tbody>
</table>

1) Don’t care, if pin programmed as input (see CR1).
2) '0', if pin programmed as output (see CR1).
The four possible cases of the signaling byte format are listed below.

<table>
<thead>
<tr>
<th>Case</th>
<th>Receive Signaling Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>7</td>
</tr>
<tr>
<td>1</td>
<td>SBB</td>
</tr>
<tr>
<td>2</td>
<td>X</td>
</tr>
<tr>
<td>3</td>
<td>SBB</td>
</tr>
<tr>
<td>4</td>
<td>X</td>
</tr>
</tbody>
</table>

X ... don't care

<table>
<thead>
<tr>
<th>Case</th>
<th>Transmit Signaling Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>7</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>SBB</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>SBB</td>
</tr>
</tbody>
</table>

Case 1: SBA and SBB are programmed as signaling outputs  
Case 2: SBA is programmed as output, SBB is programmed as signaling input  
Case 3: SBB is programmed as output, SBA is programmed as signaling input  
Case 4: SBA and SBB are programmed as signaling inputs

**IOM®-2 Interface Command/Indication Byte**

The SICOFI-2 offers a 11 pin parallel command/indication SLIC interface

**Indication input pins:**  
I1A (associated with channel A)  
I1B (associated with channel B)

**Command output pins:**  
C1A, C2A (associated with channel A)  
C1B, C2B (associated with channel B)  
C3A

**Programmable command/indication pins:**  
Cl1A, Cl2A (associated with channel A)  
Cl1B, Cl2B (associated with channel B)

Data present at I1A, I1B and Cl1A ... Cl2B (if programmed as input) are sampled and transferred upstream. Data received downstream from IOM-2 interface are latched and fed to C1A ... C2B and Cl1A ... Cl2B (if programmed as output).
### Data-downstream C/I channel byte format (receive):

<table>
<thead>
<tr>
<th>BIT</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ADR</td>
<td>C3A</td>
<td>CI2A/B</td>
<td>CI1A/B</td>
<td>C2A/B</td>
<td>C1A/B</td>
</tr>
</tbody>
</table>

In data-downstream direction, the 6 bit C/I field is split into an address bit and a 5 bit data-word. Depending on the ADR bit, data are transmitted to pins associated to channel A or channel B, and to pin C3A in either case.

### Data-upstream C/I channel byte format (transmit):

<table>
<thead>
<tr>
<th>BIT</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CI2B</td>
<td>CI1B</td>
<td>I1B</td>
<td>CI2A</td>
<td>CI1A</td>
<td>I1A</td>
</tr>
</tbody>
</table>

In data-upstream direction, the 6 bit C/I field is partitioned in two 3 bit fields. The three bits C/I 1 ... 3 and 4 ... 6 contain the command/indication data associated with an analogue channel. Typical examples for the C/I byte are listed below.

<table>
<thead>
<tr>
<th>Case</th>
<th>Data-Downstream (Receive) Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ADR</td>
</tr>
<tr>
<td>2</td>
<td>ADR</td>
</tr>
<tr>
<td>3</td>
<td>ADR</td>
</tr>
<tr>
<td>4</td>
<td>ADR</td>
</tr>
</tbody>
</table>

X ... don't care

<table>
<thead>
<tr>
<th>Case</th>
<th>Data-Upstream (Transmit) Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>CI2B</td>
</tr>
<tr>
<td>4</td>
<td>CI2B</td>
</tr>
</tbody>
</table>

Case 1: CI2A/B and CI1A/B are programmed as command outputs
Case 2: CI2A/B is programmed as output, CI1A/B is programmed as indication input
Case 3: CI2A/B is programmed as input, CI1A/B is programmed as command output
Case 4: CI2A/B and CI1A/B are programmed as indication inputs

1) Don't care, if pin programmed as input (see CR2)
2) Don't care, if pin C3A is programmed as detector select output (see CR1)
3) '0', if pin programmed as output (see CR2)
4) A for ADR = 0, B for ADR = 1
SLD Interface Programming Procedure

The following table shows typical control byte sequences. If the SICOFI-2 has to be configured completely during initialization, up to 60 bytes will be transferred.

<table>
<thead>
<tr>
<th>DIR</th>
<th>Receive</th>
<th>Transmit</th>
<th>Receive</th>
<th>Transmit</th>
<th>Receive</th>
<th>Transmit</th>
<th>Receive</th>
<th>Transmit</th>
<th>Receive</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**No Operation**

| | NOP | NOP | NOP | NOP | NOP | NOP | NOP | NOP | NOP |

**SOP Write**

| LSEL = 00 | SOP | NOP |   |   |   |   |   |   |   |
| LSEL = 11 | SOP | NOP | CR1 | NOP |   |   |   |   |   |
| LSEL = 10 | SOP | NOP | CR2 | NOP | CR1 | NOP |   |   |   |
| LSEL = 01 | SOP | NOP | CR3 | NOP | CR2 | NOP | CR1 | NOP |   |

**SOP Read**

| LSEL = 00 | SOP | NOP |   |   |   |   |   |   |   |
| LSEL = 11 | SOP | CR1 |   |   |   |   |   |   |   |
| LSEL = 10 | SOP | CR2 | X | CR1 |   |   |   |   |   |
| LSEL = 01 | SOP | CR3 | X | CR2 | X | CR1 |   |   |   |

**COP Write**

| 4 Bytes | COP | NOP | DB4 | NOP | DB3 | NOP | DB2 | NOP | DB1 | NOP |
| 8 Bytes | COP | NOP | DB8 | NOP | DB7 | NOP | DB2 | NOP | DB1 | NOP |

**COP Read**

| 4 Bytes | COP | DB4 | X | DB3 | DB1 | X | CR2 | X | CR1 |
| 8 Bytes | COP | DB8 | X | DB7 | DB1 | X | CR2 | X | CR1 |

DB1 ... DB8 coefficient data byte 1 ... 8
X don't care
## IOM®-2 Interface Programming Procedure

Example for a typical IOM-2 interface programming procedure, consisting of identification request and answer, a SOP write command with four byte following, and SOP read to verify the programming.

<table>
<thead>
<tr>
<th>Frame</th>
<th>Data Down</th>
<th>Data Up</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Monitor</td>
<td>MR/MX</td>
</tr>
<tr>
<td>1</td>
<td>11111111</td>
<td>11</td>
</tr>
<tr>
<td>2</td>
<td>IDRQT.1st byte</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>IDRQT.1st byte</td>
<td>10</td>
</tr>
<tr>
<td>4</td>
<td>IDRQT.2nd byte</td>
<td>11</td>
</tr>
<tr>
<td>5</td>
<td>IDRQT.2nd byte</td>
<td>10</td>
</tr>
<tr>
<td>6</td>
<td>11111111</td>
<td>11</td>
</tr>
<tr>
<td>7</td>
<td>11111111</td>
<td>11</td>
</tr>
<tr>
<td>8</td>
<td>11111111</td>
<td>01</td>
</tr>
<tr>
<td>9</td>
<td>11111111</td>
<td>01</td>
</tr>
<tr>
<td>10</td>
<td>11111111</td>
<td>11</td>
</tr>
<tr>
<td>11</td>
<td>11111111</td>
<td>01</td>
</tr>
<tr>
<td>12</td>
<td>Address</td>
<td>10</td>
</tr>
<tr>
<td>13</td>
<td>Address</td>
<td>10</td>
</tr>
<tr>
<td>14</td>
<td>SOP Write</td>
<td>11</td>
</tr>
<tr>
<td>15</td>
<td>SOP Write</td>
<td>10</td>
</tr>
<tr>
<td>16</td>
<td>CR4</td>
<td>11</td>
</tr>
<tr>
<td>17</td>
<td>CR4</td>
<td>10</td>
</tr>
<tr>
<td>18</td>
<td>CR3</td>
<td>11</td>
</tr>
<tr>
<td>19</td>
<td>CR3</td>
<td>10</td>
</tr>
<tr>
<td>20</td>
<td>CR2</td>
<td>11</td>
</tr>
<tr>
<td>21</td>
<td>CR2</td>
<td>10</td>
</tr>
<tr>
<td>22</td>
<td>CR1</td>
<td>11</td>
</tr>
<tr>
<td>23</td>
<td>CR1</td>
<td>10</td>
</tr>
<tr>
<td>24</td>
<td>SOP Read</td>
<td>11</td>
</tr>
<tr>
<td>25</td>
<td>SOP Read</td>
<td>10</td>
</tr>
<tr>
<td>26</td>
<td>11111111</td>
<td>11</td>
</tr>
<tr>
<td>27</td>
<td>11111111</td>
<td>11</td>
</tr>
<tr>
<td>28</td>
<td>11111111</td>
<td>01</td>
</tr>
<tr>
<td>29</td>
<td>11111111</td>
<td>01</td>
</tr>
<tr>
<td>30</td>
<td>11111111</td>
<td>11</td>
</tr>
<tr>
<td>31</td>
<td>11111111</td>
<td>01</td>
</tr>
<tr>
<td>32</td>
<td>11111111</td>
<td>11</td>
</tr>
<tr>
<td>33</td>
<td>11111111</td>
<td>01</td>
</tr>
<tr>
<td>34</td>
<td>11111111</td>
<td>11</td>
</tr>
<tr>
<td>35</td>
<td>11111111</td>
<td>01</td>
</tr>
<tr>
<td>36</td>
<td>11111111</td>
<td>11</td>
</tr>
<tr>
<td>37</td>
<td>11111111</td>
<td>01</td>
</tr>
</tbody>
</table>

*IDRQT ... identification request (80H, 00H)*
*IDANS ... answer to identification request (80H, 80H)*
*Address ... SICOFI-2 specific address byte (81H)*
*CRx ... Data for/of configuration register x.*
Operating Modes

Basic Setting Mode

Upon initial application of $V_{DD}$ or resetting pin RS to '1' during operation, or by software-reset (see SOP Command), the SICOFI-2 enters a basic setting mode. Basic setting means, that the SICOFI-2 configuration registers CR1 ... CR4 are initialized to '0' for both channel A and B. All programmable filters are disabled, A-law is chosen, all programmable signaling or command/indication pins are inputs. Analog gains are set to 0 dB amplification or attenuation respectively. The two tone-generators as well as any testmodes are disabled. There is no persistance checking and pin C3A is programmed command output if IOM-2 mode is selected. Receive signaling registers are cleared. SIP/DU is in high impedance state, the two analog outputs VOUTA and VOUTB and the receive signaling outputs are forced to ground.

The serial SLD or IOM-2 interface is ready to receive commands, starting with the next 8 kHz frame. In SLD interface mode the serial interface port SIP remains in high impedance state, until reception of a valid SOP or COP command.

If any voltage is applied to any input-pin before initial application of $V_{DD}$, the SICOFI-2 may not enter the basic setting mode. In this case it is necessary to reset the SICOFI-2 or to initialize the SICOFI-2 configuration registers to '0'.

Standby Mode

The SICOFI-2 is forced to standby mode with a power-down command by the 1st SOP-byte. Both channels A and B must be programmed separately. During standby mode the serial SICOFI-2 interface is ready to receive and transmit commands and data.

Operating Mode

The operating mode for any of the two channels is entered upon recognition of a power-up bit '1' in a SOP command for the specific channel.
Transmission Characteristics

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) needs a complete knowledge of the SICOFI-2's analog environment. Unless otherwise stated, the transmission characteristics are guaranteed within the test condition below.

\[ T_A = 0 \text{ to } 70 \, ^\circ C \text{ (PEB 2260)}; \quad T_A = -40 \text{ to } 85 \, ^\circ C \text{ (PEF 2260)}; \quad V_{DD} = 5 \, V \pm 5\%; \]
\[ V_{SS} = -5 \, V \pm 5\%; \quad GNDA = GNDB = GNDD = 0 \, V \]
\[ R_L > 10 \, k\Omega; \quad C_L < 50 \, pF; \quad H(Z) = H(B) = 0; \quad H(X) = H(R) = 1; \]
\[ G_X = 0 \text{ to } 8 \, dB; \quad G_R = 0 \text{ to } -8 \, dB; \]
\[ AG_X = 0, 6.00, 11.95, 13.90 \, dB; \quad AGR = 0, -6.00, -11.95, -13.90 \, dB; \]
\[ f = 1000 \, Hz; \quad 0 \, dBm0; \quad A-law \text{ or } \mu-law; \]

A 0 dBm0 signal is equivalent to 1.5763 [1.5710] Vrms. A 3.14 [3.17] dBm0 signal is equivalent to 2.263 Vrms which corresponds to the overload point of 3.2 V (A-law, [\mu-law]).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (either value)(^1)</td>
<td>Gain absolute (AGR = AGX = 0)</td>
<td>(G)</td>
<td>(-0.20 \pm 0.06)</td>
</tr>
<tr>
<td>(T_A = 25 , ^\circ C, \quad V_{DD} = 5 , V, \quad V_{SS} = -5 , V)</td>
<td></td>
<td>(-0.30)</td>
<td>(0.30)</td>
</tr>
<tr>
<td>(T_A = 0 \text{ to } 70 , ^\circ C, \quad V_{DD} = 5 , V \pm 5%, \quad V_{SS} = -5 , V \pm 5%)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain absolute (AGR = 0 to 13.90 dB, AGX = 0 to 13.90 dB)</td>
<td>Gain absolute</td>
<td>(G)</td>
<td>(-0.40)</td>
</tr>
<tr>
<td>(T_A = 0 \text{ to } 70 , ^\circ C, \quad V_{DD} = 5 , V \pm 5%, \quad V_{SS} = -5 , V \pm 5%)</td>
<td></td>
<td>(0.40)</td>
<td></td>
</tr>
<tr>
<td>Total harmonic distortion, 0 dBm0, (f = 1000 , Hz); 2nd, 3rd order</td>
<td>THD</td>
<td></td>
<td>(-50)</td>
</tr>
<tr>
<td>Intermodulation</td>
<td>(2/1 - f_2^2)</td>
<td>IMD</td>
<td></td>
</tr>
<tr>
<td>(2/1 - f_2^3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Crosstalk</td>
<td>CT(_{XR})</td>
<td></td>
<td>(-85)</td>
</tr>
<tr>
<td>0 dBm0, (f = 300 , Hz) to 3400 Hz</td>
<td>CT(_{RX})</td>
<td></td>
<td>(-85)</td>
</tr>
<tr>
<td>Transmit to receive</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Receive to transmit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Idle channel noise, transmit, A-law, psophometric</td>
<td>(V_{IN} = 0 , V)</td>
<td>(N_{TP})</td>
<td></td>
</tr>
<tr>
<td>transmit, (\mu)-law, C-message</td>
<td>(V_{IN} = 0 , V)</td>
<td>(N_{TC})</td>
<td></td>
</tr>
<tr>
<td>receive, A-law, psophometric</td>
<td>idle code + 0</td>
<td>(N_{RP})</td>
<td></td>
</tr>
<tr>
<td>receive, (\mu)-law, C-message</td>
<td>idle code + 0</td>
<td>(N_{RC})</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) \(R_L = 300 \, \Omega\) causes an additional attenuation in the range between \(-0.1\) to 0 dB.

\(^2\) Equal input levels in the range between \(-4 \, dBm0\) and \(-21 \, dBm0\); different frequencies in the range between 300 Hz and 3400 Hz.

\(^3\) Input level \(-9 \, dBm0\), frequency range 300 Hz to 3400 Hz and \(-23 \, dBm0\), 50 Hz.
Attenuation Distortion
Attenuation deviations stay within the limits in the figures below.

**Receive:** Reference frequency 1 kHz, input signal level 0 dBm0

**Transmit:** Reference frequency 1 kHz, input signal level 0 dBm0
Group Delay

Maximum delays for operating the SICOFI-2 with \( H(B) = H(Z) = 0 \) and \( H(R) = H(X) = 1 \) including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group delay deviations stay within the limits in the figures below.

**Group Delay Absolute Values:** Input signal level 0 dBm0

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmit Delay</td>
<td>( D_{XA} )</td>
<td>300 µs</td>
<td></td>
<td>( f = 1.4 \text{ kHz} )</td>
</tr>
<tr>
<td>Receive Delay</td>
<td>( D_{RA} )</td>
<td>240 µs</td>
<td></td>
<td>( f = 300 \text{ Hz} )</td>
</tr>
</tbody>
</table>

**Group Delay Distortion:** Input signal level 0 dBm0, reference frequency = 1.4 kHz
Out-of-Band Signals at Analog Input

With an out-of-band sine wave signal with frequency $f$ and level $A$ applied to the analog input, the level of any resulting frequency component at the digital output will stay at least $X$ dB below level $A$.

Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave of frequency $f$ applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least $X$ dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.
Gain Tracking (Receive and Transmit)

The gain deviations stay within the limits in the figures below.

Gain Tracking: Measured with noise signal according to CCITT recommendations, reference level is –10 dBm0, AGX = AGR = 0

Gain Tracking: Measured with sine wave in the range 700 to 1100 Hz, reference level is –10 dBm0, AGX = AGR = 0
Total Distortion
The signal-to-distortion ratio exceeds the limits in the following figures.

**Receive:** Measured with noise signal according to CCITT recommendations

**Transmit:** Measured with noise signal according to CCITT recommendations
The signal to distortion ratio exceeds the limits in the following figure.

- **Receive & Transmit:** Measured with sine wave in the range 700 to 1100 Hz excluding submultiples of 8 kHz

### Parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Input Level</th>
<th>Unit</th>
<th>Total Distortion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital loop back via B-filter or digital loop back via analog port</td>
<td>0 dBm0</td>
<td>31 dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-30 dBm0</td>
<td>31 dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-40 dBm0</td>
<td>25 dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-45 dBm0</td>
<td>20 dB</td>
<td></td>
</tr>
</tbody>
</table>

### Transhybrid Loss

The quality of transhybrid-balancing is very sensitive to deviations in gain and group delay – deviations inherent to the SICOFI-2 A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP’s etc.)

The SICOFI-2 transhybrid loss is measured the following way: A sine wave signal with level 0 dBm0 and a frequency in the range of 300 – 3400 Hz is applied to the digital input. The resulting analog output signal at pin VOUT is directly connected to VIN, e.g. with the SICOFI-2 testmode "Digital Loop Back via Analog Port" (see CR3). The programmable filters R, GR, X, GX and Z are disabled, the balancing filter B is enabled with coefficients optimized for this configuration (VOUT = VIN).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below.
B-filter coefficients recommended for transhybrid loss measurement with $V_{OUT} = V_{IN}$

<table>
<thead>
<tr>
<th>COP-Write</th>
<th>Coefficients</th>
</tr>
</thead>
<tbody>
<tr>
<td>B-filter part 1</td>
<td>(03)/(83)</td>
</tr>
<tr>
<td>B-filter part 2</td>
<td>(0B)/(8B)</td>
</tr>
<tr>
<td>B-filter delay</td>
<td>(18)/(98)</td>
</tr>
</tbody>
</table>

**Parameter** | **Symbol** | **Limit Values** | **Unit** | **Test Condition** |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Transhybrid loss at 500 Hz</td>
<td>$THL_{500}$</td>
<td>min.</td>
<td>typ.</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 2500 Hz</td>
<td>$THL_{2500}$</td>
<td>29</td>
<td>40</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 3000 Hz</td>
<td>$THL_{3000}$</td>
<td>27</td>
<td>35</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 500 Hz</td>
<td>$THL_{500}$</td>
<td>min.</td>
<td>typ.</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 2500 Hz</td>
<td>$THL_{2500}$</td>
<td>27</td>
<td>35</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 3000 Hz</td>
<td>$THL_{3000}$</td>
<td>25</td>
<td>30</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 500 Hz</td>
<td>$THL_{500}$</td>
<td>min.</td>
<td>typ.</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 2500 Hz</td>
<td>$THL_{2500}$</td>
<td>17</td>
<td>25</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 3000 Hz</td>
<td>$THL_{3000}$</td>
<td>15</td>
<td>20</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 500 Hz</td>
<td>$THL_{500}$</td>
<td>min.</td>
<td>typ.</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 2500 Hz</td>
<td>$THL_{2500}$</td>
<td>15</td>
<td>25</td>
<td>dB</td>
</tr>
<tr>
<td>Transhybrid loss at 3000 Hz</td>
<td>$THL_{3000}$</td>
<td>13</td>
<td>20</td>
<td>dB</td>
</tr>
</tbody>
</table>
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ referred to GNDD</td>
<td></td>
<td>–0.3 5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{SS}$ referred to GNDD</td>
<td></td>
<td>–5.5 0.3</td>
<td>V</td>
</tr>
<tr>
<td>GNDA to GNDD</td>
<td></td>
<td>–0.6 0.6</td>
<td>V</td>
</tr>
<tr>
<td>Analog input and output voltage referred to $V_{DD} = 5,V$; $V_{SS} = –5,V$</td>
<td>$V_{IN}$</td>
<td>–10.3 0.3</td>
<td>V</td>
</tr>
<tr>
<td>referred to $V_{SS} = –5,V$; $V_{DD} = 5,V$</td>
<td>$V_{IN}$</td>
<td>–0.3 10.3</td>
<td>V</td>
</tr>
<tr>
<td>All digital input voltages referred to $V_{DD} = 0,V$; $V_{DD} = 5,V$</td>
<td>$V_{IN}$</td>
<td>–0.3 5.3</td>
<td>V</td>
</tr>
<tr>
<td>referred to $V_{DD} = 5,V$; GNDD = 0 V</td>
<td>$V_{IN}$</td>
<td>–5.3 0.3</td>
<td>V</td>
</tr>
<tr>
<td>DC input and output current at any input or output pin</td>
<td>$I_{DC}$</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td>–60 125</td>
<td>°C</td>
</tr>
<tr>
<td>Ambient temperature under bias</td>
<td>$T_{A}$</td>
<td>–10 80</td>
<td>°C</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>$P_{D}$</td>
<td>1</td>
<td>W</td>
</tr>
</tbody>
</table>
Operating Range

\[ T_A = 0 \text{ to } 70 \, ^\circ\text{C}; \quad V_{DD} = 5 \, V \pm 5\%; \quad V_{SS} = -5 \, V \pm 5\%; \quad GNDD = 0 \, V; \quad GNDA = 0 \, V \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ I_{DD} ] supply current</td>
<td>[ I_{DD} ]</td>
<td>0.5/22</td>
<td>0.8/28</td>
<td>mA</td>
</tr>
<tr>
<td>standby</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>operating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[ I_{SS} ] supply current</td>
<td>[ I_{SS} ]</td>
<td>0.05/12</td>
<td>0.08/18</td>
<td>mA</td>
</tr>
<tr>
<td>standby</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>operating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply rejection</td>
<td>[ PSRR ]</td>
<td>30</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>(of either supply/direction)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power dissipation</td>
<td>[ P_{Ds} ]</td>
<td>2.75/110</td>
<td>4.4/150</td>
<td>mW</td>
</tr>
<tr>
<td>standby</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power dissipation</td>
<td>[ P_{Do1} ]</td>
<td>170</td>
<td>230</td>
<td>mW</td>
</tr>
<tr>
<td>operating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power dissipation</td>
<td>[ P_{Do2} ]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>operating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| \[ T_A = 0 \text{ to } 85 \, ^\circ\text{C}; \quad V_{DD} = 5 \, V \pm 5\%; \quad V_{SS} = -5 \, V \pm 5\%; \quad GNDD = 0 \, V; \quad GNDA = 0 \, V \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ I_{DD} ] supply current</td>
<td>[ I_{DD} ]</td>
<td>0.6/0.65</td>
<td>0.95/1.1</td>
<td>mA</td>
</tr>
<tr>
<td>standby</td>
<td></td>
<td>26/28</td>
<td>34/37</td>
<td>-25°C/-40°C</td>
</tr>
<tr>
<td>operating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[ I_{SS} ] supply current</td>
<td>[ I_{SS} ]</td>
<td>0.06/0.065</td>
<td>0.08/18</td>
<td>mA</td>
</tr>
<tr>
<td>standby</td>
<td></td>
<td>14/16</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td>operating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply rejection</td>
<td>[ PSRR ]</td>
<td>30</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>(of either supply/direction)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power dissipation</td>
<td>[ P_{Ds} ]</td>
<td>3.3/3.6</td>
<td>5.2/6.1</td>
<td>mW</td>
</tr>
<tr>
<td>standby</td>
<td></td>
<td>132/143</td>
<td>180/195</td>
<td>1 channel</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>[ P_{Do1} ]</td>
<td>200/220</td>
<td>280/305</td>
<td>mW</td>
</tr>
<tr>
<td>operating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power dissipation</td>
<td>[ P_{Do2} ]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Electrical Characteristics**

### Digital Interface

\[ T_A = 0 \text{ to } 70 \, ^\circ\text{C (PEB 2260); } T_A = -40 \text{ to } 85 \, ^\circ\text{C (PEF 2260)}; \, V_{DD} = 5 \, V \pm 5\%; \, V_{SS} = -5 \, V \pm 5\%; \, GNDD = 0 \, V; \, GNDA = 0 \, V \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values min.</th>
<th>Limit Values max.</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>L-input voltage</td>
<td>( V_{IL} )</td>
<td>-0.3</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>H-input voltage</td>
<td>( V_{IH} )</td>
<td>2.0</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Negative-input voltage</td>
<td>( V_{IN} )</td>
<td>-3.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>L-output voltage</td>
<td>( V_{OL} )</td>
<td>0.45</td>
<td></td>
<td>V</td>
<td>( I_0 = -2 , mA )</td>
</tr>
<tr>
<td>H-output voltage</td>
<td>( V_{OH} )</td>
<td>2.4</td>
<td></td>
<td>V</td>
<td>( I_0 = 400 , \mu A )</td>
</tr>
<tr>
<td>Input leakage current</td>
<td>( I_{IL} )</td>
<td>( \pm 1 )</td>
<td></td>
<td>( \mu A )</td>
<td>(-0.3 \leq V_{IN} \leq V_{DD})</td>
</tr>
</tbody>
</table>

### Analog Interface

\[ T_A = 0 \text{ to } 70 \, ^\circ\text{C (PEB 2260); } T_A = -40 \text{ to } 85 \, ^\circ\text{C (PEF 2260)}; \, V_{DD} = 5 \, V \pm 5\%; \, V_{SS} = -5 \, V \pm 5\%; \, GNDD = 0 \, V; \, GNDA = 0 \, V \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values min.</th>
<th>Limit Values max.</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog input resistance</td>
<td>( R_I )</td>
<td>10</td>
<td></td>
<td>( \Omega )</td>
<td></td>
</tr>
<tr>
<td>Analog output resistance</td>
<td>( R_O )</td>
<td>10</td>
<td></td>
<td>( \Omega )</td>
<td></td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>( V_{IO} )</td>
<td>( \pm 50 )</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Output offset voltage</td>
<td>( V_{OO} )</td>
<td>( \pm 50 )</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Input voltage range</td>
<td>( V_{IR} )</td>
<td>( \pm 3.2 )</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output voltage range</td>
<td>( V_{OR} )</td>
<td>( \pm 3.1 )</td>
<td></td>
<td>V</td>
<td>( R_L \geq 300 , \Omega, , C_L \leq 50 , pF )</td>
</tr>
</tbody>
</table>

### Reset Timing

To reset the SICOFI-2 to basic setting mode, positive pulses applied to pin RS have to be longer than \( 2 \times t_{SCLK} \) for SLD Interface mode, or \( 2 \times t_{DCL} \) for IOM-2 Interface mode. The SICOFI-2 is resetted, if a clock is applied at pin 21 (SCLK/DCL). Spikes shorter than \( t_{SCLK} \) (\( t_{DCL} \)) will be ignored.
SIP Interface Timing (SLD)

Switching Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Period SCLK(^1)</td>
<td>(t_{SCLK})</td>
<td>1/512 kHz</td>
<td></td>
</tr>
<tr>
<td>SCLK duty cycle</td>
<td></td>
<td>20 50 80</td>
<td>%</td>
</tr>
<tr>
<td>Period DIR(^1)</td>
<td>(t_{DIR})</td>
<td>125</td>
<td>(\mu)S</td>
</tr>
<tr>
<td>DIR setup time</td>
<td>(t_{DIR \times S})</td>
<td>40 (t_{SCLKH})</td>
<td>ns</td>
</tr>
<tr>
<td>DIR hold time</td>
<td>(t_{DIR \times H})</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>SIP data in setup time</td>
<td>(t_{DIN \times S})</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>SIP data in hold time</td>
<td>(t_{DIN \times H})</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>SIP data out delay</td>
<td>(t_{dOUT})</td>
<td>150 250</td>
<td>ns</td>
</tr>
<tr>
<td>SIP data out high impedance delay</td>
<td>(t_{dDHZ})</td>
<td>50 70</td>
<td>ns</td>
</tr>
</tbody>
</table>

\(^1\) \(t_{DIR} = 64 \times t_{SCLK}\)
Signaling Interface Timing (SLD)

Switching Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay signaling out</td>
<td>$t_{dSIGOUT}$</td>
<td>250</td>
<td>350</td>
</tr>
<tr>
<td>Delay signaling high impedance</td>
<td>$t_{dSIGZ}$</td>
<td>150</td>
<td>200</td>
</tr>
<tr>
<td>Delay signaling active</td>
<td>$t_{dSIGA}$</td>
<td>150</td>
<td>200</td>
</tr>
<tr>
<td>SIG in setup time</td>
<td>$t_{SIGIN \times S}$</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>SIG in hold time</td>
<td>$t_{SIGIN \times H}$</td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

1) Pins SO1 ... SO3; Pins SA ... SD as output
2) Pins SI1 ... SI3; Pins SA ... SD as input
3) For programmable signaling pins SBA/SBB
### IOM®-2 Interface Timing

#### Switching Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Period DCL 'slow' mode(^1)</td>
<td>( t_{\text{DCL}} )</td>
<td>1/512 kHz</td>
<td></td>
</tr>
<tr>
<td>Period DCL 'fast' mode(^1)</td>
<td>( t_{\text{DCL}} )</td>
<td>1/4096 kHz</td>
<td></td>
</tr>
<tr>
<td>DCL duty cycle</td>
<td></td>
<td>40</td>
<td>60 %</td>
</tr>
<tr>
<td>Period FSC(^1)</td>
<td>( t_{\text{FSC}} )</td>
<td>125</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>FSC setup time</td>
<td>( t_{\text{FSC} \times s} )</td>
<td>70</td>
<td>( t_{\text{DCLH}} )</td>
</tr>
<tr>
<td>FSC hold time</td>
<td>( t_{\text{FSC} \times H} )</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>DD data in setup time</td>
<td>( t_{\text{DD} \times s} )</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>DD data in hold time</td>
<td>( t_{\text{DD} \times H} )</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>DU data out delay</td>
<td>( t_{\text{DU}} )</td>
<td>150(^2)</td>
<td>250</td>
</tr>
</tbody>
</table>

---

1\(^{\text{IOM-2 interface mode, DCL = 512 kHz: } t_{\text{FSC}} = 64 \times t_{\text{DCL}}}
2\(^{\text{IOM-2 interface mode, DCL = 4096 kHz: } t_{\text{FSC}} = 512 \times t_{\text{DCL}}}

\(^2\) Depending on pull up resistor (typical 10 \( \Omega \))
IOM®-2 Command/Indication Interface Timing

Switching Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command out delay</td>
<td>$t_{dc\text{out}}$</td>
<td>min.</td>
<td>typ.</td>
</tr>
<tr>
<td>Command out high impedance</td>
<td>$t_{dcz}$</td>
<td>150</td>
<td>200</td>
</tr>
<tr>
<td>Command out active</td>
<td>$t_{dca}$</td>
<td>150</td>
<td>200</td>
</tr>
<tr>
<td>Indication in setup time</td>
<td>$t_{lin \times S}$</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>Indication in hold time</td>
<td>$t_{lin \times H}$</td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>
Detector Select Timing

IOM®-2 Interface, DCL = 512 kHz (one channel per frame)

IOM®-2 Interface, DCL = 4096 kHz (eight channels per frame)

Detail A

Switching Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detector select high time</td>
<td>$t_{C3Ah}$</td>
<td>15.6</td>
<td>µs</td>
</tr>
<tr>
<td>Detector select delay, 'slow' mode</td>
<td>$t_{C3Ads}$</td>
<td>82.0</td>
<td>µs</td>
</tr>
<tr>
<td>Detector select delay, 'fast' mode</td>
<td>$t_{C3Adf}$</td>
<td>−46.8</td>
<td>µs</td>
</tr>
<tr>
<td>Indication in setup time</td>
<td>$t_{in,s}$</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Indication in hold time</td>
<td>$t_{in,h}$</td>
<td>100</td>
<td>ns</td>
</tr>
</tbody>
</table>
Appendix A

On Chip Tone Generation

With bit TG2, TG1 in configuration register CR2 two tone generators per channel can be activated in receive direction; the R-filter output is set to ‘0’ with any tone generator activated. Each tone generator frequency and amplitude is programmable individually via R-filter coefficients.

Every byte sequence is started with 2B/AB depending on the channel to be programmed.

<table>
<thead>
<tr>
<th>TG1</th>
<th>TG2</th>
<th>Byte Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>TG1-Coefficent</td>
</tr>
<tr>
<td>2000</td>
<td>0</td>
<td>2000</td>
</tr>
<tr>
<td>1000</td>
<td>0</td>
<td>1000</td>
</tr>
<tr>
<td>800</td>
<td>0</td>
<td>800</td>
</tr>
<tr>
<td>697</td>
<td>0</td>
<td>770</td>
</tr>
<tr>
<td>852</td>
<td>0</td>
<td>941</td>
</tr>
<tr>
<td>1209</td>
<td>0</td>
<td>1336</td>
</tr>
<tr>
<td>1477</td>
<td>0</td>
<td>1633</td>
</tr>
<tr>
<td>2000</td>
<td>0</td>
<td>1000</td>
</tr>
<tr>
<td>1000</td>
<td>0</td>
<td>500</td>
</tr>
<tr>
<td>1000</td>
<td>-2.5</td>
<td>500</td>
</tr>
<tr>
<td>1000</td>
<td>-6</td>
<td>500</td>
</tr>
<tr>
<td>1000</td>
<td>-5</td>
<td>500</td>
</tr>
<tr>
<td>1000</td>
<td>-4.1</td>
<td>500</td>
</tr>
<tr>
<td>1000</td>
<td>-2.5</td>
<td>500</td>
</tr>
<tr>
<td>1000</td>
<td>-1.5</td>
<td>500</td>
</tr>
</tbody>
</table>

Note: The generated tones are sinewaves with harmonic distortion $<-25$ dB
Appendix B

IOM®-2 Interface MONITOR Transfer Protocol

The MONITOR channel is used for the transfer of maintenance information between two functional blocks. By use of two MONITOR control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure.

The MR and MX bits in the fourth octet (the control channel) of the IOM-2 frame are used for the handling of the MONITOR channel.

- A pair of MR and MX in the inactive state for two or more consecutive frames indicates an idle state on the MONITOR channel and the end of message (EOM)
- A start of transmission is initiated by the transmitter with the transmission of the MX bit from the inactive state to the active state together with the first byte sent on the MONITOR channel. The receiver acknowledges the first byte by setting the MR bit in the other direction to active and keeping it active for at least one more frame.
- The same byte is sent continuously in each frame until either a new byte is transmitted, the end of message or an abort
- Flow control, in the form of transmission delay, can only take place when the transmitters MX and the receivers MR bit are in active state.
- Any false MX or MR bit received by the receiver or transmitter leads to a request for abort or abort, respectively.
- Since the receiver is able to receive the MONITOR data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received the receiver will wait for the receipt of two identical successive bytes (last look function).
- A collision resolution mechanism is implemented in the transmitter. This is done by looking for the idle phase of the MX-bit and making a per bit collision check on the transmitted MONITOR data.
- Any abort leads to a reset of the SICOFI-2 command stack, the device is ready to receive new commands.
- To obtain a maximum speed data transfer, the transmitter anticipates the falling edge of the receivers acknowledgement.
- Due to the inherent SLD-programming structure, duplex operation is not possible.
Identification Command

In order to be able to unambiguously identify different devices by software, a two byte identification command is defined for analog line IOM-2 devices.

```
1 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0
```

Each device will then respond with its specific identification code. For the SICOFI-2 this two byte identification code is:

```
1 0 0 0 0 0 0 0 0
1 0 0 0 0 0 0 0 0
```

Each byte is transferred at least twice (in two consecutive frames).
State Diagram of the SICOFI®-2 MONITOR Transmitter

- **MR**: MR-bit received
- **MX**: MX-bit calculated and expected on DU-line
- **MXR**: MX-bit sampled on DU-line
- **CLS**: Collision within the MONITOR data byte
- **RQT**: Request for transmission form internal source
- **ABT**: Abort request/indication
State Diagram of the SICOFI®-2 MONITOR Receiver

- **MR**  ... MR-bit transmitted on DU-line
- **MX**  ... MX-bit received data downstream
- **LL**  ... Last lock of MONITOR byte received
- **ABT** ... Abort indication to internal source
Plastic Dual-in-Line Package, P-DIP-22

Dimensions in mm

1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include chamfer protrusion of 0.15 max. per side

Approx. weight 2.1 g

Plastic-Leaded Chip Carrier, P-LCC-28-R (SMD)

Dimensions in mm

1) Does not include plastic or metal protrusion of 0.10 max. per side

SMD = Surface Mounted Device
### 1 General Overview on Hardware / Software Tools

<table>
<thead>
<tr>
<th>Designation</th>
<th>Ordering Code</th>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>User Boards</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SICOFI Testboard</td>
<td>STUT 2060</td>
<td>Q67100-H6058</td>
<td>–</td>
</tr>
<tr>
<td>SICOFI-2 Module¹</td>
<td>SIPB 5135</td>
<td>Q67100-H6149</td>
<td>–</td>
</tr>
<tr>
<td><strong>SLIC Boards</strong></td>
<td></td>
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</tr>
<tr>
<td>HARRIS HC 5502/5504</td>
<td>STUS 5502</td>
<td>Q67100-H6175</td>
<td>A</td>
</tr>
<tr>
<td>HARRIS HC 5509</td>
<td>STUS 5509</td>
<td>Q67100-H6270</td>
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</tr>
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<td>STM L3000 + L3030</td>
<td>STUS 3030</td>
<td>Q67100-H6178</td>
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<td>ERICSSON PBL 3762</td>
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<td>Q67100-H6180</td>
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<td>ERICSSON PBL 3736</td>
<td>STUS 3736</td>
<td>Q67100-H6181</td>
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<td>Feeding</td>
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<td>Transformer Transverse Feeding</td>
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<td>Q67100-H6177</td>
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<tr>
<td><strong>Software</strong></td>
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</tr>
<tr>
<td>SICOFI Coefficient and Simulation Program for PEB 2060/PEB2260</td>
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¹ for the ISDN PC Userboard System (SIPB)
² Mainboard Firmware and Menu Software
A = available
U = under development

---

1) for the ISDN PC Userboard System (SIPB)
2) Mainboard Firmware and Menu Software
A = available
U = under development
2 SICOFI® Coefficients Program (STS 2060)

2.1 Features

- Coefficients program available on floppy disk for PC AT or compatible
- Calculates the coefficients for all digital filters in SICOFI PEB 2060/PEB 2260 (Z, R, X, B, GR, GX)
- Menu driven program surface
- Graphic screen output for various SLIC/SICOFI transfer functions
- Direct programming of SICOFI testboard STUT 2060
- SLIC program parts for various standard SLICs included
- Analog simulation program for modelling new user specific SLICs included

2.2 General Overview

The high flexibility of the SICOFI is based on a variety of user programmable filters, which consist of analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.

To gain an optimum result within a given environment while observing existing prescriptions, Siemens offers to the SICOFI user the software packet STS 2060, which performs the calculation of the filter coefficients by using an overall optimizing approach.

Because of the modularity of the SICOFI software program, it is possible to use the SICOFI together with
- transformer SLICs with series or transverse feeding
- fixed electronic SLICs (Boards and SLIC program parts are available from Siemens Semiconductor)
- new user specific SLICs

The STS 2060 software runs on any IBM-AT compatible PC under MD-DOS Version 3.0 or later providing 640 Kbyte available RAM, a 1.2 Mbyte floppy disk drive, and the math coprocessor 80287 (optional).

The STS 2060 software consists of the two major sections: SLIC program (SLIC.EXE) and SICOFI program (SICOFI.BAT). A transfer file (SLIC.SLI) provides the interface between these two programs. Instead of SLIC.EXE it is possible to use a special analog simulation program (S.BAT) for modelling new user specific SLICs.

All the specific values concerning the SLIC and its external circuitry (physical data, filter dimensions, ...) are gathered in an input file SLIC.INP.

The SLIC program SLIC.EXE models the SLIC and its external circuitry in order to create a file SLIC.SLI which contains their transmission characteristics.

SLIC.SLI is a transfer file (output/input file) between the SLIC program and the SICOFI program to introduce the SLIC circuit data into the SICOFI program.

COUNTRY.SPE is an input file of the SICOFI program describing the customer's specification (CCITT etc ...) and measurement configuration parameters (e.g. termination impedance).
REF.BYT is an optional input file of the SICOFI program. It is a reference file which defines a frame in which the program can write the calculated coefficients with some predefined commands. These commands are the macrocommands necessary to send the SICOFI coefficients from the PBC/PIC (PEB 2050/52) to the SICOFI (PEB 2060/2260) by means of the SLD-bus control byte. After a calculation the actual SICOFI coefficients may be stored in an output file called e.g. USER.BYT. This file contains the commands from the REF.BYT file together with updated coefficients.

SICOFI.CTL is the control file of the SICOFI program. It contains the data controlling the optimization and simulation processes.

SICOFI.BAT is the SICOFI batch program which starts an execution program to generate the SICOFI coefficients and calculate the theoretical transfer functions of the set of SLIC-SICOFI.

RESULT.RES is the output file of SICOFI.BAT. It contains the coefficients for programming the SICOFI according to the SLIC used. The calculated results corresponding to various measurements to be taken on the set SICOFI + SLIC are listed. (e.g. return loss, frequency response, echo return loss, etc.) This result file can also be used as control file of SICOFI.BAT.

![SICOFI® Software Structure Diagram](image-url)
3 SICOFI® Test Board (STUT 2060)

3.1 Features
- Two SICOFI PEB 2060 and one PBC PEB 2050 or PIC PEB 2052 onboard
- SAB 8031 microprocessor system
- Serial interface
- Two interfaces for connecting customer specific SLIC boards
- Adapter for connecting SICOFI-2 PEB 2260 included

3.2 General Overview
The SICOFI® test board STUT 2060 is a stand alone board which offers the possibility of connecting any external customer specific SLICs with the SICOFI for evaluation of customer specific combinations of SLIC and SICOFI. This setup allows measurements and tests covering the transfer functions of the complete subscriber line module.

The board is programmable via an RS 232 interface by a terminal or PC. The registers of the PBC or PIC and SICOFI can be accessed and therefore the SLIC can be programmed.

Different customer specific SLICs or ready designed SLIC boards available from Siemens Semiconductor may be connected to the SICOFI testboard STUT 2060 via a 64-pin connector. With this setup it is possible to make the following investigations:
- to test the SLIC hardware
- to verify the programmed coefficients, which are calculated with the SICOFI coefficients program
- to measure many different SLICs in a short time
4 SICOFI®-2 Module (SIPB 5135)

4.1 Features

- Compatible to SIPB 5000 userboard system
- Two interfaces for connecting customer specific SLIC boards
- Same SLIC connector as on the SICOFI Testboard STUT 2060
- SICOFI-2 can be operated in two different interface modes (SLD or IOM®-2)

4.2 General Overview

The use of the Siemens ISDN PC Development System provides significant savings in R & D time when designing a customer specific ISDN application. The system consists of modular hardware in the form of the Siemens ISDN PC User Board (SIPB) and of several software packages.

With the SICOFI-2 PEB 2260 the SICOFI-2 module already provides a ready to use codec/filter and interfaces to two SLICs. Thus this module offers the outstanding advantage of enabling immediate starting with experiments on a subscriber line board.

The SICOFI-2 module SIPB 5135 is developed to be used in connection with the Line Card Module SIPB 5121. If at the secondary side of the Line Card Module a PCM4 Adaptor SIPB 5311 is connected, a very useful development and testing tool for the analog line card is built up. Using a PCM4 of Wandel & Goltermann the following measurements are possible:

- return loss
- level in A/D- and D/A-direction
- gain tracking in A/D- and D/A-direction
- noise in A/D- and D/A-direction
- echo return loss
Measuring Set Up with SICOFI®-2 Module
## Software Description STS 2060

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1 Introduction
How to Use This Manual

If you are already familiar with the former SICOFI software version 2.0, we suggest starting having a look at the 'New features in SICOFI software version 3.0' described in the appendix 9.1.

The background and some theory is described in chapters 2, 3 and 4.

If you want to start straightaway with the program, begin directly with chapter 5.

An example in chapter 6 explains how to obtain SICOFI coefficients for a special SLIC application.

Some tricks to take advantage of all the possibilities of the program are explained in chapter 7.

Measurements of SICOFI-SLIC transfer functions and some specifications are described in chapter 8.

The modularity and flexibility of the software introduces a large amount of files and variables.

An alphabetical index is available at the end of this document in chapter 10:

'Index of the variables used in the software'

An idea of how to proceed in any case is suggested by the following figure 1.
Figure 1
General Suggestions for Using this Manual
The SICOFI provides separate input and output ports for transmit and receive direction.

**Transmit Direction**

The analog input signal is A/D converted, digitally filtered and transmitted either PCM-encoded or linear. The A/D converter used is a modified slope adaptive interpolative sigma-delta modulator with a sampling rate of 128 kHz. To remove resulting noise, antialiasing is done with a 2nd order Sallen-Key prefilter (PREFI). Subsequently the signal is downsampled to 8 kHz by decimation filters D1 and D2 together with the PCM bandpass filters (LPX, HP).

**Receive Direction**

The digital input signal is received PCM-encoded or linear, digitally filtered and D/A converted to generate the analog output signal. Digital interpolation up to 128 kHz is done by the PCM lowpass filter (LPR) and the interpolation filters I1 and I2. The D/A Converter output is fed to the 2nd order Sallen-Key postfilter (POFI).

**Programmable Function**

The high flexibility of the SICOFI is based on a variety of user programmable filters, which are analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.

To gain an optimum result within a given environment while observing existing prescriptions, Siemens offers to the SICOFI user the software packet STS 2060, which performs the calculation of the filter coefficients by using an overall optimizing approach.

Because of the modularity of the SICOFI software program, it is possible to use the SICOFI together with

- transformer SLICs with series or transverse feeding
- fixed electronic SLICs (see chapter 9.2: Available SICOFI / SLIC Documentation)
- new user specific SLICs

The STS 2060 software runs on any IBM-AT compatible PC under MS-DOS Version 3.0 or later providing 640 Kbyte available RAM, a 1.2 Mbyte floppy disk drive, and the math coprocessor 80297 (optional).

The purpose of the following pages is to given an overview on the SICOFI software and its background.

For more details on the SICOFI hardware, refer to the SICOFI data sheets.

A list of the available SICOFI software and hardware tools will be found in chapter 9.2.
2  SICOFI® Software Principle

The hardware can be split into two parts: SLIC and its external circuitry on the one hand and SICOFI on the other (see figure 2).

Figure 2
SLIC-SICOFI® Hardware

Accordingly the STS 2060 software consists of two major sections: SLIC program and SICOFI program.

A transfer file (SLIC file) provides the interface between these two programs (see figure 3).

Figure 3
Software Structure
Details of the SICOFI software structure are shown in the following figure:

![Diagram](https://via.placeholder.com/150)

**Figure 4**  
Details of the Software Structure

All the specific values concerning the SLIC and its external circuitry (physical data, filter dimensions, ...) are gathered in an input file SLIC.INP.

The SLIC program SLIC.EXE models the SLIC and its external circuitry in order to create a file SLIC.SLI which contains their transmission characteristics.

SLIC.SLI is a transfer file (output/input file) between the SLIC program and the SICOFI program to introduce the SLIC circuit data into the SICOFI program.

COUNTRY.SPE is an input file of the SICOFI program describing the customer’s specification (CCITT etc ...) and measurement configuration parameters (e.g. termination impedance).
REF.BYT is an optional input file of the SICOFI program. It is a reference file which defines a frame in which the program can write the calculated coefficients with some predefined commands. These commands are the macrocommands necessary to send the SICOFI coefficients from the Peripheral Board Controller PBC (PEB 2050) to SICOFI (PEB 2060) by means of the SLD-bus control byte. After a calculation the actual SICOFI coefficients may be stored in an output file called e.g. USER.BYT. This file contains the commands from the REF.BYT file together with updated coefficients.

SICOFI.CTL is the control file of the SICOFI program. It contains the data controlling the optimization and simulation processes.

SICOFI.BAT is the SICOFI batch program which starts a execution program to generate the SICOFI coefficients and calculate the theoretical transfer functions of the set of SLIC-SICOFI.

RESULT.RES is the output file of SICOFI.BAT. It contains the coefficients for programming the SICOFI according to the SLIC used. The calculated results corresponding to various measurements to be taken on the set SICOFI + SLIC are listed. (e.g. return loss, frequency response, echo return loss, etc.). This result file can also be used as control file of SICOFI.BAT.
3  SLIC Program Description

3.1  Program Functions, M-Parameter

The SLIC program SLIC.EXE generates a model of the SLIC and its external circuitry to provide the SICOFI program with the transfer functions of this circuit. The SLIC and its external circuitry are accessible through three ports as shown in figure 5.

![SLIC and its External Circuitry as a Three-Port](image)

Figure 5
SLIC and its External Circuitry as a Three-Port

$I_1$, $I_2$, and $I_3$ are port currents and $V_1$, $V_2$, and $V_3$ are port voltages. This circuit can be described by the following set of equations:

1. $I_1 = M_{11} V_1 + M_{12} V_3 + M_{13} I_2$
2. $V_2 = M_{21} V_1 + M_{22} V_3 + M_{23} I_2$
3. $I_3 = M_{31} V_1 + M_{32} V_3 + M_{33} I_2$

**Note:** definition of a port

![Diagram of Port Definition](image)

When the SLIC is connected to the SICOFI, we can assume that:

- $I_2 = 0$ because of the high SICOFI input impedance. (In special cases the SICOFI input impedance can be included in the three-port model.)
- $I_3$ is not relevant in the following calculations because the SICOFI works as an ideal voltage generator. (In special cases the SICOFI output impedance of about 10 Ω may be included in the SLIC model.)

According to the above remarks the equations can be simplified as follows:

4. $I_1 = M_{11} V_1 + M_{12} V_3$
5. $V_2 = M_{21} V_1 + M_{22} V_3$

Not a hallucination.
The four remaining parameters M11, M12, M21, M22 fully describe the SLIC and its external circuitry. They are determined as follows:

- **M11 = \( I_1/V_1 \) with \( V_3 = 0 \)**
  - \( I_2 = 0 \), Open Circuit
  - \( V_3 = 0 \), Short Circuit

- **M12 = \( I_1/V_3 \) with \( V_1 = 0 \)**
  - \( I_2 = 0 \), Open Circuit

- **M21 = \( V_2/V_1 \) with \( V_3 = 0 \)**
  - \( V_3 = 0 \), Short Circuit

- **M22 = \( V_2/V_3 \) with \( V_1 = 0 \)**
  - \( V_3 = 0 \), Short Circuit

*Figure 6: Definition of M-Parameters*
Each M-parameter is then expressed in the SLIC program as an algebraic equation, containing a combination of the various SLIC parameters which are provided by the SLIC input file SLIC.INP. According to the values of the SLIC input data the SLIC program calculates the values of the M-parameters as a function of frequency and writes them to an output file SLIC.SLI. The values of each M-parameter for frequencies between 10 Hz and 3990 Hz in steps of 10 Hz are written into a table (see chapter 3.3).

SLIC.SLI then serves for the interface between the SLIC program and the SICOFI program. The SLIC program SLIC.EXE and its source file SLIC.FOR are provided for fixed SLICs (see hereunder listed SLIC programs) and can be modified by the user to suit his peculiar application.

SLIC programs provided on the Siemens floppy disk STS 2060:

- HARRIS.EXE execution program of HARRIS SLIC HC 5502
- TRAFOS.EXE execution program of a transformer SLIC
- TRAFOT.EXE with series or transverse feeding.

The following SLIC programs are also available on request:

- SGS.EXE execution program of SGS SLIC L3030
- NSGS.EXE execution program of SGS SLIC L3090
- ERIC.EXE execution program of ERICSSON SLIC PBL 3762

The user can also develop his own SLIC program using any programming language. The only condition is to respect the standard format defined for the tables of SLIC.SLI (see chapter 3.3).

Chapter 3.2 shows an example of the SLIC input file for the HARRIS SLIC 5502.

The format of the SLIC program output file SLIC.SLI is shown in chapter 3.3.
3.2 Input File Description for HARRIS SLIC

This description is an example of the SLIC input file for the HARRIS SLIC HC 5502. Figure 7 shows the interconnection of the HARRIS SLIC and the SICOFI.

**Figure 7**

Connection SICOFI®-HARRIS SLIC

**Note:** SICOFI version V 4.x already includes a programmable attenuation (AGR) in the receive path.

The input file HARRIS.INP of the HARRIS SLIC program contains the following variables, which may be changed prior to a new run of the HARRIS.EXE program:

- **Variable name:** VOR
  - **Function:** indicates the VOltage amplification factor between SICOFI and SLIC in Receive path
  - **Value:** REAL number \( V_1/V_0 = R_2/R_1 + R_2 \) if \( R_1, R_2 << R_{IR} \) e.g. \( R_1 = R_2 = 300 \Omega \)

- **Variable name:** RIR
  - **Function:** Input Resistor of the HARRIS SLIC in the Receive path
  - **Value:** in \( \Omega \), e.g. \( R_{IR} = 90000 \Omega \) (data sheet)

- **Variable name:** CKR
  - **Function:** decoupling Capacitor of the Receive path
  - **Value:** in Farad
Variable name: VOX
Function: indicates the VOltage amplification factor between SLIC and SICOFI in transmit (Xmit) path.
Value: REAL number \( (V_3/V_2) \)

Variable name: RIX
Function: Input Resistor in the transmit (Xmit) path
Value: in Ohm

Variable name: CKX
Function: decoupling Capacitor of the transmit (Xmit) path.
Value: in Farad

Variable name: \( R_0 \) \( (R_0 = R_{B1} + R_{B2} + R_{B3} + R_{B4}) \)
Function: controls the impedance matching (with help of SICOFI Z-filter it can be very simple (REAL))
Value: in Ohm (REAL value)

Variable name: ZSLI
Function: minimal attenuation (resp. maximal gain) of the SLIC 4-wire side. Used by the SICOFI program during automatic calculation of Z-filter coefficients to check any possible overload in SICOFI Z-filter – SLIC loop (see figure 8)
Value: in dB (must be expressed as attenuation: \( -20 \times \log (V_T/V_R) \))
Practical use: must be measured before using the SLIC and the SICOFI programs. It can be changed with an editor.
**Note:** The attenuation of the closed loop “Z filter – SLIC” must be greater than 1 (gain < 0 dB) in the frequency band 0 – 16 kHz in order to avoid any overload or oscillation.

The user has to measure the attenuation of the loop "SLIC input to SLIC output" over the whole frequency band 0 – 16 kHz for different terminating impedances.

The worst case (the smallest attenuation resp. the greatest gain) has then to be declared under the variable named ZSLI.

---

**Figure 8**

**ZSLI Definition**

Example: 3.5 dB gain in the loop "SLIC input to SLIC output": ZSLI = –3.5
3.3 Output File Description, Format of the M-Parameter Table

The output file of the SLIC program has to be named "***.SLI".

The SICOFI program expects a table as shown in **figure 9**.

**Figure 9**
Format of the M-Parameter Table

* HARRIS SLIC
* VOR = 0.50000  RIR = 90000.  CKR = 1.000E-06  Comment
* VOX = 1.00000  RIX = 0.10000E+06  CKX = 1.000E-06  lines
* R0  = 600.00

ZSLI  worst case half loop value
0.50000

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<th>REAL</th>
<th>IMAG</th>
<th>keyword</th>
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<td><strong>IMAG</strong></td>
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<td></td>
</tr>
<tr>
<td><strong>M21-TABLE</strong></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>10.000000</td>
<td>9.752955E-01</td>
<td>1.552231E-01</td>
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<tr>
<td>20.000000</td>
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<td>7.907671E-02</td>
<td></td>
</tr>
<tr>
<td>........</td>
<td>.................</td>
<td>...............</td>
<td></td>
</tr>
<tr>
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<td>9.999999E-01</td>
<td>3.998867E-04</td>
<td></td>
</tr>
<tr>
<td>3990.000000</td>
<td>9.999999E-01</td>
<td>3.988845E-04</td>
<td></td>
</tr>
<tr>
<td><strong>M22-TABLE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
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<td>-3.177564E-01</td>
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<td>20.000000</td>
<td>-9.790611E-01</td>
<td>-1.656447E-01</td>
<td></td>
</tr>
<tr>
<td>........</td>
<td>.................</td>
<td>...............</td>
<td></td>
</tr>
<tr>
<td>3980.000000</td>
<td>-9.999999E-01</td>
<td>-8.442052E-04</td>
<td></td>
</tr>
<tr>
<td>3990.000000</td>
<td>-9.999999E-01</td>
<td>-8.420893E-04</td>
<td></td>
</tr>
</tbody>
</table>

The first comment lines beginning with "***" document the external SLIC components. These lines are copied to the SICOFI result file.
The first column indicates the frequency value, the second one the real part value of the M-parameter at this frequency and the third one the imaginary part value.
These three values are separated by at least a single space character.
Every REAL number must contain a decimal point (e.g. 2. or 2.00).
The value of the variable ZSLI of the SLIC input file is obligatorily declared again in this file.
4 SICOFI® Program Description

The actual SICOFI program section starts with an overview of the SICOFI program features. Then it describes the different input files of the SICOFI program like the CONTROL file, SPECIFICATION file and the BYT file. At the end of this chapter you will find a description of the SICOFI RESULT file with additional explaining comments.

4.1 Program Functions

The SICOFI program has been developed to help the user in adapting the SICOFI to his particular application.

It allows him:
- to find the optimal set of coefficients of each SICOFI filter and to calculate the theoretical transfer functions of the whole circuit SICOFI-SLIC (return loss, transhybrid loss, frequency responses, …) (Command OPT).
- to simulate the transfer functions of a part of the circuit SICOFI-SLIC and to perform some tolerance analysis (Command SIM).

The SICOFI program is user friendly.
Without exiting the program one can:
- modify the value of the variables in the control file (SICOFI.CTL) and interchange input files (Command DATA).
- use abbreviations for the variable units (powers of ten).
- store a calculation session in a file (Command ECHO).
- generate a USER.BYT file newest to the set of coefficients optimized (Command BYT).
- store in a file some intermediate results or the final ones (Command RES).
- access help files (Command HELP).
- use DOS commands (Command DOS).
- start a SLIC calculation without leaving the program.
- program the SICOFI testboard with a RS232 interface program.

A command line which shows the above mentioned commands is always presented after a filter calculation run at the bottom of the screen.

4.2 Control File: SICOFI.CTL

This file contains the data controlling the optimization and simulation processes. A control file HARRIS.CTL is given at the end of this variable list on chapter 4.2. If not adversely noted, variables may be changed during a session (use command DATA).

Variable name: SPEC
Abbreviation meaning: SPECification file name.
Function: indicates in which file the specifications to be fulfilled are described.

Value: the name of an existing file!

Practical use: the file has to be prepared with the editor before running the program. For different countries peculiar SPEC-files may be prepared. The SPEC file name can be changed during the session (command DATA). The extension name must be ***.SPE.

Variable name: SLIC
Abbreviation meaning: SLIC program output file.
Function: indicates the name of the output file of the SLIC which contains the SLIC parameters.
Value: give the name of an existing file!
Practical use: the file is generated by the SLIC program and it can be changed during the session by changing the name (SLIC = OTHER.SLI) with command DATA. The extension name must be ***.SLI.

Variable name: VERSION
Abbreviation meaning: VERSION of the SICOFI which coefficients have to be calculated.
Function: indicates the version of the SICOFI in order that the program can take the adequate SICOFI transfer functions into account.
Value: Vx.y (e.g. V3.1, V4. x …)

Variable name: REL
Abbreviation meaning: RELative question flag
Function: indicates whether the values of the transfer functions in simulation mode are relative (refering to values at FREF) or absolute.
Value: Y (relative) or N (absolute)
Variable name: BYTE
Abbreviation meaning: reference BYTE file.
Function: indicates the name of the reference file used to generate a new file consisting of the Peripheral Board Controller macrocommands combined with the newly calculated coefficients.
Value: give the name of an existing file!
Practical use: the reference file must be prepared with an editor before running the session but the name can be changed during the session (command DATA). The extension name must be ***.BYT.

Variable name: CHNR
Abbreviation meaning: CHannel NummbeR.
Function: indicates for which SIP-line (0 … 7) and which channel (A or B) the macrocommands of the reference file have to be updated.
Value: CHNR = 0, A for SIP line 0 and voice channel A.

Variable name: PLQ
Abbreviation meaning: PLot Question flag.
Function: the calculated transfer functions ZIN, AD, DA and DD are stored together with the corresponding specification masks by the command RES. This will provide the possibility to plot the result curves together with the specification masks.
Value: Y or N.
Practical use: **Note:** You may generate a plot table with the command 4 SIM. This plot file is stored with the command 6 RES. The screen plot program is not available with the present program version (3.0), but the user may use his own plot program to display the prepared plot data.

Variable name: FSTA
Abbreviation meaning: plot Frequency STArt.
Function: defines at which frequency the plot starts.
Value: in Hz (FSTA > 0 Hz).
Practical use: Data valid only when PLQ = Y.
<table>
<thead>
<tr>
<th>Variable name:</th>
<th>FSTO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>plot Frequency STOp.</td>
</tr>
<tr>
<td>Function:</td>
<td>defines at which frequency the plot stops.</td>
</tr>
<tr>
<td>Value:</td>
<td>in Hz (FSTO &lt; 4000 Hz).</td>
</tr>
<tr>
<td>Practical use:</td>
<td>Data valid only when PLQ = Y. You must define: FSTO &gt; FSTA.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable name:</th>
<th>STEP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>plot frequency STEP.</td>
</tr>
<tr>
<td>Function:</td>
<td>defines the frequency step used for calculation of the plot results.</td>
</tr>
<tr>
<td>Value:</td>
<td>in Hz.</td>
</tr>
<tr>
<td>Practical use:</td>
<td>Data valid only when PLQ = Y.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable name:</th>
<th>ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>SICOFI filters switched ON.</td>
</tr>
<tr>
<td>Function:</td>
<td>defines which filters are switched on for the optimization and simulation process.</td>
</tr>
<tr>
<td>Value:</td>
<td>All or a combination of Z, X, R, GX, GR and B: e.g. ON = Z or ON = Z + R + X + B or ON = ALL</td>
</tr>
<tr>
<td>Practical use:</td>
<td>You must declare variables ON or OFF.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable name:</th>
<th>OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>SICOFI filters switched OFF.</td>
</tr>
<tr>
<td>Function:</td>
<td>defines which filters are switched off during the optimization and simulation process.</td>
</tr>
<tr>
<td>Value:</td>
<td>All or a combination of Z, X, R, GX, GR and B: e.g. OFF = R + X + B or OFF = ALL</td>
</tr>
<tr>
<td>Practical use:</td>
<td>You must declare variables ON or OFF.</td>
</tr>
</tbody>
</table>
Variable name: SHORT
Abbreviation meaning: SHORT display flag
Function: flag which indicates that the results will be displayed in a short form.
No: display of the calculated coefficients and of all the transfer functions.
Yes: neither the calculated coefficients nor the return loss and trans-hybrid loss are displayed.
For Z and B filters only the minimum reserve to or the maximum violation of corresponding specifications are displayed.
Value: Y (Yes) or N (No)

Variable name: OPT
Abbreviation meaning: OPTimization of the SICOFI filter coefficients
Function: indicates the filters for which the program will calculate the coefficients.
Value: ALL or a combination of Z, X, R and B
  e.g. OPT = Z or OPT = Z + R + X + B or OPT = ALL.
  GR and GX filters are optimized at the same time as the R and X filters respectively.
Practical use: An optimization starts with the command OPT.

Variable name: SIM
Abbreviation meaning: SIMulation of different transfer paths.
Function: indicates the path of the circuit SICOFI-SLIC which transfer function will be simulated.
The different transfer functions, which can be simulated, are explained in chapter 5.6 (command SIM).
Value: ALL or a combination of ZIN, AD, DA, DD, ASI, ASO, DSI, DSO (e.g. ZIN + DSI)
Practical use: A simulation starts with the command SIM.
<table>
<thead>
<tr>
<th>Variable name:</th>
<th>ZXRB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>Calculation status of the Z-, X-, R- and B-filter respectively.</td>
</tr>
<tr>
<td>Function:</td>
<td>indicates the calculation status: Which filter coefficients have already been calculated?</td>
</tr>
<tr>
<td>Value:</td>
<td>N (New), O (old) or X (not calculated).</td>
</tr>
<tr>
<td>Practical use:</td>
<td>Is simply an indicator to the user which must not be changed during the session.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable name:</th>
<th>ZAUTO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>AUTOMATIC calculation flag of the Z filter coefficients.</td>
</tr>
<tr>
<td>Function:</td>
<td>indicates whether the program is to use mathematical algorithms to optimize the Z filter coefficients (automatic calculation), or the sampling points FZP defined by the variables PZIN, PSP, WFZ (no automatic calculation).</td>
</tr>
<tr>
<td>Value:</td>
<td>Y (automatic) or N (no automatic calculation)</td>
</tr>
<tr>
<td>Practical use:</td>
<td>Note: ZAUTO was previously defined by PZIN = 0. During the automatical calculation, an iteration number appears on the screen to show the progression of the program and indicates how close the program is to a satisfying result. As soon as the iteration number turns negative, the result is fulfilling the required specifications. The more negative the result is, the better it is.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable name:</th>
<th>PZIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>number of sampling Points for Z-filter calculation within the speechband.</td>
</tr>
<tr>
<td>Function:</td>
<td>indicates the number of frequency sampling points of the Z filter within the speech band (100 Hz &lt; FREQ &lt; 3400 Hz) if the Z filter coefficients are not automatically optimized (ZAUTO = N).</td>
</tr>
<tr>
<td>Value:</td>
<td>between 5 and 20 (One must have: 5 &lt; PZIN + PSP &lt; 20).</td>
</tr>
<tr>
<td>Practical use:</td>
<td>Experience has shown that the optimum value for PZIN is between 8 and 13.</td>
</tr>
</tbody>
</table>
Variable name: PSP
Abbreviation meaning: number of sampling Points in Stop band
Function: indicates the number of frequency sampling points of the Z filter out of the speech band (3400 Hz < FREQ < 16000 Hz) if the Z filter coefficients are not automatically optimized (ZAUTO = N).
Value: PSP must fulfill the following condition: 5 < PZIN + PSP < 20.
Practical use: Experience has shown that PSP = 3 is the optimum value.

Variable name: FZP
Abbreviation meaning: Frequency points for Z-filter calculation
Function: indicates the frequency of the sampling points of the Z filter in non-automatic (ZAUTO = N) optimization mode (PZIN + PSP values are expected).
Value: between 100 and 16000 Hz.
Practical use:
- FZP (2) = 500, 2.0
  changes Z-filter frequency point (2) to new frequency (500 Hz) and new weighting factor (2.0).
  The user may also change all sampling frequency points:
  FZP = 350, 450, 1000, 1300, 1600, 2000, 2500, 2800, 3000, 3200, 3400, 8000, 10000, 13000

Variable name: WFZ
Abbreviation meaning: Weighting Factors for Z filter.
Function: indicates the weighting factors assigned to individual frequency sampling points FZP of the Z filter in non automatic optimization mode (ZAUTO = N). PZIN and PSP weighting factors are expected.
Value: INTEGER value.
Practical use:
Experience has shown that the values of WFZ preferably are between 0.1 and 10.0. They can be changed during the session (command DATA).
WFZ = 1.0, 1.5, 1.5, 2.0, 2.0, 1.5, 1.0, 1.0, 1.0, 1.0, 1.0, 1.0, 1.0, 1.0
changes all the weighting factors for the frequency points defined in FZP. If different frequency points have a relative high weighting factor, the program tries to calculate good results at this points, but the results at other frequencies may become worse.
Variable name: FZ
Abbreviation meaning: Frequency range for Z-filter calculation. In automatic optimization mode (ZAUTO = Y) FZ indicates the frequency band to which optimization applies (2 values are expected).
Value: The range should be within the limits defined in the actual specification file:
FZ = 300 3400
Practical use: FZ = 500 3200 defines a new optimization range for the Z-filter.

Variable name: ZLIM
The value of this variable has to be changed only in special cases ... See its description in chapter 7.1.

Variable name: ZREP
Abbreviation meaning: REPeat flag of Z filter automatic calculation
Function: indicates whether or not the automatic optimization of Z filter coefficients will be restarted from precalculated values.
Value: Y (Yes) or N (No).

Variable name: ZSIGN
The value of this variable has to be changed only in special cases. See its description in chapter 7.1. Most of the time ZSIGN = 1.
Variable name: FR
Abbreviation meaning: Frequency band for R filter calculation
Function: indicates the frequency band which the optimization of the R filter coefficients applies.
Value: two INTEGER values within the speech band. The range should be within the limits defined in the actual specification file:
FR = 300 3400

Variable name: RDISP
Abbreviation meaning: R filter frequency response DISPlay flag
Function: indicates whether or not the absolute frequency response of the R filter alone will be displayed.
Value: Y (Yes) or N (No).
Practical use: Note: In software versions prior to V3.0 RDISP was defined by RFIL.

Variable name: RREFQ
The value of this variable has to be changed only in special cases ... See its description in chapter 7.1. Most of the time RREFQ = N.

Variable name: RREF
The value of this variable has to be changed only in special cases ... See its description in chapter 7.1.

Variable name: FX
Abbreviation meaning: Frequency band for X filter calculation
Function: indicates the frequency band to which the optimization of the X filter coefficients applies.
Value: two INTEGER values within the speech band:
FX = 300 3400
Variable name: XDISP
Abbreviation meaning: X filter frequency response DISPlay flag
Function: indicates whether or not the absolute frequency response of the X filter alone will be displayed.
Value: Y (Yes) or N (No).
Practical use: Note: XDISP was previously defined by XFIL

Variable name: XREFQ
The value of this variable has to be changed only in special cases ... See its description in chapter 7.1. In general XREFQ = N.

Variable name: XREF
The value of this variable has to be changed only in special cases ... See its description in chapter 7.1.

Variable name: BAUTO
Abbreviation meaning: AUTOmatic calculation flag of the B filter coefficients.
Function: indicates whether the program uses mathematical algorithms to optimize the B filter coefficients (automatic calculation) or the sampling points FBP defined by the variables PB, GWFB, WFB (non-automatic calculation). (see also ZAUTO)
Value: Y (automatic) or N (non-automatic)
Practical use: Note: BAUTO was previously defined by PB = 0

Variable name: PB
Abbreviation meaning: number of sampling Points for B filter calculation
Function: indicates the number of frequency sampling points of the B filter within the speech band (100 Hz < FREQ < 3400 Hz) if the B filter coefficients are not automatically optimized (BAUTO = N).
Value: between 10 and 20.
Practical use: the program uses the sampling points defined in the control file to calculate the B filter coefficients. Experience has shown that the optimum value for PB is around 10.
Variable name: GWFB
Abbreviation meaning: General Weighting Factors for B filter.
Function: indicates the general weighting factor of the B filter in non-automatic optimization mode (BAUTO = N).
Value: REAL.
Practical use: Experience has shown that the optimum value for GWFB is between 0.01 and 0.1.

Variable name: FBP
Abbreviation meaning: Frequencies of sampling Points for B filter calculation
Function: indicates the frequencies of the sampling points for B filter calculation in non-automatic optimization mode (PB values are expected).
Value: value between 100.0 and 3400.0 Hz.
Practical use: 
FBP (3) = 800, 1.5 changes B-filter frequency point (3) to new frequency (800 Hz) and new weighting factor (1.5).
The user may also change all sampling frequency points: FBP = 350, 450, 800, 1000, 1600, 2000, 2500, 2800, 3200, 3300

Variable name: FB
Abbreviation meaning: Frequency range for B filter calculation
Function: In automatic optimization mode (BAUTO = Y) FB indicates the sampling frequency band (2 values are expected):
FB = 300 3400
Value: the range should be within the limits defined in the actual specification file.
Practical use: FB = 500 3200 defines a new optimization range for the B filter.
Variable name: WFB
Abbreviation meaning: Weighting Factors for B filter.
Function: indicates the weighting factors of the individual sampling frequency points of the B filter in non-automatic optimization mode (BAUTO = N).
Value: REAL value.
Practical use: Experience has shown that the values of WFB are between 0.5 and 5.0. WFB = 3.0, 2.5, 2.0, 1.0, 1.0, 1.0, 1.0, 1.0, 1.0, 1.0 changes all the weighting factors for the frequency points defined in FBP. If different frequency points have a relative high weighting factor, the program tries to calculate good results at this points, but the results at other frequencies may become worse.

Variable name: BDF
Abbreviation meaning: B-Delay Filter
Function: indicates the delay factor of the B filter in multiples of 62.5 micro sec.
Value: 0, 1, 2 or 3 (× 62.5 micro sec.).
Practical use: Experience has shown that the optimum value is mostly BDF = 1.
Practical use: Note: In software versions prior to V3.0 BDF was defined by TBM.

Variable name: BLIM
The value of this variable has to be changed only in special cases ... See its description in chapter 7.1.

Variable name: BREP
Abbreviation meaning: REPeat flag of B filter automatic calculation
Function: indicates whether or not the automatic optimization of B filter coefficients will be restarted from already calculated values.
Value: Y (Yes) or N (No).

Variable name: BSIGN
The value of this variable has to be changed only in special cases ... See its description in chapter 7.1. In general BSIGN = 1.
Variable name: DPOF  
Abbreviation meaning: supplementary Delay after the SICOFI POst-Filter  
Function: Allows the insertion of an additional group delay in receive path between the SLIC and the SICOFI.  
Value: in seconds.  
Practical use: See also special application described in chapter 7.1.

Variable name: DPRE  
Abbreviation meaning: supplementary Delay before the SICOFI PRE-filter  
Function: Allows the insertion of an additional group delay in transmit path between the SLIC and the SICOFI.  
Value: in seconds.  
Practical use: See also special application described in chapter 7.1.

Variable name: APOF  
Abbreviation meaning: supplementary Amplification after the SICOFI POst-Filter  
Function: Allows the insertion of an additional attenuation in receive path between the SLIC and the SICOFI.  
Value: in dB.  
Practical use: See also special application described in chapter 7.1.

Variable name: APRE  
Abbreviation meaning: supplementary Amplification before the SICOFI PRE-filter  
Function: Allows the insertion of an additional attenuation in transmit path between the SLIC and the SICOFI.  
Value: in dB.  
Practical use: See also special application described in chapter 7.1.
Variable name: AGX
Abbreviation meaning: Analog Gain control transmit-path (Xmit) of SICOFI.
Function: Allows an additional amplification in transmit path of SICOFI.
Value:
- AGX = 00  0 dB
- AGX = 01  6 dB amplification
- AGX = 10  12 dB amplification
- AGX = 11  14.2 dB amplification

Practical use: AGX is used for SICOFI versions V 4.1 or later. It is programmed by the SICOFI configuration register CR3.

Variable name: AGR
Abbreviation meaning: Analog Gain control receive-path of SICOFI.
Function: Allows an additional attenuation in receive path of SICOFI.
Value:
- AGR = 00  0 dB
- AGR = 01  6 dB attenuation
- AGR = 10 12 dB attenuation
- AGR = 11 14.2 dB attenuation

Practical use: AGR is used for SICOFI versions V 4.1 or later. It is programmed by the SICOFI configuration register CR3.

Variable name: TM3
Abbreviation meaning: Test Mode of SICOFI:
Additional digital gain in transmit path
Function: Allows an additional digital amplification in transmit path of SICOFI.
Value:
- TM3 = 000  0 dB
- TM3 = 001  6 dB amplification
- TM3 = 011 12 dB amplification

Practical use: TM3 is used for SICOFI versions V 4.1 or later. It is programmed by the SICOFI configuration register CR4.
The quantization steps of the SICOFI GX filter are relative high in the range of 8 to 12 dB. By programming TM3 you may find a GX amplification range with smaller quantization steps in the range 0 to 8 dB. Additional programming of TM3 is allowed which is not used in the SICOFI coefficients program:
- TM3 = 100  Enable on chip sine wave generation
- TM3 = 110  Far analog loop back
4.2.1 Listing of the SICOFI Control File HARRIS.CTL

SPEC = BRD.SPE  SLIC = HARRIS.SLI
BYTE = REF.BYT  CHNR = 0,A
VERSION = 4.2  REL = Y
ON = ALL
OPT = Z+X+R+B  ZXR = NNNN
ZAUTO = N  PZIN = 11  PSP = 3
FZP = 300.0  500.0  1000.0  1300.0  1500.0
  2000.0  2500.0  2900.0  3000.0  3200.0
  3400.0  7000.0  10000.0  14000.0.
WFZ = 0.100  1.00  2.00  1.50  1.00
  3.00  1.00  1.00  1.00  3.00
  2.80  1.00  1.00  1.00  1.00
FR 300.00  3400.0
RDISP = Y  RREFQ = N
FX 300.00  3400.0
XDISP = Y  XREFQ = N
BAUTO = N  PB = 10  GWFB = 0.500E-01  BDF = 1
FBP = 300.0  500.0  700.0  1000.0  1500.0
  2100.0  2300.0  2900.0  3200.0  3300.0.
WFB = 4.000  2.000  1.000  5.000  1.000
  2.000  1.000  5.000  1.000  1.000
APRE = 0.0  DPRE = 0.0  APOF = 0.0  DPOF = 0.0
AGR = 00  AGX = 00  TM3 = 000
;

4.3 Specification File: COUNTRY.SPE

This file defines the national specifications which must be fulfilled. A specification file BRD.SPE containing the particular specifications for the Federal Republic of Germany is given at the end of this variable list on chapter 4.3.3. Values of variables may be changed by using a common editor (Using command DOS).

Variable name: FREF
Abbreviation meaning: Frequency REFerence.
Function: indicates the reference frequency all calculations and frequency responses are referred to.
Value: in Hz, e.g. FREF = 1014.
Practical use: Once defined for an application it does not need to be modified.

Variable name: LAW
Abbreviation meaning: Compression/expansion LAW.
Function: defines the law according to which the 16 bit word is compressed (resp. the 8 bit word is expanded).
Value: A or U.
Practical use: Once defined for an application it does not need to be modified.

Variable name: VREF
Abbreviation meaning: REFerence Voltage.
Function: equals the reference voltage defined by the PTT (Telecom Authority). The reference voltage is the resulting voltage at the reference impedance ZR, if 1 mW of power of frequency FREF are applied.
VREF = SQRT (0.001* ZR).
Value: in V.
Practical use: Once defined for an application it does not need to be modified. Instead of using this reference voltage VREF you may use the country specific reference impedance ZR (see ZRRP1, ZRCP1, ZRRP2, ZRCP2, ZRRS, ZRCS). Then the SICOFI program automatically calculates the corresponding reference voltage.
<table>
<thead>
<tr>
<th>Variable name:</th>
<th>ZRRP1, ZRCP1, ZRRP2, ZRCP2, ZRRS, ZRCS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>resistors and capacitors of the impedance ZR (see circuit library in chapter 4.3.2).</td>
</tr>
<tr>
<td>Function:</td>
<td>ZR defines the impedance used to calculate the reference voltage if this one is not explicitly declared.</td>
</tr>
<tr>
<td>Value:</td>
<td>resistors in Ohm and capacitors in Farad.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable name:</th>
<th>RLX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>Relative Level of the Xmit signal.</td>
</tr>
<tr>
<td>Function:</td>
<td>indicates the relative levels on the a,b line of the transmit signal with the reference level (0 dBm0) on the digital side.</td>
</tr>
<tr>
<td>Value:</td>
<td>in dBr.</td>
</tr>
<tr>
<td>Practical use:</td>
<td>See sign convention explained in chapter 4.3.1.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable name:</th>
<th>RLR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>Relative Level of the Receive signal.</td>
</tr>
<tr>
<td>Function:</td>
<td>indicates the relative level on the a,b line of the receive signal with the reference level (0 dBm0) on the digital side.</td>
</tr>
<tr>
<td>Value:</td>
<td>in dBr.</td>
</tr>
<tr>
<td>Practical use:</td>
<td>See sign convention explained in chapter 4.3.1.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable name:</th>
<th>ABIMP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abbreviation meaning:</td>
<td>A, B -wire IMPedance</td>
</tr>
<tr>
<td>Function:</td>
<td>indicates the terminating impedance of the a,b line used for the measurements of the frequency response.</td>
</tr>
<tr>
<td>Value:</td>
<td>&quot;ZI&quot; or &quot;Z3&quot;.</td>
</tr>
<tr>
<td>Practical use:</td>
<td>This impedance is not being considered in calculating the return loss and transhybrid loss. (see ZIRP1, ZICP1, ZIRP2, ZICP2, ZIRS, ZICS and Z3RP1, Z3CP1, Z3RP2, Z3CP2, Z3RS, Z3CS).</td>
</tr>
</tbody>
</table>
Variable names: ZIRP1, ZICP1, ZIRP2, ZICP2, ZIRS, ZICS
Abbreviation meaning: resistors and capacitors of impedance equivalent circuit "ZI" (see circuit library in chapter 4.3.2).
Function: "ZI" defines the input impedance which the line card has to present from a,b line.
Value: resistors in Ohm and capacitors in Farad.

Variable names: ZLRP1, ZLCP1, ZLRP2, ZLCP2, ZLRS, ZLCS
Abbreviation meaning: resistors and capacitors of impedance equivalent circuit "ZL" (see circuit library in chapter 4.3.2).
Function: "ZL" defines the load impedance used for digital to digital measurements and calculations (e.g. echo return loss).
Value: resistors in Ohm and capacitors in Farad.

Variable names: Z3RP1, Z3CP1, Z3RP2, Z3CP2, Z3RS, Z3CS
Abbreviation meaning: resistors and capacitors of impedance equivalent circuit "Z3" (see circuit library in chapter 4.3.2).
Function: "Z3" defines a terminating impedance used for analog to digital and digital to analog measurements when ABIMP = Z3.
Value: resistors in Ohm and capacitors in Farad.
The following variables define specification masks.

A mask can be described as a table as follows:

- **FR** defines the frequency at which the mask value changes.
- **AT–** defines the lower threshold value of the mask at the frequency FR.
- **AT+** defines the higher threshold value of the mask at the frequency FR.

Example: **figure 10** defines the mask of the return loss.

![Figure 10: Specification Mask](image)

**Figure 10**
**Specification Mask**

In the specification file the following specification masks can be described:

- **Variable name:** ZRE
  - **Function:** defines the mask of the return loss.
  - **Value:** FR in Hz, AT– and AT+ in dB.

- **Variable name:** ZMIR
  - This variable does not need to be modified by the user. It is described in **chapter 7.1**.

- **Variable name:** DA, UPPER
  - **Function:** defines the upper bound of the specification mask of the frequency response in receive path (D/A).
  - **Value:** FR in Hz, AT– and AT+ in dB.
Variable name: DA, LOWER
Function: defines the lower bound of the specification mask of the frequency response in receive path (D/A).
Value: FR in Hz, AT– and AT+ in dB.

Variable name: DA, DELAY
Function: defines the specification mask of the group delay in receive path (D/A).
Value: FR in Hz, AT– and AT+ in ms.

Variable name: AD, UPPER
Function: defines the upper bound of the specification mask of the frequency response in transmit path (A/D).
Value: FR in Hz, AT– and AT+ in dB.

Variable name: AD, LOWER
Function: defines the lower bound of the specification mask of the frequency response in transmit path (A/D).
Value: FR in Hz, AT– and AT+ in dB.

Variable name: AD, DELAY
Function: defines the specification mask of the group delay in transmit path (A/D).
Value: FR in Hz, AT– and AT+ in ms.

Variable name: DD
Function: defines the mask of the transhybrid loss
Value: FR in Hz, AT– and AT+ in dB.
4.3.1 Sign Convention for Relative Levels

For a transmission system the relative levels are defined in dBr corresponding to the reference level 0 dBm0 of the signal at the reference point as shown below.

This convention is used in the SICOFI program and has to be applied to the circuit SICOFI-SLIC to determine the correct signs of the variables RLX and RLR.

The circuit SICOFI-SLIC can be described with separated transmit and receive paths as shown below.

Or drawn from another viewpoint:

If \( A \) is the gain in transmit direction \( (A = 20 \log \frac{V_0}{V_{ab}}) \), then RLX = \(-A\) dBr.

If \( B \) is the gain in receive direction \( (B = 20 \log \frac{V_{ab}}{V_0}) \), then RLR = \(+B\) dBr.
4.3.2 Circuit Library

The impedance used in the SICOFI Coefficient Program are all described in terms of the equivalent circuit diagram shown below:

Impedance $Z^*$ is e.g. $Z_i$, $Z_L$, $Z_3$ or $Z_R$.

- $Z_i$ defines the input impedance which the line card has to present to a,b line.
- $Z_L$ is the load impedance used for digital to digital measurements.
- $Z_3$ defines a terminating impedance used for analog to digital and digital to analog measurements when $ABIMP = Z_3$.
- $Z_R$ is the reference impedance for calculation of the reference voltage $V_{REF}$ ($Z_R$ or $V_{REF}$ may be used to define the reference).
4.3.3 Listing of the SiCOFI® Specification File BRD.SPE

FREF = 1014.0  LAW = A
VREF = 0.9480  RLX = 0.  RLR = -7.0
ABIMP = ZI
ZLRP1 = 820.  ZLCP1 = 0.  ZLRP2 = 0.  ZLCP2 = 0.115E-06
ZLRS = 220.  ZLCS = 0.
ZIRP1 = 820.  ZICP1 = 0.  ZIRP2 = 0.  ZICP2 = 0.115E-06
ZIRS = 220.  ZICS = 0.
Z3RP1 = 820.  Z3CP1 = 0.  Z3RP2 = 0.  Z3CP2 = 0.115E-06
Z3RS = 220.  Z3CS = 0.
ZRRP1 = 820.  ZRCP1 = 0.  ZRRP2 = 0.  ZRCP2 = 0.115E-06
ZRRS = 220.  ZRCS = 0.

ZRE
FR  300  500  3k  3.4k
AT– 0  20  20  16
AT+ 16  20  20  0

ZMIR
FR  4k  12k
AT– 30  3
AT+ 30  3

DA,UPPER
FR  300  500  2.7k  3k  3.4k
AT– 100  .75  .25  .35  .75
AT+ .75  .25  .35  .75  100

DA,LOWER
FR  300  3.4k
AT– 0  –.25
AT+ –.25  0

DA,DELAY
FR  500  600  1k  2.6k  2.8k
GD– 10k  .420  .150  .085  .150
GD+ .420  .150  .085  .150  10k

AD,UPPER
FR  300  500  2.7k  3k  3.4k
AT– 100  .75  .25  .35  .75
AT+ .75  .25  .35  .75  100
### Listing of the SICOFI® Specification File BRD.SPE (cont’d)

<table>
<thead>
<tr>
<th>AD, LOWER</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>FR</td>
<td>300</td>
<td>3.4k</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AT⁻</td>
<td>0</td>
<td>-.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AT⁺</td>
<td>-.25</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AD, DELAY</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>FR</td>
<td>500</td>
<td>600</td>
<td>1k</td>
<td>2.6k</td>
<td>2.8k</td>
</tr>
<tr>
<td>GD⁻</td>
<td>10k</td>
<td>.420</td>
<td>.150</td>
<td>.085</td>
<td>.150</td>
</tr>
<tr>
<td>GD⁺</td>
<td>.420</td>
<td>.150</td>
<td>.085</td>
<td>.150</td>
<td>10k</td>
</tr>
<tr>
<td>DD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FR</td>
<td>300</td>
<td>500</td>
<td>2.5k</td>
<td>3.4k</td>
<td></td>
</tr>
<tr>
<td>AT⁻</td>
<td>0</td>
<td>27</td>
<td>27</td>
<td>23</td>
<td></td>
</tr>
<tr>
<td>AT⁺</td>
<td>23</td>
<td>27</td>
<td>27</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
4.4 Byte File: USER.BYT

This file contains the commands used by the program RS 232 to program the SICOFI Test Board STUT 2060 from the Peripheral Board Controller PBC (see chapter 5.4). The calculated SICOFI coefficients are the same as in the SICOFI-Application: HARRIS SLIC HC 5502.

The table below gives the meaning of the different commands.

<table>
<thead>
<tr>
<th>Command</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSR = 36</td>
<td>Defines the phase shift on PCM Highway between the frame synchronization pulse SYP of the PBC and the PCM time slots.</td>
</tr>
<tr>
<td>CAM00 = 41</td>
<td>Assignment of the time slots.</td>
</tr>
<tr>
<td>CAM20 = 40</td>
<td>Assignment of the time slots.</td>
</tr>
<tr>
<td>CIWO = 26, F4, 80</td>
<td>Deactivates all SICOFI filters.</td>
</tr>
<tr>
<td>CIWO = 13, 20, BA, EA, 25, 23, 41, C1, BB</td>
<td>Writes Z filter coefficients 20, BA, EA, 25, 23, 41, C1, BB in SICOFI A of SIP0 line.</td>
</tr>
<tr>
<td>CIWO = 23, 50, C8, B5, 4A, C2, 21, 04, 90</td>
<td>Writes X filter coefficients 50, C8, B5, A4, C2, 21, 04, 90</td>
</tr>
<tr>
<td>CIWO = 2B, D0, C8, 84, DC, B1, 93, 02, 1D</td>
<td>Writes R filter coefficients D0, C8, 84, DC, B1, 93, 02, 1D</td>
</tr>
<tr>
<td>CIWO = 30, A0, 11, 20, 92</td>
<td>Writes GX and GR filter coefficients A0, 11, 20, 92</td>
</tr>
<tr>
<td>CIWO = 03, C4, 12, 23, 32, 72, B9, B2, BA</td>
<td>Writes B filter coef. (1st part) C4, 12, 23, 32, 72, B9, B2, BA</td>
</tr>
<tr>
<td>CIWO = 0B, 00, 97, FD, C8, DD, 4C, C2, BC</td>
<td>Writes B filter coef. (2nd part) 00, 97, FD, C8, DD, 4C, C2, BC</td>
</tr>
<tr>
<td>CIWO = 18, 19, 19, 11, 19</td>
<td>Writes B-Delay filter coefficients 19, 19, 11, 19</td>
</tr>
<tr>
<td>SIG0 = C0</td>
<td>Writes signaling byte C0.</td>
</tr>
<tr>
<td>CIWO = 26, F4, 78</td>
<td>Activates all SICOFI filters.</td>
</tr>
</tbody>
</table>
### 4.5 Listing and Description of the RESULT.RES File

The following pages comment the contents of the result file HARRIS.RES.

<table>
<thead>
<tr>
<th>Input_file_name: HARRIS.CTL</th>
<th>Date: 31.01.89 15:56</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPEC = BRD.SPE</td>
<td>SLIC = HARRIS.SLI</td>
</tr>
<tr>
<td>BYTE = REF.BYT</td>
<td>CHNR = 0,A</td>
</tr>
<tr>
<td>PLQ = N</td>
<td></td>
</tr>
<tr>
<td>ON = ALL</td>
<td>VERSION = 4.2</td>
</tr>
<tr>
<td>OPT = Z+X+R+B</td>
<td>SHORT = N</td>
</tr>
<tr>
<td>ZAUTO = N</td>
<td></td>
</tr>
<tr>
<td>FZ = 300.00</td>
<td>ZREP = N</td>
</tr>
<tr>
<td>FZP = 300.00</td>
<td>ZSIGN = 1</td>
</tr>
<tr>
<td>WFZ = .100</td>
<td>ZLIM = 300.00</td>
</tr>
<tr>
<td>FR = 300.00</td>
<td>RDISP = Y</td>
</tr>
<tr>
<td>RDF = 300.00</td>
<td>RREFQ = N</td>
</tr>
<tr>
<td>FX = 300.00</td>
<td>RREF = .18639</td>
</tr>
<tr>
<td>XAUTO = N</td>
<td></td>
</tr>
<tr>
<td>XZQ = .16406250E+00</td>
<td></td>
</tr>
<tr>
<td>XRQ = .94531250E+00</td>
<td></td>
</tr>
<tr>
<td>XXQ = .57226560E+00</td>
<td></td>
</tr>
</tbody>
</table>

Quantized values of the optimized coefficients

Input file: HARRIS.CTL

<table>
<thead>
<tr>
<th>Control file section of SICOFI program</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPEC = BRD.SPE</td>
</tr>
<tr>
<td>SLIC = HARRIS.SLI</td>
</tr>
<tr>
<td>BYTE = REF.BYT</td>
</tr>
<tr>
<td>CHNR = 0,A</td>
</tr>
<tr>
<td>PLQ = N</td>
</tr>
<tr>
<td>ON = ALL</td>
</tr>
<tr>
<td>OPT = Z+X+R+B</td>
</tr>
<tr>
<td>ZAUTO = N</td>
</tr>
<tr>
<td>ZREP = N</td>
</tr>
<tr>
<td>FZ = 300.00</td>
</tr>
<tr>
<td>FZP = 300.00</td>
</tr>
<tr>
<td>WFZ = .100</td>
</tr>
<tr>
<td>FR = 300.00</td>
</tr>
<tr>
<td>RDF = 300.00</td>
</tr>
<tr>
<td>FX = 300.00</td>
</tr>
<tr>
<td>XAUTO = N</td>
</tr>
<tr>
<td>XZQ = .16406250E+00</td>
</tr>
<tr>
<td>XRQ = .94531250E+00</td>
</tr>
<tr>
<td>XXQ = .57226560E+00</td>
</tr>
</tbody>
</table>
Run # 1
Z-FILTER calculation results
Reference impedance for optimization:
ZIRP1 = 820. ZICP1 = .000 ZIRP2 = 0. ZICP2 = .115E-06
ZIRS = 220. ZICS = .000
Calculated and quantized coefficients:
XZ = .16507 .26725 .21631 .09693 .01324
XZQ = .16406 .26758 .21680 .09766 .01318

Bytes for Z-Filter (13): 60,2B,A3,2B,4B,42,33,22

Returns LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>33.772</td>
<td>2000.</td>
<td>21.902</td>
</tr>
<tr>
<td>200.</td>
<td>31.952</td>
<td>2100.</td>
<td>22.372</td>
</tr>
<tr>
<td>300.</td>
<td>29.816</td>
<td>2200.</td>
<td>22.981</td>
</tr>
<tr>
<td>400.</td>
<td>28.025</td>
<td>2300.</td>
<td>23.756</td>
</tr>
<tr>
<td>500.</td>
<td>26.560</td>
<td>2400.</td>
<td>24.740</td>
</tr>
<tr>
<td>600.</td>
<td>25.362</td>
<td>2500.</td>
<td>25.993</td>
</tr>
<tr>
<td>700.</td>
<td>24.374</td>
<td>2600.</td>
<td>27.601</td>
</tr>
<tr>
<td>800.</td>
<td>23.558</td>
<td>2700.</td>
<td>29.665</td>
</tr>
<tr>
<td>900.</td>
<td>22.886</td>
<td>2800.</td>
<td>32.059</td>
</tr>
<tr>
<td>1000.</td>
<td>22.337</td>
<td>2900.</td>
<td>33.430</td>
</tr>
<tr>
<td>1100.</td>
<td>21.897</td>
<td>3000.</td>
<td>31.760</td>
</tr>
<tr>
<td>1200.</td>
<td>21.555</td>
<td>3100.</td>
<td>28.591</td>
</tr>
<tr>
<td>1300.</td>
<td>21.305</td>
<td>3200.</td>
<td>25.633</td>
</tr>
<tr>
<td>1400.</td>
<td>21.138</td>
<td>3300.</td>
<td>23.126</td>
</tr>
<tr>
<td>1500.</td>
<td>21.052</td>
<td>3400.</td>
<td>21.005</td>
</tr>
<tr>
<td>1600.</td>
<td>21.049</td>
<td>3500.</td>
<td>19.171</td>
</tr>
<tr>
<td>1700.</td>
<td>21.125</td>
<td>3600.</td>
<td>17.558</td>
</tr>
<tr>
<td>1800.</td>
<td>21.290</td>
<td>3700.</td>
<td>16.123</td>
</tr>
<tr>
<td>1900.</td>
<td>21.543</td>
<td>3800.</td>
<td>14.832</td>
</tr>
</tbody>
</table>

Theoretical return loss expected to be measured when SICOFI is programmed with the quantized values of the optimized coefficients of Z filter.
Min. Z-loop reserve: **2.944 dB at frequency: 500.0 Hz**

Min. Z-loop mirror reserve: **11.341 dB at frequency: 4000.0 Hz**

Run # 1

**X-FILTER calculation results**

Reference impedance for optimization:
- ZIRP1 = 820
- ZICP1 = .000
- ZIRP2 = 0
- ZICP2 = .115E-06
- ZIRS = 220
- ZICS = .000

Calculated and quantized coefficients:

**GX results:**
- **Min. Z-loop reserve:** 2.944 dB at frequency: 500.0 Hz
- **Min. Z-loop mirror reserve:** 11.341 dB at frequency: 4000.0 Hz

Run # 1

**X-FILTER calculation results**

Reference impedance for optimization:
- ZIRP1 = 820
- ZICP1 = .000
- ZIRP2 = 0
- ZICP2 = .115E-06
- ZIRS = 220
- ZICS = .000

Calculated and quantized coefficients:

<table>
<thead>
<tr>
<th>Z-loop reserve</th>
<th>X-loop mirror reserve</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.944 dB</td>
<td>11.341 dB</td>
</tr>
</tbody>
</table>

Calculated and quantized coefficients:

**XX** = 1.51053, .65349, .06808, .02365, .00057

**XXQ** = 1.50781, .65625, .06836, .02368, .00049

**Bytes for X-Filter (23):** 70, C8, A5, 4D, 14, 21, 02, 61

X-filter attenuation function (in dB), (always absolute values):

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>-7.059</td>
<td>.048</td>
<td>2000</td>
<td>-3.933</td>
<td>.009</td>
</tr>
<tr>
<td>200</td>
<td>-7.030</td>
<td>.047</td>
<td>2100</td>
<td>-3.675</td>
<td>.006</td>
</tr>
<tr>
<td>300</td>
<td>-6.982</td>
<td>.047</td>
<td>2200</td>
<td>-3.411</td>
<td>.003</td>
</tr>
<tr>
<td>400</td>
<td>-6.915</td>
<td>.046</td>
<td>2300</td>
<td>-3.143</td>
<td>.000</td>
</tr>
<tr>
<td>500</td>
<td>-6.830</td>
<td>.045</td>
<td>2400</td>
<td>-2.869</td>
<td>-.003</td>
</tr>
<tr>
<td>600</td>
<td>-6.726</td>
<td>.043</td>
<td>2500</td>
<td>-2.589</td>
<td>-.006</td>
</tr>
<tr>
<td>700</td>
<td>-6.606</td>
<td>.041</td>
<td>2600</td>
<td>-2.304</td>
<td>-.009</td>
</tr>
<tr>
<td>800</td>
<td>-6.469</td>
<td>.039</td>
<td>2700</td>
<td>-2.014</td>
<td>-.013</td>
</tr>
<tr>
<td>900</td>
<td>-6.318</td>
<td>.037</td>
<td>2800</td>
<td>-1.719</td>
<td>-.018</td>
</tr>
<tr>
<td>1000</td>
<td>-6.151</td>
<td>.035</td>
<td>2900</td>
<td>-1.420</td>
<td>-.022</td>
</tr>
<tr>
<td>1100</td>
<td>-5.972</td>
<td>.033</td>
<td>3000</td>
<td>-1.119</td>
<td>-.028</td>
</tr>
<tr>
<td>1200</td>
<td>-5.780</td>
<td>.030</td>
<td>3100</td>
<td>-.818</td>
<td>-.034</td>
</tr>
<tr>
<td>1300</td>
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<td>.028</td>
<td>3200</td>
<td>-.521</td>
<td>-.040</td>
</tr>
<tr>
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<td>.025</td>
<td>3300</td>
<td>-.234</td>
<td>-.047</td>
</tr>
<tr>
<td>1500</td>
<td>-5.143</td>
<td>.022</td>
<td>3400</td>
<td>-.039</td>
<td>-.054</td>
</tr>
<tr>
<td>1600</td>
<td>-4.913</td>
<td>.020</td>
<td>3500</td>
<td>.290</td>
<td>-.061</td>
</tr>
<tr>
<td>1700</td>
<td>-4.677</td>
<td>.017</td>
<td>3600</td>
<td>.511</td>
<td>-.068</td>
</tr>
<tr>
<td>1800</td>
<td>-4.435</td>
<td>.014</td>
<td>3700</td>
<td>.695</td>
<td>-.074</td>
</tr>
<tr>
<td>1900</td>
<td>-4.187</td>
<td>.011</td>
<td>3800</td>
<td>.832</td>
<td>-.078</td>
</tr>
</tbody>
</table>

**Optimized coefficients of X filter**

**Quantized values of the optimized coefficients of X filter**

**Hexadecimal codes of the optimized coefficients of X filter**

**Hexadecimal code of the coefficient operation command used to program the X filter**

**Absolute frequency response of the X filter alone**

(attenuation + group delay).

**This table is displayed only with the SICOFI control file variable XDISP = Y.**

**Reminder of the reference frequency**

**Ideal value of GX starting from the desired value of Rx**

Second byte for Gain: 13, 20, B2

**Ideal value of GX starting from the desired value of Rx**

Quantized value of GX

Hexadecimal code of the optimized coefficient of GX
Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

Group delay in transmit direction (A/D) for the voice channel A and B resp. at the reference frequency FREF.

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>Loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>Loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>13.831</td>
<td>2.520</td>
<td>2000</td>
<td>.049</td>
<td>.009</td>
</tr>
<tr>
<td>200</td>
<td>.346</td>
<td>1.784</td>
<td>2100</td>
<td>.053</td>
<td>.014</td>
</tr>
<tr>
<td>300</td>
<td>.015</td>
<td>.587</td>
<td>2200</td>
<td>.055</td>
<td>.019</td>
</tr>
<tr>
<td>400</td>
<td>.037</td>
<td>.286</td>
<td>2300</td>
<td>.057</td>
<td>.025</td>
</tr>
<tr>
<td>500</td>
<td>.034</td>
<td>.164</td>
<td>2400</td>
<td>.059</td>
<td>.032</td>
</tr>
<tr>
<td>600</td>
<td>.023</td>
<td>.102</td>
<td>2500</td>
<td>.062</td>
<td>.041</td>
</tr>
<tr>
<td>700</td>
<td>.012</td>
<td>.066</td>
<td>2600</td>
<td>.066</td>
<td>.051</td>
</tr>
<tr>
<td>800</td>
<td>.003</td>
<td>.043</td>
<td>2700</td>
<td>.072</td>
<td>.063</td>
</tr>
<tr>
<td>900</td>
<td>-.003</td>
<td>.028</td>
<td>2800</td>
<td>.081</td>
<td>.076</td>
</tr>
<tr>
<td>1000</td>
<td>-.006</td>
<td>.018</td>
<td>2900</td>
<td>.095</td>
<td>.092</td>
</tr>
<tr>
<td>1100</td>
<td>-.006</td>
<td>.011</td>
<td>3000</td>
<td>.113</td>
<td>.112</td>
</tr>
<tr>
<td>1200</td>
<td>-.003</td>
<td>.006</td>
<td>3100</td>
<td>.137</td>
<td>.136</td>
</tr>
<tr>
<td>1300</td>
<td>.002</td>
<td>.003</td>
<td>3200</td>
<td>.171</td>
<td>.166</td>
</tr>
<tr>
<td>1400</td>
<td>.008</td>
<td>.001</td>
<td>3300</td>
<td>.218</td>
<td>.207</td>
</tr>
<tr>
<td>1500</td>
<td>.016</td>
<td>.000</td>
<td>3400</td>
<td>.291</td>
<td>.260</td>
</tr>
<tr>
<td>1600</td>
<td>.024</td>
<td>.000</td>
<td>3500</td>
<td>.412</td>
<td>.337</td>
</tr>
<tr>
<td>1700</td>
<td>.031</td>
<td>.001</td>
<td>3600</td>
<td>.640</td>
<td>.455</td>
</tr>
<tr>
<td>1800</td>
<td>.038</td>
<td>.003</td>
<td>3700</td>
<td>1.145</td>
<td>.648</td>
</tr>
<tr>
<td>1900</td>
<td>.044</td>
<td>.006</td>
<td>3800</td>
<td>2.476</td>
<td>.984</td>
</tr>
</tbody>
</table>

Frequency response in transmit direction (A/D) of the set SICOFI+SLIC+external circuitry.
These are the theoretical values expected to be measured when SICOFI is programmed with the quantized values of the optimized coefficients of X filter.
Run # 1
R-FILTER calculation results

Reference impedance for optimization:
ZIRP1=  820.  ZICP1=  .000  ZIRP2=  0.  ZICP2=  .115E-06
ZIRS =  220.  ZICS =  .000

Calculated and quantized coefficients:

Calculated coefficients of R filter

Quantized values of the optimized coefficients of R filter

Hexadecimal codes of the optimized coefficients of R filter

Hexadecimal code of the COP-command used to program the R filter

R-filter attenuation function (in dB),
(always absolute values)

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>.537</td>
<td>-.008</td>
<td>2000.</td>
<td>.052</td>
<td>.011</td>
</tr>
<tr>
<td>200.</td>
<td>.522</td>
<td>-.007</td>
<td>2100.</td>
<td>.078</td>
<td>.011</td>
</tr>
<tr>
<td>300.</td>
<td>.497</td>
<td>-.006</td>
<td>2200.</td>
<td>.113</td>
<td>.011</td>
</tr>
<tr>
<td>400.</td>
<td>.465</td>
<td>-.005</td>
<td>2300.</td>
<td>.156</td>
<td>.011</td>
</tr>
<tr>
<td>500.</td>
<td>.425</td>
<td>-.003</td>
<td>2400.</td>
<td>.208</td>
<td>.010</td>
</tr>
<tr>
<td>600.</td>
<td>.381</td>
<td>-.002</td>
<td>2500.</td>
<td>.269</td>
<td>.009</td>
</tr>
<tr>
<td>700.</td>
<td>.334</td>
<td>.000</td>
<td>2600.</td>
<td>.339</td>
<td>.008</td>
</tr>
<tr>
<td>800.</td>
<td>.286</td>
<td>.002</td>
<td>2700.</td>
<td>.418</td>
<td>.006</td>
</tr>
<tr>
<td>900.</td>
<td>.238</td>
<td>.003</td>
<td>2800.</td>
<td>.505</td>
<td>.004</td>
</tr>
<tr>
<td>1000.</td>
<td>.192</td>
<td>.005</td>
<td>2900.</td>
<td>.600</td>
<td>.002</td>
</tr>
<tr>
<td>1100.</td>
<td>.151</td>
<td>.006</td>
<td>3000.</td>
<td>.701</td>
<td>-.000</td>
</tr>
<tr>
<td>1200.</td>
<td>.113</td>
<td>.008</td>
<td>3100.</td>
<td>.807</td>
<td>-.003</td>
</tr>
<tr>
<td>1300.</td>
<td>.082</td>
<td>.009</td>
<td>3200.</td>
<td>.915</td>
<td>-.006</td>
</tr>
<tr>
<td>1400.</td>
<td>.056</td>
<td>.009</td>
<td>3300.</td>
<td>1.022</td>
<td>-.009</td>
</tr>
<tr>
<td>1500.</td>
<td>.037</td>
<td>.010</td>
<td>3400.</td>
<td>1.126</td>
<td>-.013</td>
</tr>
<tr>
<td>1600.</td>
<td>.025</td>
<td>.011</td>
<td>3500.</td>
<td>1.222</td>
<td>-.016</td>
</tr>
<tr>
<td>1700.</td>
<td>.021</td>
<td>.011</td>
<td>3600.</td>
<td>1.307</td>
<td>-.019</td>
</tr>
<tr>
<td>1800.</td>
<td>.023</td>
<td>.011</td>
<td>3700.</td>
<td>1.378</td>
<td>-.021</td>
</tr>
<tr>
<td>1900.</td>
<td>.034</td>
<td>.011</td>
<td>3800.</td>
<td>1.431</td>
<td>-.023</td>
</tr>
</tbody>
</table>

This table is displayed only with the SICOFI control file variable \( R_{DISP} = Y \).

Reminder of the reference frequency

Ideal value of GR starting from the desired value of \( R_{LR} \)

From obtained value of \( R_{LR} \) quantized value of GR

Hexadecimal code of the optimized coefficient of GR

All attenuation values (in dB) refer to \( F_{REF} = 1014 \) Hz

First byte for Gain \( GR = 30 \) : \( 31,33 \)
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to $F_{REF} = 1014.0\,\text{Hz}$

$TG_{ref\,CA} = .235\,\text{ms}$  
$TG_{ref\,CB} = .218\,\text{ms}$

Group delay in transmit direction (D/A) for the voice channel A and B resp. at the reference frequency $F_{REF}$.

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>.059</td>
<td>.011</td>
<td>2000.</td>
<td>.047</td>
<td>.041</td>
</tr>
<tr>
<td>200.</td>
<td>.056</td>
<td>.001</td>
<td>2100.</td>
<td>.050</td>
<td>.048</td>
</tr>
<tr>
<td>300.</td>
<td>.050</td>
<td>.000</td>
<td>2200.</td>
<td>.052</td>
<td>.055</td>
</tr>
<tr>
<td>400.</td>
<td>.042</td>
<td>.000</td>
<td>2300.</td>
<td>.053</td>
<td>.062</td>
</tr>
<tr>
<td>500.</td>
<td>.034</td>
<td>.001</td>
<td>2400.</td>
<td>.053</td>
<td>.071</td>
</tr>
<tr>
<td>600.</td>
<td>.025</td>
<td>.002</td>
<td>2500.</td>
<td>.054</td>
<td>.081</td>
</tr>
<tr>
<td>700.</td>
<td>.017</td>
<td>.004</td>
<td>2600.</td>
<td>.055</td>
<td>.092</td>
</tr>
<tr>
<td>800.</td>
<td>.010</td>
<td>.005</td>
<td>2700.</td>
<td>.058</td>
<td>.106</td>
</tr>
<tr>
<td>900.</td>
<td>.006</td>
<td>.007</td>
<td>2800.</td>
<td>.063</td>
<td>.121</td>
</tr>
<tr>
<td>1000.</td>
<td>.003</td>
<td>.009</td>
<td>2900.</td>
<td>.071</td>
<td>.139</td>
</tr>
<tr>
<td>1100.</td>
<td>.003</td>
<td>.011</td>
<td>3000.</td>
<td>.084</td>
<td>.161</td>
</tr>
<tr>
<td>1200.</td>
<td>.005</td>
<td>.013</td>
<td>3100.</td>
<td>.105</td>
<td>.188</td>
</tr>
<tr>
<td>1300.</td>
<td>.008</td>
<td>.015</td>
<td>3200.</td>
<td>.136</td>
<td>.221</td>
</tr>
<tr>
<td>1400.</td>
<td>.013</td>
<td>.018</td>
<td>3300.</td>
<td>.185</td>
<td>.264</td>
</tr>
<tr>
<td>1500.</td>
<td>.019</td>
<td>.021</td>
<td>3400.</td>
<td>.267</td>
<td>.321</td>
</tr>
<tr>
<td>1600.</td>
<td>.026</td>
<td>.024</td>
<td>3500.</td>
<td>.408</td>
<td>.401</td>
</tr>
<tr>
<td>1700.</td>
<td>.033</td>
<td>.028</td>
<td>3600.</td>
<td>.671</td>
<td>.522</td>
</tr>
<tr>
<td>1800.</td>
<td>.038</td>
<td>.032</td>
<td>3700.</td>
<td>1.231</td>
<td>.718</td>
</tr>
<tr>
<td>1900.</td>
<td>.043</td>
<td>.036</td>
<td>3800.</td>
<td>2.640</td>
<td>1.056</td>
</tr>
</tbody>
</table>

Frequency response in transmit direction (D/A) of the set SICOFI+SLIC+external circuitry.
These are the theoretical values expected to be measured when SICOFI is programmed with the quantized values of the optimized coefficients of R filter.
Run # 1
B-FILTER calculation results

Reference impedance for optimization:
ZLRP1 = 820. ZLCP1 = 0.000 ZLRP2 = 0. ZLCP2 = 0.115E-06
ZLRS = 220. ZLCS = 0.000

Calculated and quantized coefficients:

\[
\begin{align*}
\text{XB} & = -0.11222 -0.35881 0.08265 0.19353 -0.06063 \\
\text{XBQ} & = -0.11133 -0.35938 0.08203 0.19531 -0.06061 \\
\text{XB} & = -0.08008 0.06006 0.01549 0.01419 \\
\end{align*}
\]

Options and values:

- Optimized coefficients of B filter
- Quantized values of the optimized coefficients of B filter
- Hexadecimal codes of the second part of the optimized coefficients of B filter
- Hexadecimal codes of the first part of the optimized coefficients of B filter
- Hexadecimal code of the COP-command used to program the second part of B filter
- Hexadecimal code of the COP-command used to program the first part of B filter

Theoretical transhybrid loss expected to be measured when SICOFI is programmed with the quantized values of the optimized coefficients of B filter.

Note: Theoretical values of the transhybrid loss greater than 40 dB are only calculated but may not be measurable exactly!

Value of the delay of B filter

Hexadecimal code of the B-delay filter coefficients

Hexadecimal code of the COP-command used to program the B-delay filter
5 Using the Software Packet

Note: To aid comprehensibility the following symbol < > has been introduced.
Any text enclosed within this symbol has to be typed from the PC keyboard.

5.1 Installation of SICOFI® Software

The SICOFI program STS 2060 requires the following environment:
- an IBM-AT Personal Computer or compatible running MS-DOS Version 3.0 or later
- a coprocessor 80287
- 640 Kbyte RAM available memory
- 1.2 Mbyte floppy disk drive
  (on request the program can be provided for a 360 Kbyte floppy disk drive)

Note: CONFIG.SYS file has to include:
  SET BUFFERS = 20
  SET FILES = 20
  DEVICE = ANSI.SYS
Various files and buffers are opened by the program. The program automatically closes
them with the command EXIT.

Having assembled all the necessary material you can start working with the program:

Insert the SICOFI disk in drive A.

Change to drive A: <a:>

Call the installation program: <setup>

The program SETUP creates the directories C:\SICOFI and C:\SICOFI\DOC on drive C (hard
disk).

The tables on the next page show which files will be copied by the program SETUP into each
directory.

Warning: The program SETUP will overwrite any existing files.
<table>
<thead>
<tr>
<th>Directory of C:\SICOFI</th>
<th>File contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>SICOFI.BAT</td>
<td>running batch file using SICO.EXE</td>
</tr>
<tr>
<td>SICO.EXE</td>
<td>SICOFI execution program</td>
</tr>
<tr>
<td>HARRIS.FOR</td>
<td>source file of HARRIS SLIC program written in FORTRAN</td>
</tr>
<tr>
<td>HARRIS.EXE</td>
<td>SLIC execution program of HARRIS SLIC</td>
</tr>
<tr>
<td>HARRIS.INP</td>
<td>input file of HARRIS.EXE</td>
</tr>
<tr>
<td>HARRIS.SLI</td>
<td>output file of HARRIS.EXE</td>
</tr>
<tr>
<td>HARRIS.CTL</td>
<td>control file of SICOFI program when calculating coefficients for SICOFI-HARRIS SLIC applications</td>
</tr>
<tr>
<td>HARRIS.RES</td>
<td>result file of SICOFI coefficients calculation for HARRIS SLIC</td>
</tr>
<tr>
<td>TRAFOS.FOR</td>
<td>source files of transformer SLIC</td>
</tr>
<tr>
<td>TRAFOT.FOR</td>
<td>programs with series or transverse feeding written in FORTRAN</td>
</tr>
<tr>
<td>TRAFOS.EXE</td>
<td>SLIC execution programs of transformer</td>
</tr>
<tr>
<td>TRAFOT.EXE</td>
<td>SLIC of the SICOFI User Board STU 2060</td>
</tr>
<tr>
<td>TRAFOS.INP</td>
<td>input file of TRAFOS.EXE</td>
</tr>
<tr>
<td>TRAFOT.INP</td>
<td>input file of TRAFOT.EXE with series or transverse feeding</td>
</tr>
<tr>
<td>TRAFOT.SLI</td>
<td>output file of transformer SLIC program</td>
</tr>
<tr>
<td>TRAFO.CTL</td>
<td>control file of SICOFI program when calculating coefficients for SICOFI-transformer SLIC applications</td>
</tr>
<tr>
<td>BRD.SPE</td>
<td>specification file for Germany</td>
</tr>
<tr>
<td>REF.BYT</td>
<td>reference byte file (USER.BYT)</td>
</tr>
<tr>
<td>BRD1.SPE</td>
<td>modified specification file for Germany</td>
</tr>
<tr>
<td>BRD1.IMP</td>
<td>impedance file</td>
</tr>
<tr>
<td>SICOAUTO.BAT</td>
<td>SICOFI BATCH program</td>
</tr>
<tr>
<td>MODE.CTL</td>
<td>SICOFI BATCH MODE file</td>
</tr>
<tr>
<td>BATCH.CTL</td>
<td>SICOFI BATCH CONTROL file</td>
</tr>
<tr>
<td>MARK.COM</td>
<td>mark current memory position</td>
</tr>
<tr>
<td>RELEASE.COM</td>
<td>release memory above last mark</td>
</tr>
<tr>
<td>RS232.EXE</td>
<td>RS232 Interface Program</td>
</tr>
</tbody>
</table>
The following SLIC programs are also available on request:

SGS.EXE  execution program of SGS-THOMSON SLIC L3030 + L3000
NSGS.EXE  execution program of SGS-THOMSON SLIC L3090 + L3000
ERIC.EXE  execution program of ERICSSON SLIC PBL 3762

A READ.ME file is available on the floppy disk.

To modify the SLIC part of the program, the following is necessary:
- an editor
- a compiler (e.g. MICROSOFT FORTRAN COMPILER advised, IBM professional FORTRAN compiler PROFORT, RMFORT ... )

  Note: our SLIC programs have been compiled using MICROSOFT compiler
- a linker (e.g. MICROSOFT, PROFORT, PLINK86 ... )

To start the program, type: <SICOFI>
5.2 STS 2060 Main Menu

Enter your selection:

1. SLIC Calculation
2. SICOFI Program
3. RS 232 SICOFI Programming
4. EXIT

<1>: you calculate the model of your SLIC (see chapter 5.3).
<2>: you start the SICOFI program (see chapter 5.5).
<3>: you initialize the RS 232 interface in order to program the SICOFI Test Board from your PC (see chapter 5.4).
<0>: you leave the STS 2060 software packet to return to MS-DOS.
5.3 STS 2060 SLIC Menu

<table>
<thead>
<tr>
<th>Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HARRIS SLIC HC 5502 / 5504</td>
</tr>
<tr>
<td>2</td>
<td>Transformer SLIC with Series Feeding</td>
</tr>
<tr>
<td>3</td>
<td>Transformer SLIC with Transverse Feeding</td>
</tr>
<tr>
<td>4</td>
<td>SGS - Thomson SLIC L3030 / L3000</td>
</tr>
<tr>
<td>5</td>
<td>SGS - Thomson SLIC L3090 / L3000</td>
</tr>
<tr>
<td>6</td>
<td>ERICSSON SLIC PBL 3736 / AMD 7950</td>
</tr>
<tr>
<td>7</td>
<td>ERICSSON SLIC PBL 3762</td>
</tr>
<tr>
<td>8</td>
<td>USER SLIC</td>
</tr>
<tr>
<td>0</td>
<td>EXIT To Main Menu</td>
</tr>
</tbody>
</table>

Enter your selection:

<1>, ... or <7>: the model of the indicated SLIC will be calculated and the corresponding M-parameters will be generated and written in a file (named by yourself) "***.SLI".

<8>: you have written your own SLIC routine. This routine has to be named "USER.EXE". This routine has to generate the M-parameters or K-parameters and to write them to a file named "***.SLI".

<0>: you return to the STS 2060 main menu.
5.4 STS 2060 RS 232 Menu

The program RS 232 uses the ***.BYT file to program the SICOFI Test Board STUT 2060.

This Test Board has to be connected to the PORT COM1.

The contents of the ***.BYT file is sent through the PORT COM1 via the interface RS 232 to the Test Board (see chapter 4.4 Byte file: US-ER.BYT).

<table>
<thead>
<tr>
<th>RS 232 Program V 1.0</th>
<th>Siemens HL IT PD 22</th>
</tr>
</thead>
<tbody>
<tr>
<td>9600 Baud, 8 bit, no Parity Bit and one Stop Bit at Port COM1</td>
<td>(1) File Definition (2) File Programming (3) Terminal Programming (0) END RS232 Programming</td>
</tr>
</tbody>
</table>

INPUT: 1

Please enter input file name: REF.BYT

⇒ Programming input file: REF.BYT

Enter your selection:

<1>: you declare which ***.BYT file you want to use to program the SICOFI Test Board.

<2>: the ***.BYT file has already been declared. The programming of the SICOFI Test Board can start immediately.

<3>: The SICOFI Test Board is programmed directly from the PC keyboard (without using any ***.BYT file).

<0>: you return to STS 2060 main menu.

Note: If you have used the command <3>, the command <Q> will bring you back to the above menu.
5.5 Using SICOFl® Program

Before starting the SICOFl program you must check:

- at least one control file "***.CTL" exists in the working directory.
- the specification file "***.SPE" and the SLIC transfer file "***.SLI" respectively declared by the control file variables SPEC and SLIC exist in the working directory.

Siemens AG., Components Group, HL IT PD 22
Authors: Mr. Kliese, Mr. Glasser Tel.: 089/4144-3662

Enter control file name: <***.ctl>
Reading SICOFl control file ... ***.CTL
Reading SLIC parameter file ... ***.SLI
Reading specification file ... ***.SPE
1 Disp 2 DATA 3 Opt 4 Sim 5 Byt 6 Res 7 Echo 8 Help 9 DOS 0 EXIT
5.6  STS 2060 SICOFI® Menu

At this point different commands are accessible. These commands can be chosen by typing the number or moving the cursor up to the desired command.

<1> or DISP:
Using this command you can display the current control file on the PC screen.
If you change the value of a variable (command DATA), this will be taken into account by the next display.
To display other files of the working directory, refer to the command DOS.

<2> or DATA:
Using this command you can change the value of a variable. How to proceed?
Type: <variable name><separator><new value><RETURN>
The possible separators are: < > <,> < = > <*> <%= > <$><%>
Several variables may be changed at the same time.
If the value of a variable corresponding to a file name (e.g. SPEC) is changed, not only the change will be taken into account but also the contents of the file will be automatically read and available for the SICOFI program.
To facilitate the declaration of the particular values of a variable the program offers the possibility to abbreviate the power of ten factor using the following conventions:

P  corresponds to pico  (1.0 E - 12)
N  corresponds to nano  (1.0 E - 09)
U  corresponds to micro (1.0 E - 06)
M  corresponds to milli  (1.0 E - 03)
K  corresponds to kilo  (1.0 E + 03)
MEG corresponds to mega  (1.0 E + 06)
G  corresponds to giga  (1.0 E + 09)

e.g.  OPT = X + R
      SIM = ALL
      ZAUTO = Y
      FX = 300,3.2k
<3> or OPT:

Using this command the program will optimize, automatically or not (see variables ZAUTO and BAUTO), the coefficients of the filters indicated by the variable OPT.

**Note:** The coefficient of the GR filter is automatically calculated together with those of the R filter.  
The coefficient of the GX filter is automatically calculated together with those of the X filter.  
The coefficient of the B-delay filter is automatically calculated together with those of the B filter.

Once obtained each coefficient is quantized to the closest value programmable at the SICOFI.  
Assuming the SICOFI is now programmed with the quantized coefficients, the program calculates the theoretical transfer functions of the set SICOFI-SLIC (taking into account which filters are switched on and which are switched off; see variables ON/OFF).

The table below shows which transfer function is calculated after which coefficient optimization:

<table>
<thead>
<tr>
<th>optimized coefficients</th>
<th>calculated transfer functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z filter</td>
<td>Return loss</td>
</tr>
<tr>
<td>R filter</td>
<td>Transfer function in receive direction (4-wire to 2-wire).</td>
</tr>
<tr>
<td></td>
<td>R filter absolute frequency response (if RDISP = Y)</td>
</tr>
<tr>
<td>X filter</td>
<td>Transfer function in transmit direction (4-wire to 2-wire).</td>
</tr>
<tr>
<td></td>
<td>X filter absolute frequency response (if XDISP = Y)</td>
</tr>
<tr>
<td>B filter</td>
<td>Transhybrid loss</td>
</tr>
</tbody>
</table>
<4> or SIM:

Using this command the program will simulate the absolute or relative (see variable REL) transfer functions or the set SICOFI-SLIC indicated by the variable SIM. These transfer functions may be checked by measurements (taking into account which filter is switched on and which one is switched off; see variables ON/OFF).

The diagram and table below show the meaning of each transfer function that can be simulated:

![Diagram of transfer functions](image)

**Figure 11**

**Definition of Transfer Functions**

<table>
<thead>
<tr>
<th>Transfer Function</th>
<th>Equivalent Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZRE: return loss</td>
<td>at a,b (Z = ZIN)</td>
</tr>
<tr>
<td>ZIN: input impedance</td>
<td>at a,b</td>
</tr>
<tr>
<td>AD: analog to digital</td>
<td>a,b to e</td>
</tr>
<tr>
<td>DA: digital to analog</td>
<td>e to a,b</td>
</tr>
<tr>
<td>DD: digital to digital</td>
<td>e to e via a,b (Z = ZL)</td>
</tr>
<tr>
<td>ASI: analog to SICOFI input</td>
<td>a,b to c</td>
</tr>
<tr>
<td>ASO: analog to SICOFI output</td>
<td>a,b to d (Z-filter on)</td>
</tr>
<tr>
<td>DSI: digital to SICOFI analog input</td>
<td>e to c via a,b</td>
</tr>
<tr>
<td>DSO: digital to SICOFI analog output</td>
<td>(Z = ZL or Z = ZI)</td>
</tr>
<tr>
<td></td>
<td>e to d</td>
</tr>
</tbody>
</table>

When the variable REL of the control file is "N", the program calculates absolute attenuation values.

With the REL variable of the control file set "Y", the program displays relative values normalized to the frequency FREF.
<5> or BYT:
Using this command the program takes the file declared under the variable BYTE as reference file and interchanges the coefficients written in this file with those calculated by the SICOFI program. Using the command BYT the program asks for a new ***.BYT file name. This new file can then be used with the program RS 232 to program the SICOFI Test Board.

<6> or RES:
Using this command you can store the results of the last SICOFI coefficient calculation in a file which name may be defined by yourself. The result file is described in chapter 4.5. To have a complete documentation of the transfer functions and coefficients, all SICOFI filters should be switched on (OPT = ALL or OPT = Z + R + X + B) in the last calculation.

<7> or ECHO:
Using this command under the current directory a file is created in which everything appearing on the PC screen is stored. To close the echo file type ECHO once again. After a session you may print the echo file for documentation purposes.

<8> or HELP:
Using this command you may access the program documentation without leaving the SICOFI program.

<9> or DOS:
Using this command you can work with the DOS of your PC. All the usual DOS commands are available (DIR, RENAME, TYPE, ...). After having used this command you automatically return to the SICOFI menu.

<0> or EXIT:
Using this command you return to the STS 2060 main menu.
6 Example: How to Obtain SICOFI® Coefficients for a Special SLIC Application

6.1 Calculation of M-Parameters for HARRIS SLIC

The following chapter gives an example showing how to obtain the optimized SICOFI coefficients for an application using the HARRIS SLIC HC 5508. The specifications to be fulfilled are those of the "Deutsche Bundespost".

Figure 12 shows in the upper part a simplified block diagram of the HARRIS SLIC HC 5508 and in the lower part the architecture which is taken from the datasheet.

In figure 13 you see the connection of the HARRIS SLIC to the SICOFI. In the two blocks AX and AR with external interface components capacitors $C_{CX}$ and $C_{CR}$ decouple a DC offset. Because the SICOFI input impedance is very high (MΩ), we then also need the resistor $R_{IX}$ in transmit path to have a defined high pass and time constant. In our application we take $C_{CX} = C_{CK} = 1\ \mu F$, $R_{IX} = 100\ \text{kΩ}$ and $VOX = VOR = 1$.

To gain the transfer function of the SLIC and its external interface components, it is necessary first to derive the M-Parameter as described in chapter 3.1.

The user then has to write a SLIC program which calculates the M-Parameters. With his SLIC program he generates a M-Parameter table of the SLIC like the table in chapter 3.3. The name of the M-Parameter output file may be HARRIS1.SLI and is used for an input file to the SICOFI coefficients program.

Next a SICOFI control file like HARRIS.CTL, which is listed on chapter 4.2.1, has to be edited. You have to update the "SLIC = HARRIS.SLI" to "SLIC = HARRIS1.SLI".

Now you may calculate the SICOFI coefficients as described in chapter 6.2.

The results are stored in a result file HARRIS1.RES which is described in chapter 4.5.
a) Derivation of the equations of the M-parameters:
In the following equations, AX and AR are the transfer function factors of the two blocks. With the factor K = 1000 we get:

\[ I_1 = \frac{(V_1 - V_0)}{(2 \times R_F)} \]  
(1)

\[ V_0 = -V_m + \frac{V_m \times K \times Z_0}{K \times 2 \times R_F} - 2 \times AR \times V_3 \]  
(2)

\[ V_0 = -(V_1 - V_0) + \frac{(V_1 - V_0) \times K \times Z_0}{K \times 2 \times R_F} - 2 \times AR \times V_3 \]  
(3)

\[ \frac{(V_1 - V_0) \times K \times Z_0}{K \times 2 \times R_F} = \frac{(V_1 - V_0) \times Z_0}{2 \times R_F} = V_1 + 2 \times AR \times V_3 \]  
(4)

with (1) and (4)

\[ I_1 \times Z_0 = V_1 + 2 \times AR + V_3 \]  
(5)

\[ V_2 = -AX \times (V_1 - V_0) + \frac{K \times Z_0}{K \times 2 \times R_F} = -AX \times (V_1 - V_0) + \frac{Z_0}{2 \times R_F} \]  
(6)

Conclusions:

\[ M11 = \frac{I_1}{V_1} = \frac{1}{Z_0} \quad \text{with } V_3 = 0 \]  
(7)

\[ M12 = \frac{I_1}{V_3} = \frac{2 \times AR}{Z_0} \quad \text{with } V_1 = 0 \]  
(8)

with \( V_3 = 0 \) and (5)

\[ V_1 = I_1 \times Z_0 \]  
(9)

\[ M21 = \frac{V_2}{V_1} = -AX \times (V_1 - V_0) \frac{1}{2 \times R_F \times I_1} = -AX \]  
(10)

with (6), (9) and (1)

\[ V_3 = \frac{(V_1 - V_0) \times Z_0}{2 \times AR \times 2 \times R_F} \quad \text{with (4)} \]  
(11)

\[ M22 = \frac{V_2}{V_3} = -2 \times AX \times AR \times \text{with } V_1 = 0 \text{ and (6), (11)} \]  
(12)
Figure 12
Internal Architecture of HARRIS SLIC HC 5508/09
Figure 13
Connection of HARRIS SLIC HC 5508/09 with SICOFI®
6.2 Working Method for Calculating SICOFI® Coefficients

The aim of this chapter is to give you some hints to take advantage of the flexibility of the STS 2060 software.

- The SICOFI is a CODEC filter which enables you to have only a single SLIC circuit for different application purposes (e.g. different countries).

The SLIC circuit has to be optimized first in order to use the SICOFI filters in their optimum working range (optimum use of the filters). For this aim you start in calculating the Z filter coefficients for the different applications. Modify the values of the different SLIC parameters in order to obtain the best compromise.

Then the SLIC parameters are frozen and, using the automatic calculation of the Z filter (ZAUTO = Y), the Z filter coefficients are optimized.

Subsequently the R (GR) and/or X (GX) filter coefficients are optimized.

Only then the B filter coefficients may be optimized in the automatic mode (BAUTO = Y).

Due to the architecture of the SICOFI, the filter coefficients have to be calculated in the sequence described above.

- Several specification files can be prepared before using the program in order to proceed more quickly during the calculation of the coefficients for different applications. Indeed only the file name declared with the variable SPEC needs to be changed to restart the calculation without leaving the SICOFI program.
7 Extended SICOFI® Calculation Features

7.1 Special Variables in the Control File

The values of these variables in general do not need to be changed during the optimization of the coefficients. They can be modified however to help you to advance in the optimization process if satisfactory results have not yet been achieved. If not adversely noted, variables may be changed during a session (command DATA).

ZMIR
Abbreviation meaning: Z-loop Mirror signal mask
Function: defines the mask of the Z-loop mirror signal. In calculating the Z filter coefficients the SICOFI program checks that the convolution effects due to the decimation and interpolation filters are really negligible as they should be.
Value: FR in Hz, AT- and AT+ in dB

RREFQ
Abbreviation meaning: RREF flag question
Function: indicates whether the R filter frequency response will be automatically optimized or calculated according to the value defined by RREF (see below).
Value: Y (according to RREF) or N (automatically).

RREF
Abbreviation meaning: R filter attenuation at REference Frequency
Function: indicates the value of the R filter attenuation at the reference frequency FREF when RREFQ = Y.
Value: in dB.

XREFQ
Abbreviation meaning: XREF flag question
Function: indicates whether the X filter frequency response will be automatically optimized or calculated according to the value defined by XREF (see below).
Value: Y (according to XREF) or N (automatically).
XREF
Abbreviation meaning: X filter attenuation at REference Frequency
Function: indicates the value of the X filter attenuation at the reference frequency FREF when XREFQ = Y.
Value: in dB.

ZLIM
Abbreviation meaning: Z filter coefficient LIMit
Function: indicates the limit of Z filter coefficient values during the automatic optimization (ZAUTO = Y).
Value: REAL value < 3.0.
Practical use: The variable ZLIM influences the precision of the quantization of the Z filter coefficients. By modifying the value of ZLIM you can decrease the quantization error.

ZLIM is the limit of the scale used to quantize the coefficients. The recommended value is 2. It can be set to a larger value in order to expand the scale but the actual coefficients should NOT be larger than 3.

ZSIGN
Abbreviation meaning: Z filter optimization SIGN
Function: indicates whether the automatic optimization of Z filter coefficients will be as far as possible from or as close as possible to the defined return loss specification ZRE.
Value: 1 (far) or –1 (close).
Practical use: Valid only when ZAUTO = Y.
BLIM
Abbreviation meaning: B filter coefficient LIMit
Function: indicates the limit of B filter coefficient values during the automatic optimization (BAUTO = Y).
Value: REAL value < 3.0.
Practical use: The explanation concerning the variable ZLIM applies to BLIM accordingly.

BSIGN
Abbreviation meaning: B filter optimization SIGN
Function: indicates whether the automatic optimization of B filter coefficients will be as far as possible from or as close as possible to the defined transhybrid loss specification DD.
Value: 1 (far) or –1 (close).
Practical use: Valid only when BAUTO = Y.

DPRE, DPOF, APOF, APRE:
When the SLIC has not been correctly modelled, the simulated frequency responses of the circuit SICOFI-SLIC may greatly differ from the measured ones.
The variables DPRE, DPOF, APOF, APRE introduce some fictive delays or attenuations respectively to allow the user to correct any failure in the SLIC model.
The optimum values of these variables are obtained experimentally; the influence of these variables however can be roughly described as follows:
Positive values of the variables DPRE and DPOF cause a deterioration of the frequency response in the high frequency band.

Positive values of the variables APRE and APOF cause a deterioration of the frequency response in the whole speech band (see diagram below).

This diagram is also valid for DPRE.

This diagram is also valid for APRE.
7.2 Special Variables in the Specification File

In the specification file some impedance like the input impedance $Z_I$, load impedance $Z_L$, terminating impedance $Z_3$ and the reference impedance $Z_R$ are defined. These impedances are described in terms of the equivalent circuit diagram shown in chapter 4.3.

In special cases like the British Telecom it is necessary to calculate more complex impedance schemes which cannot be described using our impedance library. Therefore we introduce the additional feature of reading a defined complex impedance table from a file.

If the equivalent circuit of the impedance $Z_I$, $Z_L$, or $Z_3$ is not defined in the specification file, the SICOFL program searches for the keywords 'ZI', 'ZL' or 'Z3' with an assignment of the name of an impedance file *.IMP.

If you want to use these complex impedances you may write a small program written in any programming language which calculates the impedance in the range of 10 Hz – 4000 Hz in steps of 10 Hz. A listing of the specification file BRD1.SPE using these special variables is given below.
### 7.2.1 Listing of the Specification File BRD1.SPE with Special Variables

FREF = 1014.0  LAW = A
VREF = 0.9480  RLX = 0.  RLR = -7.0
ABIMP = ZI
ZL = BRD1.IMP
ZI = BRD1.IMP
Z3 = BRD1.IMP

<table>
<thead>
<tr>
<th>ZRE</th>
<th>FR</th>
<th>AT-</th>
<th>AT+</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>300</td>
<td>20</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td>500</td>
<td>20</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ZMIR</th>
<th>FR</th>
<th>AT-</th>
<th>AT+</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4k</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>12k</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DA, UPPER</th>
<th>FR</th>
<th>AT-</th>
<th>AT+</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>300</td>
<td>100</td>
<td>.75</td>
</tr>
<tr>
<td></td>
<td>500</td>
<td>.75</td>
<td>.25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>.75</td>
<td>.35</td>
</tr>
<tr>
<td></td>
<td></td>
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<td>.75</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
</tr>
</tbody>
</table>

<table>
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<tr>
<th>DA, LOWER</th>
<th>FR</th>
<th>AT-</th>
<th>AT+</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>300</td>
<td>0</td>
<td>-.25</td>
</tr>
<tr>
<td></td>
<td>3.4k</td>
<td></td>
<td></td>
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<th>FR</th>
<th>AT-</th>
<th>AT+</th>
</tr>
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<tr>
<td></td>
<td>500</td>
<td>100</td>
<td>.75</td>
</tr>
<tr>
<td></td>
<td>600</td>
<td>.75</td>
<td>.25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>.75</td>
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<tr>
<td></td>
<td></td>
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<td>.75</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AD, UPPER</th>
<th>FR</th>
<th>AT-</th>
<th>AT+</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>300</td>
<td>100</td>
<td>.75</td>
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<tr>
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<td>500</td>
<td>.75</td>
<td>.25</td>
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<td>.75</td>
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<td></td>
<td></td>
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<tr>
<th>AD, LOWER</th>
<th>FR</th>
<th>AT-</th>
<th>AT+</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>300</td>
<td>0</td>
<td>-.25</td>
</tr>
<tr>
<td></td>
<td>3.4k</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AD, DELAY</th>
<th>FR</th>
<th>AT-</th>
<th>AT+</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>500</td>
<td>100</td>
<td>.75</td>
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<td>.35</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>.75</td>
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<tr>
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<td></td>
<td></td>
<td>100</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>DD</th>
<th>FR</th>
<th>AT-</th>
<th>AT+</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>300</td>
<td>27</td>
<td>23</td>
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<tr>
<td></td>
<td>500</td>
<td>27</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>2.5k</td>
<td>27</td>
<td></td>
</tr>
</tbody>
</table>
7.2.2 Format of the Impedance File *.IMP

This file contains an impedance table, which is defined in the actual specification file and may be read by the SICOFI coefficients program.

The impedance file has the following standard form:

1. "*" at the first position of a line means a comment that the SICOFI program will not use for calculations. Such lines are only for documentation purposes.

2. The SICOFI program looks for the values of FREQUENCY, REAL PART and IMAGINARY PART of the calculated impedance.

* BRD.SPE : RP1 = 820, CP2 = 115E-09, RS = 220.
* FREQ     REAL       IMAG
  10.000000  1039.971000  -4.858366
  20.000000  1039.885000  -9.715708
  30.000000  1039.741000 -14.571000

........  ..........  ..........

........  ..........  ..........

  990.000000  830.084800 -357.863200
 1000.000000  826.930200 -359.608800
 1010.000000  823.776800 -361.317800
 1020.000000  820.625100 -362.990500

........  ..........  ..........

........  ..........  ..........

 3980.000000  344.981800 -294.728100
 3990.000000  344.451100 -294.213900
 4000.000000  343.923500 -293.701000
7.3 K-Parameters

It has been found that from mathematical reasons the M-parameters cannot always be used to model a SLIC. That happens with the Ericsson SLIC. Furthermore the M-parameters are not easy to be measured. Therefore we developed the K-parameters.

Each K-parameter is expressed in the SLIC program as an algebraic equation, combination of the various SLIC parameters which are provided by the SLIC input file SLIC.INP.

According to the values of the SLIC input data the SLIC program calculates the values of the K-parameters in function of the frequency and writes them in an output file SLIC.SLI.

The values of each K-parameter for the frequencies between 10 Hz and 3990 Hz in steps of 10 Hz are written in a table similar to the M-parameters. The contents of these tables are used by the SICOFI program instead of the M-Parameter tables. The format of the K-Parameter Tables is shown on chapter 7.3.2.

Proceeding in a similar manner as for obtaining the theoretical equation of the M-parameters, we get the K-parameters.

Figure 14 shows a SLIC with a symmetrical generator \( V_g \) and a symmetrical line impedance \( Z_g \). The SLIC can be considered as a circuit accessible through three ports.

![Figure 14](image)

Three equations are sufficient to describe the SLIC completely and any linear combination of these variables is possible:

Let us take the following combination:

1. \( a_1 = V_1 + Z_g \times I_1 \)
2. \( b_1 = V_1 - Z_g \times I_1 \)
Then using these new variables, the model of the SLIC becomes:

![Diagram](image.png)

**Figure 15**
Three-Port Model with the Variables a1 and b1

Following equations can now be written:

1. \( b_1 = K_{11} \times a_1 + K_{12} \times V_3 + K_{13} \times I_2 \)
2. \( V_2 = K_{21} \times a_1 + K_{22} \times V_3 + K_{23} \times I_2 \)
3. \( I_3 = K_{31} \times a_1 + K_{32} \times V_3 + K_{33} \times I_2 \)

When the SLIC is connected to the SICOFI, we can assume that:

- \( I_2 = 0 \) because the input impedance of SICOFI can be included in the model
- \( I_3 \) is not relevant in the following calculations because the SICOFI works as an ideal voltage generator. (In special cases the SICOFI output impedance of about 10 \( \Omega \) may be included in the SLIC model.)

Accordingly the equations system can be simplified as follows:

1. \( b_1 = K_{11} \times a_1 + K_{12} \times V_3 \)
2. \( V_2 = K_{21} \times a_1 + K_{22} \times V_3 \)

a) Parameter \( K_{11} \):

Equation (6) gives \( K_{11} = b_1/a_1 \) when \( V_3 = 0 \)

From (1) and (2) we can deduce:

\[
\frac{b_1}{a_1} = \frac{(V_1 - Z_g \times I_1)}{(V_1 + Z_g \times I_1)} = \frac{(V_1/I_1 - Z_g)}{(V_1/I_1 + Z_g)}
\]

Let us call \( Z_n \) the input impedance of the SLIC:

\( Z_n = \frac{V_1}{I_1} \)

Therefrom:

\[
K_{11} = \frac{(Z_n - Z_g)}{(Z_n + Z_g)} \quad \text{for} \quad V_3 = 0
\]
b) Parameter K12:
K12 = b1/V3 when a1 = 0
From (1) follows:  
\[ V_1 + Z_g \times I_1 = 0 \]
i.e.  
\[ V_1 = -Z_g \times I_1 \]
Thus  
\[ b1 = V_1 - Z_g \times I_1 = V_1 + V_1 \]
Then
\[ K12 = 2 \times \frac{V_1}{V_2} \text{ for } V_1 = -Z_g \times I_1 \]

![Figure 16](image)

**K12 Definition**

c) Parameter K21:
K21 = Vg/a1 when V3 = 0
In this case:  
\[ a1 = V_1 + Z_g \times I_1 = V_g \]
Then
\[ K21 = \frac{V_2}{V_g} \text{ for } V_3 = 0 \]

The equivalent circuit is the following:

![Figure 17](image)

**K21 Definition**
d) Parameter K22:

![K22 Diagram]

**Figure 18**
K22 Equivalent Circuit

From (1) and $a_1 = 0$ follows: $V_1 = -Z_g \times I_1$

From (7) and $a_1 = 0$:

$$K22 = \frac{V_2}{V_3}$$

for $V_1 = -Z_g \times I_1$

**Note:**
1. All these parameters are accessible by measurement with a symmetrical ground-free generator and a complex voltmeter.
2. $R_L = -20 \times \log_{10} (|K11|)$ is nothing else than the return loss of the SLIC without SICOFl.

**Warning:** The K-parameters depend on the impedance $Z_g$ and has to be recalculated for every new line impedance.
7.3.1 Format of the K-Parameter Table

This file represents the interface between SICOFI program and SLIC program with K parameters.

It has the following standard form:

Note:
1. "*" at the first position of a line means a comment that the SICOFI program will not use for calculations. Such lines are only for documentation purposes.

2. The SICOFI program looks for the keywords 'ZSLI', 'K11-TABLE', 'K12-TABLE', 'K21-TABLE' and 'K22-TABLE' which have to be at first position without '*' and are followed by the values of FREQUENCY, REAL PART and IMAGINARY PART of the actual parameter.

```
* TRAFO SLIC
* PARAMETER : K
*ZgR1 = 820.0 *ZgC1 = .0000 *ZgR2 = .0000 *ZgC2 = .1150E-06
*ZgRS = 220.0 *ZgCS = .0000
*Z0R1 = 700.0 *Z0C1 = .0000 *Z0R2 = .0000 *Z0C2 = .1000E-06
*Z0RS = .0000 *Z0CS = .0000
*ERZN = 0  *EXZN = 0
*RCU1 = 84.0  *RCU2 = 105.0  *CW1 = .1135E-09  *CW2 = .1354E-09
*L1 = 1.150  *L2 = 1.150  *M = 1.148
*CSP = .1000E-05 *
*RV = 792.0  *LV = 2.230  *CV = .2670E-08
ZSLI worst case half loop value
.5000
<table>
<thead>
<tr>
<th>FREQUENCY</th>
<th>REAL</th>
<th>IMAG</th>
</tr>
</thead>
<tbody>
<tr>
<td>K11-TABLE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10.000000</td>
<td>-1.246919E-01</td>
<td>6.369420E-02</td>
</tr>
<tr>
<td>20.000000</td>
<td>-9.300768E-02</td>
<td>1.216179E-01</td>
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<tr>
<td>................</td>
<td>................</td>
<td>................</td>
</tr>
<tr>
<td>3980.000000</td>
<td>-2.405917E-02</td>
<td>5.318151E-02</td>
</tr>
<tr>
<td>3990.000000</td>
<td>-2.436709E-02</td>
<td>5.337689E-02</td>
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<tr>
<td>K12-TABLE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10.000000</td>
<td>-5.142274E-03</td>
<td>1.191222E-04</td>
</tr>
<tr>
<td>20.000000</td>
<td>-2.146059E-02</td>
<td>1.294169E-03</td>
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<tr>
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<td>................</td>
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<tr>
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<td>1.018615</td>
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</tr>
<tr>
<td>3990.000000</td>
<td>1.018857</td>
<td>-6.285563E-02</td>
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<tr>
<td>K21-TABLE</td>
<td></td>
<td></td>
</tr>
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<td>-1.730312E-03</td>
<td>4.013790E-05</td>
</tr>
<tr>
<td>20.000000</td>
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<td>4.315760E-04</td>
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<td>................</td>
<td>................</td>
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<td>3.587218E-01</td>
<td>-1.542590E-01</td>
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<tr>
<td>3990.000000</td>
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<td>-1.547763E-01</td>
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<tr>
<td>K22-TABLE</td>
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<td></td>
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<td>10.000000</td>
<td>1.372118E-01</td>
<td>7.832120E-02</td>
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<tr>
<td>20.000000</td>
<td>1.578308E-01</td>
<td>1.551793E-01</td>
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<td>................</td>
<td>................</td>
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<td>6.382880E-01</td>
<td>1.535947E-01</td>
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<tr>
<td>3990.000000</td>
<td>6.384676E-01</td>
<td>1.540913E-01</td>
</tr>
</tbody>
</table>
```
7.4 Running SICOFI® Calculation Program in BATCH Mode

You have the possibility to run the calculation part of the SICOFI coefficients program in a BATCH mode. Instead of typing the commands for the SICOFI program into the keyboard, you may store a sequence of commands in a file.

a) MODE.CTL file

In the directory C:\SICOFI there is a file called MODE.CTL.
In normal (default) working mode the MODE.CTL file contains:

\[
\text{BATCH} = \text{N}
\]

In this normal mode the program is waiting for keyboard inputs and you may either start a SLIC program or a calculation of SICOFI coefficients by using different menus.

Using the batch mode change \text{BATCH} = \text{N} in the MODE.CTL file to

\[
\text{BATCH} = \text{Y}
\]

b) BATCH.CTL file

In the BATCH.CTL file you may store a sequence of commands for the SICOFI calculation program. This file has to be in the current working directory.

All commands of the normal calculation mode are available (commands: 1 2 3 4 5 6 7 0) except the commands 8 for HELP and 9 for DOS.

With the BATCH.CTL file shown below the SICOFI program

a) determines the SICOFI coefficients for a HARRIS SLIC application in non-automatic Z and B filter calculation mode.

b) calculates the Z and B filter in an automatic calculation mode \(ZAUTO = \text{Y}, BAUTO = \text{Y}\).

c) stores the programming bytes in a file called TEST1.BYT.

c) makes a file result file called TEST1.RES.

d) starts a simulation of SICOFI-SLIC transfer functions

e) stores the results of the simulation in a file called TEST1.SIM.

f) makes a plot file called TEST1.PLT.

g) exits with the last command 0 of the BATCH.CTL file.
Listing of the BATCH.CTL File

HARRIS.CTL
1
3
2
ZAUTO = Y ZREP = Y BAUTO = Y BREP = Y
3
5
TEST1.BYT
6
TEST1.RES
2
SIM = ALL
1
4
6
TEST1.SIM
2
SIM = ALL PLQ = Y
6
TEST1.PLT
0

c) SICOAUTO.BAT
To start the SICOFI program in batch mode there has to be a batch file e.g. SICOAUTO.BAT in the current working directory. The contents of the SICOAUTO.BAT file may be:

IF EXIST TEST1.BYT DEL TEST1.BYT
IF EXIST TEST1.RES DEL TEST1.RES
IF EXIST TEST1.SIM DEL TEST1.SIM
IF EXIST TEST1.PLT DEL TEST1.PLT
MARK
SICO<BATCH.CTL
RELEASE

This batch file starts the program SICO.EXE and takes the commands from the file BATCH.CTL.

If you want to leave this batch mode for to work in the normal SICOFI program mode don’t forget to edit the MODE.CTL file in the directory C:SICOFI and change BATCH = Y to BATCH = N.

Note: If former output files like TEST1.BYT, TEST1.RES, TEST1.SIM or TEST1.PLT already exist, the SICOFI program asks if you want to overwrite them. To suppress this question you should delete those output files before starting the batch sequence.
8 Measurements and Specifications

8.1 Measurements for Verification of SICOFI®-SLIC Transfer Functions

In the simulation mode of the SICOFI coefficients program (command SIM) different transfer functions with SICOFI filters switched on or off can be calculated. On the following pages we propose solution schemes to some of these transfer function measurements e.g:

- Input impedance
- Analog to digital path
- Digital to analog path
- Digital to digital path
- Digital to SICOFI analog output path

We use the PCM4 from Wandel & Goltermann as measurement system.

It is further possible to verify following simulated transfer functions of the SICOFI-SLIC system:
- Digital to SICOFI input path via SLIC loop
- Analog to SICOFI input path
- Analog to SICOFI analog output path via Z-filter loop
- Transfer functions of the SLIC itself with SICOFI filters switched off. This allows to check if the calculated SLIC model is correct.
Figure 19
Measuring the Transfer Function Input Impedance

Measurement of return loss with generator impedance $Z_i$ on the a, b line. Optionally, various combination of SICOFI filters can be switched ON or OFF.

Figure 20
Measuring the Transfer Function Analog – Digital

Analog signal input using the PCM4 across the a, b lines. Generator impedance $Z_i/Z_3$ on the a, b line. Digital return signal measurement with the PCM4 on the PCM-highway. Optionally, various combinations of SICOFI filters can be switched ON or OFF.
**Figure 21**

**Measuring the Transfer Function Digital – Analog**

Digital signal input via the PCM-highway on the PBC. Analog signal measurement with the PCM4 across $Z_l/Z_3$ on the a, b line. Optionally, various combinations of SICOFI filters can be switched ON or OFF.

**Figure 22**

**Measuring the Transfer Function Digital – Digital**

Digital signal input via the PCM-highway on the PBC. Terminating impedance $Z_l$ on the a, b line. Return digital signal measurement with the PCM4 on the PCM-highway. Optionally, various combinations of SICOFI filters can be switched ON or OFF.
Measuring the Transfer Function Digital – SICOFI® Output

Digital signal input via the PCM-highway on the PBC. Return analog signal measurement with the PCM4 on the SICOFI output (use $R_X > 30 \, k\Omega$). Terminate the a, b line with impedance $Z_I/ Z_s$. Optionally, various combinations of SICOFI filters can be switched ON or OFF.
8.2 Extract of Analog Line Card Specifications Valid for the "Deutsche Bundespost"

SLMA specifications differ for each country. Here the peculiar specifications of the "Deutsche Bundespost" (FTZ 12 R4-3) are shown.

The following masks are drawn:

– Return loss
– Balance return loss
– Attenuation distortion in transmit direction (analog → digital)
– Attenuation distortion in receive direction (digital → analog)
Figure 24
Return Loss $a_R$

Figure 25
Balance Return Loss $a_F$
Figure 26
Attenuation Distortion in Transmit Direction
2-Wire Analog → Digital

Figure 27
Attenuation Distortion in Receive Direction
Digital → 2-Wire Analog
9  Appendix

9.1  New Features in SICOFI® Software Version 3.0

– program is faster and more user friendly
– easy to install SICOFI software on a PC with a separate SETUP program
– menu driven program surface
– access to different help files (Command HELP) for calculating SICOFI coefficients and SLIC transfer functions. The user can scroll the text contained in different help files.
– SLIC calculation may be started without leaving SICOFI program
– DOS commands are available from program level (Command DOS)
– possibility of starting other small programs (Command DOS)
– RS232 for programming of SICOFI testboard is provided
– extended simulation mode (input impedance, ...) 
– extra impedance input files covered for input impedance $Z_i$, terminating impedance $Z_3$ and load impedance $Z_L$
– SICOFI program may be run in batch mode
– new features of SICOFI version V 4.x available, like analog amplification AGX, digital amplification TM3 in transmit path and attenuation AGR in receive path

Changes with respect to SICOFI Software Version 2.0:

– Specification file *.SPE has been modified with respect to the definition of input impedance $Z_i$, load impedance $Z_L$, impedance $Z_3$, reference impedance $Z_R$, reference voltage $V_{REF}$ and return loss specification $Z_{IN}$.

<table>
<thead>
<tr>
<th>New Variable</th>
<th>Previous</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{REF}$</td>
<td>$V_{REF}$</td>
<td>Voltage REFerence of the 0 dB level</td>
</tr>
<tr>
<td>$Z_{RE}$</td>
<td>$Z_{IN}$</td>
<td>Z-filter REturnloss specification</td>
</tr>
<tr>
<td>$Z_{IRP1}$</td>
<td>$R_{PAR}$</td>
<td>Input impedance $Z_i$ was defined together with ERZI.</td>
</tr>
<tr>
<td>$Z_{IP1}$</td>
<td>- -</td>
<td></td>
</tr>
<tr>
<td>$Z_{IRP2}$</td>
<td>- -</td>
<td></td>
</tr>
<tr>
<td>$Z_{IP2}$</td>
<td>$C_{PAR}$</td>
<td></td>
</tr>
<tr>
<td>$Z_{IRS}$</td>
<td>$R_{SER}$</td>
<td></td>
</tr>
<tr>
<td>$Z_{ICS}$</td>
<td>$C_{SER}$</td>
<td></td>
</tr>
</tbody>
</table>

Same naming conventions for impedance $Z_i$, $Z_L$, $Z_3$ and $Z_R$. 
Variables in SICOFI control file *.CTL of STS 2060 version 3.0 have been modified:

<table>
<thead>
<tr>
<th>New Variable</th>
<th>Previous</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZAUTO</td>
<td>PZIN = 0</td>
<td>AUTOmatic calculation of Z filter</td>
</tr>
<tr>
<td>BAUTO</td>
<td>PB = 0</td>
<td>AUTOmatic calculation of B filter</td>
</tr>
<tr>
<td>FZP</td>
<td>FZ</td>
<td>Frequency points for Z filter calculation in non-auto-matic optimization mode</td>
</tr>
<tr>
<td>FBP</td>
<td>FB</td>
<td>Frequency points for B filter calculation in non-auto-matic optimization mode</td>
</tr>
<tr>
<td>XDISP</td>
<td>XFIL</td>
<td>X filter frequency response DISPlay</td>
</tr>
<tr>
<td>RDISP</td>
<td>RFIL</td>
<td>R filter frequency response DISPlay</td>
</tr>
<tr>
<td>BDF</td>
<td>TBM</td>
<td>B Delay Filter</td>
</tr>
<tr>
<td>AGX</td>
<td>- -</td>
<td>Analog Gain control transmit path</td>
</tr>
<tr>
<td>AGR</td>
<td>- -</td>
<td>Analog Gain control receive path</td>
</tr>
<tr>
<td>TM3</td>
<td>- -</td>
<td>Test Mode of SICOFI V 4.x: additional gain in transmit path</td>
</tr>
</tbody>
</table>

**Note:** Do not use specification files or SICOFI control files of SICOFI software version V2.0. The former versions of SLIC.INP together with SLIC.EXE, however, and earlier result files SLIC.SLI could still be used.

| 0.590       | 1.07031250 | 1 3 1 0 -1 3 -1 1 30 B9 |
| 0.527       | 1.06250000 | 1 2 1 0 -1 2 -1 0 20 A8 |
| 0.462       | 1.05468750 | 1 3 1 0 1 3 -1 1 30 39 |
| 0.398       | 1.04687500 | 1 3 1 0 1 2 -1 1 30 29 |
| 0.333       | 1.03906250 | 1 4 1 0 1 1 -1 2 40 1A |
| 0.267       | 1.03125000 | 1 3 1 0 1 1 -1 1 30 19 |
| 0.201       | 1.02343750 | 1 4 1 0 1 2 -1 1 40 29 |
| 0.135       | 1.01562500 | -1 3 1 0 1 3 -1 0 B0 38 |
| 0.068       | 1.00781250 | 1 3 1 0 -1 4 -1 0 30 C8 |
| 0.000       | 1.00000000 | 1 0 1 1 -1 0 1 0 01 80 |
### 9.2 Gain Tables for Programming Transmit GX

Table of gain values for programming transmit GX of SICOFI V3.x.

Values from +12 dB ... 0 dB

\[
A = \left[ (V_1 \cdot 2^{-K1} + 1) \cdot V_2 \cdot 2^{-K2} + 1 \right] \cdot V_3 \cdot 2^{-K3} + 1 \cdot V_4 \cdot 2^{-K4}
\]

<table>
<thead>
<tr>
<th>(dB)</th>
<th>A</th>
<th>v3, k3</th>
<th>v4, k4</th>
<th>v1, k1</th>
<th>v2, k2</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>12.041</td>
<td>4.00000000</td>
<td>1 0</td>
<td>1 0</td>
<td>1 0</td>
<td>1 0</td>
<td>00 00</td>
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<td>3.50000000</td>
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<td>1 0</td>
<td>1 1</td>
<td>1 0</td>
<td>00 10</td>
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<td>1 0</td>
<td>1 2</td>
<td>1 0</td>
<td>00 20</td>
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<td>1 0</td>
<td>1 3</td>
<td>1 0</td>
<td>00 30</td>
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<td>1 0</td>
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<td>1 0</td>
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<td>1 0</td>
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<td>1 0</td>
<td>00 E0</td>
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<td>(-1) 5</td>
<td>1 0</td>
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<td>00 90</td>
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<td>1 0</td>
<td>(-1) 0</td>
<td>1 1</td>
<td>00 A0</td>
</tr>
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<td>2.31250000</td>
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<td>1 0</td>
<td>(-1) 0</td>
<td>1 2</td>
<td>00 B0</td>
</tr>
<tr>
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<td>2.28125000</td>
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<td>1 0</td>
<td>(-1) 0</td>
<td>1 2</td>
<td>00 C0</td>
</tr>
<tr>
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<td>(-1) 0</td>
<td>1 2</td>
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<td>1 2</td>
<td>00 E0</td>
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Values from +18 db ... 0 dB

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\[ GX = A \quad \text{if TM3 = 000} \]
\[ GX = 2 \cdot A \quad \text{if TM3 = 001} \]
\[ GX = 4 \cdot A \quad \text{if TM3 = 011} \]

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### 9.3 Gain Tables for Programming Transmit GR

**Table of Attenuation Values for Programming Receive GR in SICOFI.**

Values from 0 dB ... -12 dB

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# Calculating SLIC Parameters

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Calculating SLIC Parameters of the Transformer SLIC Using M-Parameters and SPICE

Preface

A solution to the problem of modeling new SLICs is submitted by using a combination of an arbitrary SPICE program and of the Conversion Program SLIC.EXE'.

A detailed description of the Conversion Program is given, and its practical use is exemplified.

To read this application note with profits, the SICOFI Coefficients Program and generalities about the SLIC file format and the SPICE input files should be known.

1 Introduction

To calculate the parameters of a SLIC and to simulate its transfer characteristics (e.g. using the STS 2060 SICOFI coefficients program) it is necessary to write for each new type of SLIC a new program. This is not only a time consuming process, but also new errors introduced into the software model may easily lead to wrong results.

The simulation of analog circuits can also be done by using general programs like SPICE (we used the version of the firm MICROSIM: PSPICE); but there is a problem: The output provided by SPICE is not suited as input to the SICOFI coefficients program (unless the SPICE Program contains an "Analog Behavioral Modelling").

Therefore a Conversion Program was written in FORTRAN to convert and calculate the SLIC parameter file (.SLI file) to be used with the SICOFI program from the interpolated SPICE output.

Note: This Conversion Program can also be used to interpolate measured SLIC data when these data are in the form of a SPICE output file (see chapter 4.4).

Terminology:

SLIC: Subscriber Line Interface Circuit.
SICOFI: Signal processing Codec Filter (PEB2060).

In the following we will call "SLIC" the hardware and software corresponding to the analog components in a subscriber line interface circuit excluding the SICOFI chip.

Please note that the Conversion Program is also called SLIC.EXE.
2  SICOFI® Software Principle

The main functions of a Subscriber Line Interface Circuit (SLIC) are to provide the BORSHT functions (Battery feeding, Overvoltage protection, Ringing, Signaling, Hybrid function, Testing). In the case of a SLIC being used in combination with the SICOFI, the Hybrid function is split into the two-wire to four-wire conversion realized by the SLIC, and the impedance matching, hybrid balancing and gain adjustment provided by the internal filters of the SICOFI.

The other functions (such as off-hook detection, metering, stand-by mode, ringing) may also affect the speech signal, but we will not consider them in the SLIC example described below.

As has been told, the hardware can be split into two parts: The SLIC and its external circuitry on one side and the SICOFI on the other (see figure 1).

![Figure 1](image1)

**Figure 1**
**SLIC-SICOFI® Hardware**

In a similar way, the software consists of two major sections: The SLIC description file (.SLI file) and the SICOFI program.

![Figure 2](image2)

**Figure 2**
**SLIC-SICOFI® Software**
According to its functions, a SLIC is a rather complicated circuit (see figure 12). Analyzing the SLIC (e.g. for simulating its transfer characteristics) is facilitated in using e.g. PSPICE. Then the SPICE output file, which is not compatible to the SICOFI program, may be adapted by using the Conversion Program ‘SLIC.EXE’ (see figure 3).

**Figure 3**
Software Structure

In detail when using SPICE for modelling the SLIC, the complete SICOFI software structure is shown in the following figure 4:

**Figure 4**
Details of Software Structure
Calculating SLIC Parameters

SLIC2OP.LIB
All the specific values concerning the SLIC and its external circuitry (physical data, filter
dimensions, ...) are gathered in a SPICE input file SLIC2OP.LIB.
This file gets its non-standard subcircuits (like the transformer data) from the TRAFO.LIB and
e.g. the opamp from SPICE library files (LINEAR.LIB).

SLIC.LIB
The file SLIC.LIB provides the description of a particular SLIC circuit. The main advantage of
this procedure is, that the file SLIC.LIB acts like a kind of black box containing the actual SLIC:
While the black box and its connections remain unchanged, the SLIC circuitry inside the box
can easily be replaced by simply changing (the names of) the SLIC sub-circuit and it’s library
(‘SLIC2OP.LIB’).
In the following the various available library files and their use is reviewed.

TRAFO.LIB contains a description of an arbitrary transformer. The transformer components
have to be matched to the actual data.

SLIC.CIR contains the necessary test circuits to generate the SPICE output file.
This file must not be changed.

The SPICE program analyzes the test circuits and calculates voltages and currents from which
the M-parameters are deduced.

The SLIC program SLIC.EXE then converts the output of SPICE to a file SLIC.SLI which is
compatible to the SICOFI Coefficients Program and which contains the transmission
characteristics of the SLIC in the form of the M-parameters.

For easy use, the SPICE and the conversion programs are combined in a batch file S.BAT.
This batch file is run as follows:

S SLIC <ENTER> (Without the .OUT suffix)

SLIC.SLI is a transfer file (output/input file) between the SLIC program and the SICOFI
program to introduce the SLIC circuit data (M-parameters) into the SICOFI program.
Calculating SLIC Parameters

Auxiliary Files:

COUNTRY.SPE is an input file of the SICOFI program describing the customer specification (CCITT etc. ...) and measurement configuration parameters (e.g. termination impedance).

REF.BYT is an input file of the SICOFI program which defines a frame into which the program can write the newly calculated coefficients together with some predefined commands (required for sending the SICOFI coefficients from the Peripheral Board Controller PBC (PEB 2051) to the SICOFI) and stores them in a USER.BYT file.

SICOFI.CTL is the control file of the SICOFI program. It contains the data controlling the optimization and simulation processes.

The SICOFI program generates the SICOFI coefficients and simulates the theoretical transfer functions of the set SLIC + SICOFI.

RESULT.RES is the output file of the SICOFI program. It contains the coefficients for programming the SICOFI and a list of the calculated results corresponding to various measurements on the set SICOFI + SLIC. (e.g. return loss, frequency response, echo return loss, etc ...).
3 The Conversion Program SLIC.EXE

3.1 Features

- The Conversion Program is written in MICROSOFT FORTRAN and runs on an IBM PC AT or compatible.

- INPUT: For the input to the Conversion Program serves the circuit description file 'SLIC.OUT' which is generated by SPICE (or a file generated by measurements). This file has the format of a SPICE ac analysis containing variable values in the frequency range of 10 to 3990 Hz in steps of 10 Hz. If not all these frequency values are contained (for instance by the use of steps larger than 10 Hz in the SPICE ac analysis in order to reduce the calculation time of SPICE), the missing values and frequencies are **interpolated**.

- OUTPUT: The program converts the SPICE output file into a SLIC file (with suffix .SLI) describing the characteristics of a SLIC, and being suitable as input for the SICOFI coefficients program containing the parameter ZSLI (minimal attenuation of the SLIC at the four wire side) and the M-parameters of the SLIC for each frequency from 10 to 3990 Hz in steps of 10 Hz.

- BATCH MODE Facility: The program can be started from the keyboard or from a **batch file** (the arguments are on the same command line).

- Flexibility: The program processes the input file with flexibility by recognizing keywords in the SPICE output file:
  - the order of the different ac analyses is **indifferent**
  - the ZSLI analysis can be missing in order to reduce the calculation time (ZSLI is then set to the default value of 0.5).
  - The program recognizes three kinds of circuits: two for the M-parameter and one for the ZSLI parameter calculation. Due to the structure of the circuits being all the same, and only the loads at ring and tip being different, there might be **more circuits** available for the ZSLI calculation, however.
3.2 Batch File S.BAT
For ease of use, the steps always following each other of SLIC circuit analysis by SPICE and adaptation of the resulting output file SLIC.OUT to an input file being compatible to the SICOFI program have been combined to a batch file S.BAT. Thus in applying S.BAT to the circuit description file SLIC.CIR, the resulting output file SLIC.SLI is directly to be used as input to the SICOFI program. Circuit analysis and conversion of the intermediate results is performed by simply calling S SLIC.

Figure 5
Contents of Program S.BAT

3.3 SLIC Description by Parameters
According to its functionality the SLIC operates as a three port. To describe its electrical properties the parameters to be used in the SICOFI program are the M-parameters and the ZSLI-value. They are defined as follows:

3.3.1 M-Parameters
The SLIC and its external circuitry are accessible through a three port (see figure 6).

Figure 6
SLIC and its External Circuitry as a Three Port
$I_1, I_2$ and $I_3$ are port currents and $V_1, V_2$ and $V_3$ are port voltages. This circuit can be described by the following equation system:

1. $I_1 = M_{11} \times V_1 + M_{12} \times V_3 + M_{13} \times I_2$
2. $V_2 = M_{21} \times V_1 + M_{22} \times V_3 + M_{23} \times I_2$
3. $I_3 = M_{31} \times V_1 + M_{32} \times V_3 + M_{33} \times I_2$

**Note:** Description of a port:

When the SLIC is connected to the SICOFI, we can assume that:
- $I_2 = 0$ because of the high SICOFI input impedance.
- $I_3$ is not relevant in the following calculations because the SICOFI works as an ideal voltage generator.

According to the above remarks the equation system can be reduced to a pair of equations containing just four M-parameters:

4. $I_1 = M_{11} \times V_1 + M_{12} \times V_3$
5. $V_2 = M_{21} \times V_1 + M_{22} \times V_3$

These parameters $M_{11}, M_{12}, M_{21}, M_{22}$ fully describe the SLIC and its external circuitry. They are defined as shown in figures 7 through 10.

Please verify that circuits of figures 7 and 9 and of figures 8 and 10 respectively are identical!
Calculating SLIC Parameters

**Figure 7**
Definition of SLIC M11-Parameter

**Figure 8**
Definition of SLIC M12-Parameter

**Figure 9**
Definition of SLIC M21-Parameter
### 3.3.2 ZSLI

ZSLI is the **minimal attenuation** (resp. maximal gain) of the SLIC 4-wire side while the a/b lines are terminated by the terminal impedance $Z_t$.

ZSLI is used by the SICOFI program during automatic calculation of Z-filter coefficients as a reference to check for possible oscillations in the SICOFI Z-filter + SLIC loop.

The value is in dB and is expressed as attenuation:

$$ZSLI = -20 \times \log \left( \frac{V_2}{V_3} \right)$$

Please verify that as $V_2$ is larger than $V_3$, ZSLI is a negative quantity.

In practice the attenuation of the loop "SLIC input to SLIC output" is measured over the whole frequency band 0 – 16 kHz for different terminating impedances $Z_t$ (see chapter 4.2.1). The worst case (the smallest attenuation resp. the greatest gain) then is taken for ZSLI.
The use of SPICE allows to obtain the ZSLI value without doing measurements.

**Note:** According to the Nyquist criteria, the attenuation of the closed loop “Z filter – SLIC” must be greater than 1 (gain < 0 dB) in the frequency band 0 – 16 kHz in order to avoid any oscillation.

### 4 Example

To exemplify circuit synthesis using SPICE together with the SICOFI program, a circuitry consisting of a transformer SLIC and a SICOFI according to *figure 12* is analyzed. While the SLIC is a real circuit of fixed properties, the SICOFI is tuned by the SICOFI program as to meet particular specifications imposed by country specific requirements. Results of simulation and measurements on a sample circuit are compared.

#### 4.1 The SLIC

The SLIC used for probing the SPICE program is a transformer SLIC with series feeding and two operational amplifiers, used in certain USA Applications.

With the names of the different nodes filled in, the circuit is shown in figure 12. This circuit is described for SPICE in the file ‘SLIC2OP.LIB’ (*see Appendix A*).

Most of the components of the SLIC are standard components and can be found in the SPICE library except the transformer. Hence this component has to be modelled separately.
4.1.1 The Transformer

The transformer (Siemens ordering code: V3301-G1023-B194-4 BW/W9) consists of two primary and one secondary coils wound on an iron core Permenorm 5000 H2 1000 NH. The equivalent circuit data are calculated from measurements.
4.2 Determination of the Equivalent Circuit Components

To determine the equivalent circuit components of the circuitry involved, a series of measurements are taken. As several of these components are not directly accessible by measurement, they are calculated from measured data.

4.2.1 Modelling the Transformer

The transformer can be described in SPICE by an equivalent circuit. In this circuit each coil is substituted by its inductance, in series with its copper resistance and in parallel with its winding capacitance (see figure 13). The inductors are coupled by a common coupling factor $k$.

![Figure 13](image)

**Figure 13**
Equivalent Circuit for Transformer Used in SPICE

The values of the different components of this equivalent circuit are calculated from the measurements on the transformer.
4.2.2 Measurements on the Transformer

The whole measurement is done in 4 steps:

1. Measurement of the copper resistances of the two primary and of the secondary coils ($R_{p1}$, $R_{p2}$ and $R_s$) using a simple Ohmmeter.

   $R_{p1} = 33 \, \Omega$
   $R_{p2} = 33 \, \Omega$
   $R_s = 66 \, \Omega$

2. Measurement of the respective transformer resonance frequencies (imaginary part = 0), with open circuit at the other coils, by using an impedance analyzer.

   [parallel equivalent circuit]
   - first primary coil $\rightarrow f_{p1} = 64.03 \, \text{kHz}$
   - second primary coil $\rightarrow f_{p2} = 63.38 \, \text{kHz}$
   - secondary coil $\rightarrow f_s = 62.67 \, \text{kHz}$

3. Measurement of winding inductances $L_{p1m}$, $L_{p2m}$ and $L_{sm}$, with open circuit at the other coils at a low frequency ($f_m = 100 \, \text{Hz}$).

   [series equivalent circuit]
   - $L_{p1m} = 0.374 \, \text{H}$
   - $L_{p2m} = 0.374 \, \text{H}$
   - $L_{sm} = 1.473 \, \text{H}$

4. Measurement of the stray inductances with a short circuit at the other coils at the resonance frequency.

   [series equivalent circuit]
   - first primary coil at $f_{p1}$ $\rightarrow L_{kp1} = 30.3 \, \mu\text{H}$
   - second primary coil at $f_{p2}$ $\rightarrow L_{kp2} = 30.6 \, \mu\text{H}$
   - secondary coil at $f_s$ $\rightarrow L_{ks} = 2.108 \, \text{mH}$

4.2.3 Calculations on the Transformer

With the measurements of 4.2.2 the only true components determined yet are the copper resistances of the coils; to get the rest of the component values (inductances and capacitances) some calculations have to be performed.

- Determination of correction factors [1]:

  $\beta_{p1} = f_m / f_{p1}$
  $\beta_{p2} = f_m / f_{p2}$
  $\beta_s = f_m / f_s$

  $\beta_{p1} = f_m / f_{p1} = 100/64.03E3 = 1.562E-3$
  $\beta_{p2} = f_m / f_{p2} = 100/63.38E3 = 1.578E-3$
  $\beta_s = f_m / f_s = 100/62.67E3 = 1.596E-3$
As is to be seen, the $\beta$’s are rather small quantities compared to unity and may be neglected in many cases.

– Calculation of the actual inductances [1]:

\[
\begin{align*}
L_{p1} &= L_{p1m} (1 - \beta_{p1}^2) \\
L_{p2} &= L_{p2m} (1 - \beta_{p2}^2) \\
L_s &= L_{sm} (1 - \beta_s^2)
\end{align*}
\]

\[L_{p1} = 0.374 \text{ H} \]
\[L_{p2} = 0.374 \text{ H} \]
\[L_s = 1.473 \text{ H} \]

– Calculation of the stray factors [1]:

\[
\frac{\sigma_{p1}}{L_{p1}} \quad \frac{\sigma_{p2}}{L_{p2}} \quad \frac{\sigma_s}{L_s}
\]

\[
\begin{align*}
\sigma_{p1} &= 8.10 \times 10^{-5} \\
\sigma_{p2} &= 8.18 \times 10^{-5} \\
\sigma_s &= 1.43 \times 10^{-3}
\end{align*}
\]

– Calculation of the turns ratio [1]:

\[
n = \sqrt{\frac{L_s}{L_{p1}}} = \sqrt{\frac{L_s}{L_{p2}}}
\]

\[(9) \quad n = 1.98\]

– Evaluation of the winding capacitances [1]:

\[
\begin{align*}
C_{p1} &= \frac{n}{(2\pi f_s)^2 L_{p1} \sigma_{p1}} \\
C_{p2} &= \frac{n}{(2\pi f_s)^2 L_{p2} \sigma_{p2}} \\
C_s &= \frac{1}{(2\pi f_s)^2 L_s \sigma_s n}
\end{align*}
\]

\[
\begin{align*}
C_{p1} &= 107 \text{ nF} \\
C_{p2} &= 106 \text{ nF} \\
C_s &= 5.9 \text{ nF}
\end{align*}
\]

– Calculation of the coupling factor [1]:

\[
\begin{align*}
\kappa_{p1} &= \frac{L_{p1} - L_{kp1}}{L_{p1}} \\
\kappa_{p2} &= \frac{L_{p2} - L_{kp2}}{L_{p2}} \\
\kappa_s &= \frac{L_s - L_{ks}}{L_s}
\end{align*}
\]

\[
\begin{align*}
\kappa_{p1} &= 0.99992 \\
\kappa_{p2} &= 0.99992 \\
\kappa_s &= 0.99857
\end{align*}
\]
Because only one coupling factor for all three coils is required by SPICE and because there are small differences among the three calculated coupling factors due to measurement errors, the average of these coupling factors is taken.

\[ k = (k_{p1} + k_{p2} + k_s)/3 = 0.999468 \]

With the parameters and the names of the different nodes, the equivalent circuit of the transformer is given in figure 14 below. This circuit is described in the SPICE file 'TRAFO.LIB' (see Appendix B).

**Figure 14**
The Complete Equivalent Circuit of the Transformer
4.3 The SPICE Input File 'SLIC.CIR'

The circuit description file SLIC.CIR is the input file from which SPICE generates all the output variables necessary for the Conversion Program.

According to chapter 3.3 for calculating the M-parameters two circuits are simulated, one circuit for the parameters M11 and M21 (figures 7 and 9), and one circuit for calculating the parameters M12 and M22 (figures 8 and 10).

The M11 and M21 parameters are calculated from the frequency response of the complex variables

\[ V_1, \ \text{the voltage between "ring" and "tip" (port 1 of the SLIC)}, \]
\[ V_2, \ \text{the voltage at } V_{IN} \ \text{(port 2 of the SLIC)}, \]
\[ I_1, \ \text{the current flowing into "ring" (into port 1 of the SLIC)}. \]

The M12 and M22 parameters are calculated from the frequency response of the complex variables

\[ V_2, \ \text{the voltage at } V_{IN} \ \text{(port 2 of the SLIC)}, \]
\[ V_3, \ \text{the voltage at } V_{OUT} \ \text{(port 3 of the SLIC)}, \]
\[ I_1, \ \text{the current flowing into the ring port of the SLIC}. \]

The description for SPICE of these two circuits can be found in the first part of the file 'SLIC.CIR' (see Appendix C).

For gaining the minimal attenuation of the SLIC at the four wire side (ZSLI), accordingly three circuits are simulated with the following terminating conditions at port 1:

- one with a short circuit between "ring" and "tip",
- one with a 600 \( \Omega \) load between "ring" and "tip", and
- one with an open circuit between "ring" and "tip",

yielding three values

\[ Z_{SLI} = -20 \times \log(V_2/V_3) \]

The magnitudes of the voltages \( V_2 \) and \( V_3 \) at \( V_{IN} \) and \( V_{OUT} \) result from a SPICE ac analysis. The minimum value out of these ZSLI's is taken for calculations.

The description for SPICE of these three circuits are found in the second part of the file 'SLIC.CIR' (see Appendix C).
4.4 Format of the SPICE Output File

The output file of SPICE generated with the 'SLIC.CIR' circuit description file consists of two to five parts containing a circuit description and a frequency analysis.

Each of the parts is arranged as follows (keywords which are recognized by the Conversion Program are shown in **bold**):

- A title line with one or two keywords to identify the circuit. The keywords can be one of the following:
  - M11 and M21
  - M12 and M22
  - ZSLI

- .lib <name of library with the SLIC>
- description of test circuit
- XSLIC ring tip + 5 V – 5 V VIN VOUT <name of SLIC>
- commands for starting analysis
- .end
- analysis output of SPICE

**AC ANALYSIS**

- one of these lines:
  - FREQ VR(VIN) VI(VIN) VR(ring,tip) VI(ring,tip) or
  - FREQ IR(vmeasure) II(vmeasure) or
  - FREQ VR(VIN) VI(VIN) VR(VOUT) VI(VOUT) or
  - FREQ V(VOUT) V(VIN)

Depending on the part of the output

- empty line
- empty line
  - 1.000E+01 1.000E+00 7.167E–08 ........
  - all points of ac analysis
  - 1.600E+04 1.000E+00 1.993E–04 ........

Line without scientific reals.
In case of M-parameter calculations the second part of the analysis follows:

**AC ANALYSIS**

<table>
<thead>
<tr>
<th>FREQ</th>
<th>IR(vmeasure)</th>
<th>II(vmeasure)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.000E+01</td>
<td>1.000E+00</td>
<td>7.167E−08</td>
</tr>
</tbody>
</table>

*all points of ac analysis*

| 1.600E+04| 1.000E+00    | 1.993E−04    |

*line without scientific reals*

End of file or next part of SPICE output

The first column of the frequency analysis contains the particular frequency value, the adjacent pair of columns contains the corresponding real and imaginary parts of the variable for that frequency.
4.5 How to Use the Conversion Program 'SLIC.EXE'

To calculate the parameters of a SLIC, proceed as follows:

1. Set up a library file containing the transformer data.
2. Prepare a library file with the description of the SLIC subcircuit for PSPICE.
3. Put the name of this library file and of the subcircuit to the proper place in the 'SLIC.LIB' file.
4. Execute the PSPICE program with the 'SLIC.CIR' file as argument.
5. Execute the Conversion Program 'SLIC.EXE' with the arguments 'SLIC.OUT SLIC.SLI'
6. Then run the SICOFI program. An example of control file is given in 'SPICE.CTL'

Note: Steps 3 and 4 are put together in the batch file 'S.BAT'.
(Use 'S SLIC' without extension).

Example:
Calculation of a SLIC 'SLIC2OP' in the library file 'SLIC2OP.LIB' (to know more about how to use this file, please refer to the manual of PSPICE [2]). Editing of the words in bold of the file 'SLIC.LIB' (see figure 15).

Figure 15
The File 'SLIC.LIB' Before Editing.
Files xxxxxxxx.LIB and yyyyyyyy are renamed to the correct library file name and to the particular SLIC subcircuit name respectively.

* file for accessing the proper SLIC with no changes in the SLIC.CIR file
* change "SLIC2OP.LIB" into the name of the library file with your particular SLIC
* subcircuit .LIB xxxxxxxx.LIB
* change the model name "SLIC2OP" for the name of your particular subcircuit .subckt SLIC ring tip +5v -5v Vin Vout xownSLIC ring tip +5v -5v Vin Vout yyyyyyyy .ends SLIC
Calculating SLIC Parameters

The file after editing is shown in **Figure 16**:

**Figure 16**

The File 'SLIC.LIB' After Editing.

The bold faced words have been changed.

```
* file for accessing the proper SLIC with no changes in the
  SLIC.CIR file
* change "SLIC2OP.LIB" to the name of the library file with
  your particular SLIC
* subcircuit
  .lib SLIC2OP.LIB
* change the model name "SLIC2OP" to the name of your
  particular subcircuit
  .subckt SLIC  ring tip +5v -5v Vin Vout
  xownSLIC  ring tip +5v -5v Vin Vout  SLIC2OP
  .ends SLIC
```

Now the batch file 'S.BAT' can be executed and if there are no errors reported, the output file 'SLIC.SLI' can be used in the SICOFI program.

For the use of the SICOFI program please refer to the Software Description of the STS 2060 SICOFI COEFFICIENTS PROGRAM [3]
4.6 Format of the SICOFI® Input File

The SICOFI input file is listed below (keywords are in bold):

* PSPICE library used for calculating  | comment
* .lib SLIC.lib  | lines
* PSPICE model used for calculating  | beginning
* M-parameters  | with "*"
* xSLIC ring tip +5v -5v Vin 0 SLIC

ZSLI
.41905

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Real Part</th>
<th>Imaginary Part</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.000000</td>
<td>2.978000E-03</td>
<td>-8.219000E-04</td>
</tr>
<tr>
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<td>-7.672104E-04</td>
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<tr>
<td>............</td>
<td>.............</td>
<td>................</td>
</tr>
<tr>
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<td>1.671095E-03</td>
<td>-9.220666E-05</td>
</tr>
<tr>
<td>3990.000000</td>
<td>1.671000E-03</td>
<td>-9.240000E-05</td>
</tr>
</tbody>
</table>

M11-TABLE

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<th>Imaginary Part</th>
</tr>
</thead>
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<td>1.064000E-03</td>
</tr>
<tr>
<td>20.000000</td>
<td>6.787197E-04</td>
<td>9.931213E-04</td>
</tr>
<tr>
<td>............</td>
<td>.............</td>
<td>................</td>
</tr>
<tr>
<td>3980.000000</td>
<td>2.234000E-03</td>
<td>-9.331572E-02</td>
</tr>
<tr>
<td>3990.000000</td>
<td>2.234000E-03</td>
<td>-9.361000E-02</td>
</tr>
</tbody>
</table>

M12-TABLE

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<th>Imaginary Part</th>
</tr>
</thead>
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<td>-3.890000E-01</td>
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<tr>
<td>20.000000</td>
<td>3.144297E-02</td>
<td>-3.902608E-01</td>
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<tr>
<td>............</td>
<td>.............</td>
<td>................</td>
</tr>
<tr>
<td>3980.000000</td>
<td>-1.515000</td>
<td>9.331572E-02</td>
</tr>
<tr>
<td>3990.000000</td>
<td>-1.515000</td>
<td>9.361000E-02</td>
</tr>
</tbody>
</table>

M21-TABLE

<table>
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<th>Imaginary Part</th>
</tr>
</thead>
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<td>-2.201000E-01</td>
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<tr>
<td>20.000000</td>
<td>3.803514E-01</td>
<td>-2.266998E-01</td>
</tr>
<tr>
<td>............</td>
<td>.............</td>
<td>................</td>
</tr>
<tr>
<td>3980.000000</td>
<td>-1.515000</td>
<td>9.331572E-02</td>
</tr>
<tr>
<td>3990.000000</td>
<td>-1.515000</td>
<td>9.361000E-02</td>
</tr>
</tbody>
</table>

M22-TABLE

The leading comment lines (beginning with "*") document which SLIC is used.
The first column of the M-Parameter Tables indicates the frequency value, from 10 to 3990 Hz in steps of 10 Hz. The second column gives the real part and the third column the imaginary part values. These three values are separated by at least a single space character. Every real number must contain a decimal point. (Fortran "REAL" format.)
4.7 Results
The SLIC was simulated using the parameters 'SLIC.SLI' of the SLIC 'SLIC2OP' in 'SLIC2OP.LIB' (Appendix B), and coefficients were calculated.
The result file of the SICOFI program was stored in 'SLIC.RES' and the calculated programming bytes in 'SLIC.BYT'.
With these bytes the SICOFI has been programmed and measurements have been taken with a "PCM 4" from Wandel & Goltermann, using the real SLIC in the STUT 2060 test board as shown in Appendix E.
The measurements comprise the levels in transmit direction (AD) and in receive direction (DA), the attenuation distortion (AD and DA), the transhybrid loss (DD), and the 2-wire impedance return loss.
The plots of measurements can be found in Appendix F.
The plot masks correspond to CCITT Recommendations G.712 and G.714

4.8 Comparison of Measurements and Simulation
The results of the simulation of the return loss with Z-filter OFF (by the means of the SIM option of the SICOFI program) and of the measured data for the return loss are compared in the last diagram of Appendix F. The differences between the respective curves may be due to imperfections of the transformer model.
The measurements show that the specifications of the SLIC for USA applications (Appendix G 'USA.SPE') are met. Simulated and measured data of the SLIC’s return loss are in good agreement.

Conclusion:
Using this combination of the PSPICE program and of the 'SLIC.EXE' Conversion Program, correct coefficients for the SICOFI are easily calculated.

5 Literature
Dipl.-Ing. Günter H. Domsch
Akademische Verlagsgesellschaft
Geeest & Portig K.-G.
Leipzig

[2] PSPICE
Microsim Corporation
20 Fairbanks, Irvine, California 92718

[3] Software Description STS 2060, SICOFI Coefficients Program
Siemens A.G.
Appendix A

The Library File 'SLIC2OP.LIB'

Transformer SLIC for USA-application with 2 opamps

```
.LIB linear.lib  
.LIB trafo.lib  

.SUBCKT SLIC2OP ring tip +5V -5V VIN VOUT  
*power supply for the 3 opamps  
Vcc  +5v  0  5V  
Vee  0 -5v  5V  
C4  +5V  0  1µF  
C5  0 -5v  1µF  
*Slic, connections are ring and tip  
Xtrafo ring 1 2 tip 3 0 trafo  
Rtrafo 1 2 220  
*Impedance conversion Vin  
R5  3 10  20k  
R0  3 7  243  
C3  7 8  330nF  
R3  8 9  15k  
R4  9 0  24k  
```

*------------- amplifier ---------------------------

```
*connections:  
*                   non-inverting input  
*                   |  inverting input  
*                   |                  |  positive power supply  
*                   |                  |  negative power supply  
*                   |                  |  output  
*                   |                  |  |  type  
Xopamp1  9 10  +5V  -5V  11  LM324  
R6  10 11  75k  
C2  11 VIN  1µF  
R7  VIN 0  10k  
*Impedance conversion VOUT  
Xopamp2 0 12 +5V -5V 7 LM324  
R2  7 12  200k  
R1  12 13  150k  
C1  13 VOUT  1µF  
.ENDS
```
Appendix B

The Library File 'TRAFO.LIB'

```
trafo
.subckt trafo 1 2 3 4 5 6
  c1 1 2 1.0725E-12
  c2 3 4 1.0617E-12
  c3 5 6 3.2766E-12
  rl1 1 1a 33
  rl2 3 3a 33
  rl3 5 5a 66
  l1 1a 2 0.374
  l2 3a 4 0.374
  l3 5a 6 1.473
  k l1 l2 l3 0.999468682
.ends
```
Appendix C 1

The Test Circuit File 'SLIC.CIR'

circuit for calculating M-parameters M11 M21 (VOUT = 0)
* 
*Version 3.0
*
*To change the SLIC to your own SLIC just change in the slic.lib file all the library and SLIC
*names used in the subcircuit
*
.lib slic.lib
Vcc +5V 0 5V ; Positive Power supply
Vee 0 -5V 5V ; Negative Power supply
xslic ring tip +5V -5V VIN 0 slic
VOSC 1 tip ac 1
Vmeasure 1 ring 0 ; for measurement of current going in ring-port
rdum tip 0 10T ; for rejecting 'floating' errors from spice, see spice manual
.ac lin 39 10 3990
.print ac vr([VIN]) vi([VIN]) vr([ring],[tip]) vi([ring]),[tip])
.print ac ir(Vmeasure) ii(Vmeasure)
.options nomod
.end

circuit for calculating M-parameters M12 M22 (input short circuit)
.lib slic.lib
Vcc +5V 0 5V ; Positive Power supply
Vee 0 -5V 5V ; Negative Power supply
xslic ring tip +5V -5V VIN VOUT slic
Vmeasure tip ring 0 ; for measurement of current going in ring-port
VOSC VOUT 0 ac 1
rdum ring 0 10T ; for rejecting 'floating' errors from spice, see spice manual
.ac lin 39 10 3990
.print ac vr([VIN]) vi([VIN]) vr([VOUT]) vi([VOUT])
.print ac ir(Vmeasure) ii(Vmeasure)
.options nomod
.end

circuit for calculating ZSLI0 (ring and tip short circuit)
.lib slic.lib
Vcc +5V 0 5V ; Positive Power supply
Vee 0 -5V 5V ; Negative Power supply
xslic ring ring +5V -5V VIN VOUT slic
VOSC VOUT 0 ac 1
rdum ring 0 10T ; for rejecting 'floating' errors from spice, see spice manual
.ac lin 30 10 16.0E3
Calculating SLIC Parameters

冯编程呂

Appendix C 2

The Test Circuit File 'SLIC.CIR'

冯编程呂

rdum ring 0 10T ; for rejecting 'floating' errors from spice, see spice manual
.ac lin 30 10 16.0E3
.print ac V([VOUT]) V([VIN])
.options nomod
.end
circuit for calculating ZSLLopen (ring and tip open circuit)
.lib slic.lib
Vcc +5V 0 5V ; Positive Power supply
Vee 0 -5V 5V ; Negative Power supply
xslic ring tip +5V -5V VIN VOUT slic
VOSC VOUT 0 ac 1
rload ring tip 10T ; for rejecting 'floating' errors from spice, see spice manual
rdum ring 0 10T
.ac lin 30 10 16.0E3
.print ac V([VOUT]) V([VIN])
.options nomod
.end
Appendix D

The Converting Program in Pseudo Language.

Available on request
Diagram of the Measurement System
Appendix F

Measurements Results and Correlation

BYTE FILE
Following byte file was loaded into the SICOFI before performing the measurements:

SPICE.BYT
PSR = 36
CAM00 = 41
CAM20 = 40
CIW0 = 26,F4,80
CIW0 = 13,60,B2,3D,73,19,25,E3,2D
CIW0 = 23,70,C8,9F,7F,3B,37,04,A6
CIW0 = 2B,70,B8,AF,72,C3,9F,01,CF
CIW0 = 03,B2,EB,EC,31,22,BB,42,12
CIW0 = 0B,00,1C,3E,12,1B,5B,16,B3
CIW0 = 18,19,19,11,19
CIW0 = 30,51,12,00,BB
SIG0 = C0
CIW0 = 25,00,08,F4,78

MEASUREMENTS
LEVEL MEASUREMENTS:
(With a 1 kHz sine wave)
A-D: – 3.28 dBm0 correct but would have to be corrected in a real application
D-A:  3.00 dBm0 correct

The other measurements results from the PCM4 (Wandel & Goltermann) are shown in the next pages.

RETURN LOSS
(Reflex.Daem.)
correct

TRANS HYBRID LOSS
(Pegelmess. DD)
correct

FREQUENCY RESPONSE
(Frequenzgang)
correct

CORRELATION
The correlation between measured results and calculated results can be seen on the plots of return loss and trans hybrid loss.
### The SICOFI® File 'USA.SPE'

<table>
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<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>FREF</td>
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</tr>
<tr>
<td>VREF</td>
<td>0.7750</td>
</tr>
<tr>
<td>LAW</td>
<td>A</td>
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<td>RLX</td>
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</tr>
<tr>
<td>RLR</td>
<td>+3.0</td>
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<tr>
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<td>ZI</td>
</tr>
<tr>
<td>ZLRP1</td>
<td>600.</td>
</tr>
<tr>
<td>ZLRP2</td>
<td>0.</td>
</tr>
<tr>
<td>ZLCP1</td>
<td>0.</td>
</tr>
<tr>
<td>ZLCP2</td>
<td>0.</td>
</tr>
<tr>
<td>ZLRS</td>
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</tr>
<tr>
<td>ZLCS</td>
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<tr>
<td>ZIRP1</td>
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<tr>
<td>ZICP1</td>
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<td>ZICP2</td>
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<td>ZIRS</td>
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<tr>
<td>3.4k</td>
</tr>
<tr>
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<tr>
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</tr>
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<td>.75</td>
</tr>
<tr>
<td>100</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AD, LOWER</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR</td>
</tr>
<tr>
<td>3.4k</td>
</tr>
<tr>
<td>AT-</td>
</tr>
<tr>
<td>-.25</td>
</tr>
<tr>
<td>AT+</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>
Calculating SLIC Parameters

AD, DELAY
FR  500  600  1k  2.6k  2.8k
GD-  10k  .420  .150  .085  .150
GD+  .420  .150  .085  .150  10k

DD
FR  300  500  2.5k  3.4k
AT-  0  27  27  23
AT+  23  27  27  0

Appendix H

The SICOFL® File 'SPICE.CTL'

SPEC = USA.SPE  SLIC = SLIC.SLI
BYTE = REF.BYT  CHNR = 0,A
VERSION = 4.2  REL = N
ON = ALL
OPT = Z+X+R+B  ZXRB = NNNN
ZAUTO = N  PZIN = 11  PSP = 3
FZP = 300.0  500.0  1000.0  1300.0  1500.0
  2000.0  2500.0  2900.0  3000.0  3200.0
  3400.0  7000.0  10000.1  14000.
WFZ = 0.100  1.00  2.00  1.50  1.00
  3.00  1.00  1.00  1.00  3.00
  2.80  1.00  1.00  1.00
FR  300.00  3400.0
RDISP = Y  RREFQ = N
FX  300.00  3400.0
XDISP = Y  XREFQ = N
BAUTO = N  PB = 10  GWFB = 0.500E-01  BDF = 1
FBP = 300.0  500.0  700.0  1000.0  1500.0
  2100.0  2300.0  2900.0  3200.0  3300.0
WFB = 4.000  2.000  1.000  5.000  1.000
  2.000  1.000  5.000  1.000  1.000
APRE = 0.0  DPRE = 0.0  APOF = 0.0  DPOF = 0.0
AGR = 00  AGX = 00  TM3 = 000
Calculating SLIC Parameters

Appendix I 1

The Result File 'SPICE.RES'

```plaintext
Input_file_name: SPICE.CTL     Date: 30.06.89  18:24
SPEC = USA.SPE     SLIC = SLIC.SLI
BYTE = REF.BYT     CHNR = 0,A
PLQ = N
ON = ALL     VERSION = 4.2     SHORT = N
OPT = Z+X+R+B     ZXR = NNNN     REL = Y
ZAUTO = Y     ZREP = N     ZSIGN = 1
FZ =  300.00     3400.0     ZLIM = 2.00
      PZIN = 11     PSP = 3
FZP =  300.00     500.00     1000.0     1300.0     1500.0
      2000.0     2500.0     2900.0     3000.0     3200.0
      3400.0     7000.0     10000.     14000.
WFZ = .100     1.00     2.00     1.50     1.00
      3.00     1.00     1.00     1.00     3.00
      2.80     1.00     1.00     1.00
FR =  300.00     3400.0
RDISP = Y     RREFQ = N     RREF = .51659E-01
FX =  300.00     3400.0
XDISP = Y     XREFQ = N     XREF = -.17369
BAUTO = Y     BREP = N     BSIGN = 1
FB =  300.00     3400.0     BLIM = 2.00     BDF = 1
      PB = 10     GWFB = .500E-01
FBP =  300.00     500.00     700.00     1000.0     1500.0
      2100.0     2300.0     2900.0     3200.0     3300.0
WFB =  4.0000     2.0000     1.0000     5.0000     1.0000
      2.0000     1.0000     5.0000     1.0000     1.0000
APRE = .00     DPRE = .00     APOF = .00     DPOF = .00
AGX = 00     AGR = 00     TM3 = 000
XZQ = -.15014650E-01     .40039060E-01     .19531250E-02
      -.35644530E-01     .19042970E-01
XRQ = .99267580E+00     -.19531250E-02     .87280270E-02
      -.53710940E-02     .97656250E-03
XXQ = .10117190E+01     .88500980E-02     .67138670E-02
      -.39367680E-02     .48828130E-03
XBQ = .85937500E-01     -.10546880E+00     .16406250E+00
      -.61035160E-01     -.10961910E+00
      .10546880E+00     .31982420E-01     -.17968750E+00
      .17187500E+00     -.93261720E-01
XGQ = .52148440E+00     .18906250E+01

;```
Calculating SLIC Parameters

Bytes for Z-Filter (13): 60,B2,3D,73,19,25,E3,2D
Bytes for R-Filter (2B): 70,B8,AF,72,C3,9F,01,CF
Bytes for X-Filter (23): 70,C8,9F,7F,3B,37,04,A6
Bytes for Gain-factors (30): 51,12,00,BB
2nd part of bytes B-Filter (0B): 00,1C,3E,12,1B,5B,16,B3
1st part of bytes B-Filter (03): B2,EB,EC,31,22,BB,42,12
Bytes for B-filter delay (18): 19,19,11,19

* PSPICE library containing SLIC:
  * .lib slic2op.lib
* PSPICE model name of SLIC:
  * xownslic   ring tip +5v -5v vin vout   slic2op

Run # 1

Z-FILTER calculation results

Reference impedance for optimization:
ZIRP1 = 600.  ZICP1 = .000  ZIRP2 = 0.  ZICP2 = .000
ZIRS  = 0.  ZICS  = .000

Calculated and quantized coefficients:
XZ  =  -.01499  .04049  .00226  -.03554  .01916
XZQ =  -.01501  .04004  .00195  -.03564  .01904

Bytes for Z-Filter (13): 60,B2,3D,73,19,25,E3,2D

RETURN LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>19.065</td>
<td>2000.</td>
<td>41.828</td>
</tr>
<tr>
<td>200.</td>
<td>26.269</td>
<td>2100.</td>
<td>41.702</td>
</tr>
<tr>
<td>300.</td>
<td>29.910</td>
<td>2200.</td>
<td>41.502</td>
</tr>
<tr>
<td>400.</td>
<td>32.327</td>
<td>2300.</td>
<td>41.332</td>
</tr>
<tr>
<td>500.</td>
<td>34.117</td>
<td>2400.</td>
<td>41.168</td>
</tr>
<tr>
<td>600.</td>
<td>35.549</td>
<td>2500.</td>
<td>41.007</td>
</tr>
<tr>
<td>700.</td>
<td>36.694</td>
<td>2600.</td>
<td>40.851</td>
</tr>
<tr>
<td>800.</td>
<td>37.657</td>
<td>2700.</td>
<td>40.711</td>
</tr>
<tr>
<td>900.</td>
<td>38.519</td>
<td>2800.</td>
<td>40.586</td>
</tr>
<tr>
<td>1000.</td>
<td>39.272</td>
<td>2900.</td>
<td>40.470</td>
</tr>
<tr>
<td>1100.</td>
<td>39.931</td>
<td>3000.</td>
<td>40.349</td>
</tr>
<tr>
<td>1200.</td>
<td>40.452</td>
<td>3100.</td>
<td>40.215</td>
</tr>
</tbody>
</table>
Calculating SLIC Parameters

Appendix I 2

The Result File 'SPICE.RES'

1300.  40.845  3200.  40.057
1400.  41.244  3300.  39.855
1500.  41.552  3400.  39.627
1600.  41.770  3500.  39.365
1700.  41.898  3600.  38.957
1800.  41.942  3700.  38.460
1900.  41.911  3800.  37.871

Min. Z-loop reserve: 23.686 dB at frequency: 8500.0 Hz
Min. Z-loop mirror reserve: 28.394 dB at frequency: 9000.0 Hz

Run # 1

X-FILTER calculation results

Reference impedance for optimization:
ZIRP1 = 600.  ZICP1 = .000  ZIRP2 = 0.  ZICP2 = .000
ZIRS = 0.  ZICS = .000

Calculated and quantized coefficients:
XX  = 1.01201  .00886  .00670  -.00391  .00064
XXQ = 1.01172  .00885  .00671  -.00394  .00049
Bytes for X-Filter (23):  70,C8,9F,7F,3B,37,04,A6

X-filter attenuation function (in dB), (always absolute values)

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>-.204</td>
<td>.002</td>
<td>2000.</td>
<td>-.048</td>
<td>-.001</td>
</tr>
<tr>
<td>200.</td>
<td>-.204</td>
<td>.002</td>
<td>2100.</td>
<td>-.035</td>
<td>-.002</td>
</tr>
<tr>
<td>300.</td>
<td>-.203</td>
<td>.002</td>
<td>2200.</td>
<td>-.023</td>
<td>-.002</td>
</tr>
<tr>
<td>400.</td>
<td>-.201</td>
<td>.002</td>
<td>2300.</td>
<td>-.013</td>
<td>-.003</td>
</tr>
<tr>
<td>500.</td>
<td>-.199</td>
<td>.002</td>
<td>2400.</td>
<td>-.005</td>
<td>-.003</td>
</tr>
<tr>
<td>600.</td>
<td>-.196</td>
<td>.002</td>
<td>2500.</td>
<td>.000</td>
<td>-.003</td>
</tr>
<tr>
<td>700.</td>
<td>-.192</td>
<td>.002</td>
<td>2600.</td>
<td>.002</td>
<td>-.003</td>
</tr>
<tr>
<td>800.</td>
<td>-.187</td>
<td>.002</td>
<td>2700.</td>
<td>.001</td>
<td>-.003</td>
</tr>
<tr>
<td>900.</td>
<td>-.182</td>
<td>.002</td>
<td>2800.</td>
<td>-.003</td>
<td>-.003</td>
</tr>
<tr>
<td>1000.</td>
<td>-.175</td>
<td>.002</td>
<td>2900.</td>
<td>-.010</td>
<td>-.002</td>
</tr>
<tr>
<td>1100.</td>
<td>-.167</td>
<td>.001</td>
<td>3000.</td>
<td>-.019</td>
<td>-.002</td>
</tr>
<tr>
<td>1200.</td>
<td>-.157</td>
<td>.001</td>
<td>3100.</td>
<td>-.031</td>
<td>-.002</td>
</tr>
<tr>
<td>1300.</td>
<td>-.147</td>
<td>.001</td>
<td>3200.</td>
<td>-.044</td>
<td>-.001</td>
</tr>
<tr>
<td>1400.</td>
<td>-.135</td>
<td>.001</td>
<td>3300.</td>
<td>-.057</td>
<td>-.000</td>
</tr>
<tr>
<td>1500.</td>
<td>-.122</td>
<td>.001</td>
<td>3400.</td>
<td>-.071</td>
<td>.000</td>
</tr>
<tr>
<td>1600.</td>
<td>-.108</td>
<td>.000</td>
<td>3500.</td>
<td>-.085</td>
<td>.001</td>
</tr>
<tr>
<td>1700.</td>
<td>-.093</td>
<td>-.000</td>
<td>3600.</td>
<td>-.097</td>
<td>.001</td>
</tr>
<tr>
<td>1800.</td>
<td>-.078</td>
<td>-.001</td>
<td>3700.</td>
<td>-.107</td>
<td>.002</td>
</tr>
<tr>
<td>1900.</td>
<td>-.063</td>
<td>-.001</td>
<td>3800.</td>
<td>-.114</td>
<td>.002</td>
</tr>
</tbody>
</table>
Calculating SLIC Parameters

GX results:
All attenuation values (in dB) refer to FREF = 1014. Hz

<table>
<thead>
<tr>
<th>RLX</th>
<th>SLIC+Z</th>
<th>AGX</th>
<th>VREF/VSIC</th>
<th>XREF</th>
<th>TM3</th>
<th>GX</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3.00</td>
<td>-3.65</td>
<td>.00</td>
<td>6.17</td>
<td>-.17</td>
<td>.00</td>
<td>-5.53 ideal</td>
</tr>
<tr>
<td>-3.00</td>
<td>-3.65</td>
<td>.00</td>
<td>6.17</td>
<td>-.17</td>
<td>.00</td>
<td>-5.53 quant</td>
</tr>
</tbody>
</table>

Second byte for Gain: ,00,BB

Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGREF CA = .052 ms  TGREF CB = .065 ms

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>15.930</td>
<td>3.431</td>
<td>2000.</td>
<td>.038</td>
<td>.209</td>
</tr>
<tr>
<td>200.</td>
<td>.445</td>
<td>2.226</td>
<td>2100.</td>
<td>.045</td>
<td>.214</td>
</tr>
<tr>
<td>300.</td>
<td>.036</td>
<td>.871</td>
<td>2200.</td>
<td>.048</td>
<td>.219</td>
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<tr>
<td>400.</td>
<td>.043</td>
<td>.527</td>
<td>2300.</td>
<td>.058</td>
<td>.226</td>
</tr>
<tr>
<td>500.</td>
<td>.037</td>
<td>.387</td>
<td>2400.</td>
<td>.062</td>
<td>.234</td>
</tr>
<tr>
<td>600.</td>
<td>.024</td>
<td>.315</td>
<td>2500.</td>
<td>.065</td>
<td>.243</td>
</tr>
<tr>
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<td>.274</td>
<td>2600.</td>
<td>.067</td>
<td>.253</td>
</tr>
<tr>
<td>800.</td>
<td>.007</td>
<td>.248</td>
<td>2700.</td>
<td>.069</td>
<td>.266</td>
</tr>
<tr>
<td>900.</td>
<td>.001</td>
<td>.230</td>
<td>2800.</td>
<td>.073</td>
<td>.281</td>
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<tr>
<td>1000.</td>
<td>-.000</td>
<td>.219</td>
<td>2900.</td>
<td>.079</td>
<td>.299</td>
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<td>-.001</td>
<td>.211</td>
<td>3000.</td>
<td>.088</td>
<td>.321</td>
</tr>
<tr>
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<td>-.001</td>
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<td>3100.</td>
<td>.104</td>
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</tr>
<tr>
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<td>-.000</td>
<td>.202</td>
<td>3200.</td>
<td>.134</td>
<td>.382</td>
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<tr>
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<td>.200</td>
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<tr>
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<td>.007</td>
<td>.200</td>
<td>3400.</td>
<td>.280</td>
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<tr>
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<td>.031</td>
<td>.206</td>
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<td>2.789</td>
<td>.000</td>
</tr>
</tbody>
</table>

Run # 1
Appendix I 3

The Result File 'SPICE.RES'

R-FILTER calculation results

Reference impedance for optimization:
ZIRP1 = 600.  ZICP1 = .000  ZIRP2 = 0.  ZICP2 = .000
ZIRS  =   0.  ZICS  = .000

Calculated and quantized coefficients:
XR  = .99291  -.00166  .00870  -.00524  .00138
XRQ = .99268  -.00195  .00873  -.00537  .00098
Bytes for R-Filter (2B):   70,B8,AF,72,C3,9F,01,CF

R-filter attenuation function (in dB), (always absolute values)

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>.043</td>
<td>.000</td>
<td>2000</td>
<td>.132</td>
<td>-.002</td>
</tr>
<tr>
<td>200</td>
<td>.043</td>
<td>.000</td>
<td>2100</td>
<td>.141</td>
<td>-.002</td>
</tr>
<tr>
<td>300</td>
<td>.043</td>
<td>.000</td>
<td>2200</td>
<td>.149</td>
<td>-.003</td>
</tr>
<tr>
<td>400</td>
<td>.043</td>
<td>.001</td>
<td>2300</td>
<td>.154</td>
<td>-.003</td>
</tr>
<tr>
<td>500</td>
<td>.044</td>
<td>.001</td>
<td>2400</td>
<td>.156</td>
<td>-.003</td>
</tr>
<tr>
<td>600</td>
<td>.044</td>
<td>.001</td>
<td>2500</td>
<td>.155</td>
<td>-.003</td>
</tr>
<tr>
<td>700</td>
<td>.045</td>
<td>.001</td>
<td>2600</td>
<td>.150</td>
<td>-.003</td>
</tr>
<tr>
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<td>.046</td>
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<td>2700</td>
<td>.141</td>
<td>-.003</td>
</tr>
<tr>
<td>900</td>
<td>.048</td>
<td>.001</td>
<td>2800</td>
<td>.129</td>
<td>-.003</td>
</tr>
<tr>
<td>1000</td>
<td>.051</td>
<td>.001</td>
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<td>.112</td>
<td>-.002</td>
</tr>
<tr>
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<td>.055</td>
<td>.001</td>
<td>3000</td>
<td>.093</td>
<td>-.002</td>
</tr>
<tr>
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<td>3100</td>
<td>.071</td>
<td>-.001</td>
</tr>
<tr>
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<td>.066</td>
<td>.001</td>
<td>3200</td>
<td>.047</td>
<td>.000</td>
</tr>
<tr>
<td>1400</td>
<td>.073</td>
<td>.000</td>
<td>3300</td>
<td>.022</td>
<td>.001</td>
</tr>
<tr>
<td>1500</td>
<td>.081</td>
<td>.000</td>
<td>3400</td>
<td>-.002</td>
<td>.002</td>
</tr>
<tr>
<td>1600</td>
<td>.090</td>
<td>.000</td>
<td>3500</td>
<td>-.024</td>
<td>.003</td>
</tr>
<tr>
<td>1700</td>
<td>.100</td>
<td>-.000</td>
<td>3600</td>
<td>-.044</td>
<td>.003</td>
</tr>
<tr>
<td>1800</td>
<td>.111</td>
<td>-.001</td>
<td>3700</td>
<td>-.061</td>
<td>.004</td>
</tr>
<tr>
<td>1900</td>
<td>.122</td>
<td>-.001</td>
<td>3800</td>
<td>-.074</td>
<td>.004</td>
</tr>
</tbody>
</table>

GR results:
All attenuation values (in dB) refer to FREF = 1014. Hz

-RLR  SLIC+Z  AGR  VSIC/VREF  RREF  GR
3.00 -  3.46 -  .00 -  -6.17 -  .05 =  5.66 ideal
3.00 =  3.46 +  .00 +  -6.17 +  .05 +  5.66 quant

First byte for Gain (30):    51,12
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF = 1014.0 Hz
Calculating SLIC Parameters

TGREF CA = .241 ms      TGREF CB = .224 ms

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>1.564</td>
<td>.947</td>
<td>2000.</td>
<td>.038</td>
<td>.032</td>
</tr>
<tr>
<td>200.</td>
<td>.102</td>
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Run # 1

B-FILTER calculation results

Reference impedance for optimization:
ZLRP1 = 600.  ZLCP1 = .000  ZLRP2 = 0.  ZLCP2 = .000
ZLRS = 0.  ZLCS = .000

Calculated and quantized coefficients:
XB = .08614  -.10297  .16350  -.06106  -.10973
    .10419  .03201  -.17924  .17427  -.09337
XBQ = .08594  -.10547  .16406  -.06104  -.10962
     .10547  .03198  -.17969  .17188  -.09326
Calculating SLIC Parameters

Appendix I 4

The Result File 'SPICE.RES'

2nd part of bytes B-Filter (0B):  00,1C,3E,12,1B,5B,16,B3
1st part of bytes B-Filter (03):  B2,EB,EC,31,22,BB,42,12

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<th>loss</th>
<th>FREQ</th>
<th>loss</th>
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<td>30.941</td>
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Additional B-filter delay (in seconds):  .625E-04
Bytes for B-filter delay (18):  19,19,11,19
Appendix J

The Batch File 'S.BAT'

```
SET pspicelib = C:\pspice;C:\slic;
          |                                                |
          |          Location of the customer SPICE libraries|
          |                                             |
          | Location of the SPICE program and libraries   |

PSPICE1 %1.cir %1.out
          |                              |       |
          |        SPICE output file      |
          |  SPICE input file             |

SPICE program

SLIC   %1.out  %1.sli
          |                              |       |
          |        Converting program output = SLIC input file for|
          |                                        SICOFI program |
          |            Converting program input   |

Converting program
```
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Calculating SLIC Transfer Functions of the ERICSSON SLIC PBL 3736 Using K-Parameters and Spice

Preface

A solution to the problem of modeling SLICs and calculating SICOFI coefficients for SLICs is submitted. This is realized by combining an arbitrary SPICE program and the Conversion Program ‘KCONVERT.EXE’. The Conversion Program links the SPICE software to the SICOFI Coefficients Program. In contrast to a former Application Note (2.90), K-parameters are used for describing the SLIC. The SLIC treated is the ERICSSON SLIC PBL 3736.

A detailed description of the Conversion Program is given, and its practical use is exemplified. As an example a hardware setup is shown that meets the German as well as the US-American specifications just by programming the SICOFI correspondingly.

To read this application note with profits, the SICOFI Coefficients Program and generalities about the SLIC file format and the SPICE input files should be known.
1 Introduction

In a digital telephone system the Subscriber Line Interface makes up a very complex structure. In the past it has turned out practical for realization purposes to split one of its main functions, the hybrid function, into the actual two-to-four wire transition (Subscriber Line Interface Circuit: SLIC) and in some means of signal processing, hybrid balancing and impedance matching (Signal Processing Codec Filter: SICOFI). To make the various existing SLIC solutions operate optimally under different country specific conditions the SICOFI may be tuned to the particular SLIC by software ("coefficients" obtained by the SICOFI Coefficients Program). Therefore, however, the transfer functions of the respective SLIC must be known.

There are several ways to describe the behaviour of a SLIC. One method is to use K-parameters. In any case it is necessary to write a new program for each new type of SLIC. This process is not only time consuming but also prone to errors in the software model.

The simulation of analog circuits can also be done by using general programs like SPICE (we used a demo version* of the program PSPICE furnished byMICROSIM CORP.). Since the output file provided by SPICE is not suited as input file for the SICOFI Coefficients Program, a Conversion Program was written in FORTRAN. This conversion program converts the SPICE output file into an input file for the SICOFI Coefficients Program. It uses K-parameters in a form that is compatible with the STS 2060 SICOFI Coefficients Program. (C.f. also "Calculating SLIC Parameters Using SPICE").

In particular this Application Note shows how to match the SICOFI PEB 2060 to the ERICSSON SLIC PBL 3736.

Terminology:
SLIC: Subscriber Line Interface Circuit.
SICOFI: Signal processing Codec Filter (PEB2060).

In the following we will call "SLIC" the hardware and software corresponding to the analog components in a subscriber line interface circuit excluding the SICOFI chip.
Please note that the Conversion Program, which calculates K-parameters from the SPICE output file, is called KCONVERT.EXE.

*) The demo version is a version of reduced features of PSPICE (c.f. section 4.3). It is available on request on diskette free of charge by Siemens HL IT AT, Balanstr. 73, D-8000 München 80.
2 SICOFI® Software Principle

The main functions of a Subscriber Line Interface Circuit (SLIC) are to provide the BORSHT functions (Battery feeding, Overvoltage protection, Ringing, Signaling, Hybrid function, Testing). In the case of a SLIC being used in combination with the SICOFI, the Hybrid function is split into the two-wire to four-wire conversion realized by the SLIC, and the impedance matching, hybrid balancing and gain adjustment provided by the internal filters of the SICOFI. The other functions (such as off-hook detection, metering, standby mode, ringing) may also affect the speech signal, but will not be considered in the SLIC example described below. As has been told, the hardware can be split into two parts: The SLIC and its external circuitry on one side and the SICOFI on the other side (see figure 1).

![Figure 1](image)

**Figure 1**
SLIC-SICOFI® Hardware

According to its functions, a SLIC and its periphery make up a rather complicated circuit structure (see figure 13). Analyzing the SLIC (e.g. simulating its transfer characteristics) is facilitated in using e.g. PSPICE. In doing so the thus gained SPICE output file is not compatible with the SICOFI program; it may, however, be adapted by using the Conversion Program 'KCONVERT.EXE' (see figure 3).

![Figure 3](image)

**Figure 2**
SLIC-SICOFI® Software

In a similar way, the software consists of two major sections: The SLIC description file (.SLI file) and the SICOFI program.

![Figure 3](image)

**Figure 3**
Software Structure
The detailed structure of the SPICE and SICOFI software is shown below (figure 4).

In the following the various SPICE library files are reviewed.

PBL3736.LIB
All the specific values concerning the SLIC and its external circuitry (physical data, filter dimensions, ...) are gathered in a SPICE input file PBL3736.LIB. If you want to simulate the SLIC with a different external circuitry, you have to make the corresponding changes in this file.

KSLIC.LIB
The file KSLIC.LIB provides the description of a particular SLIC circuit via the file PBL3736.LIB. The main advantage of this procedure is, that the file KSLIC.LIB acts like a black box containing the relevant SLIC: While the black box and its connections remain unchanged, the SLIC circuitry inside the box can easily be replaced by simply changing the names of the SLIC sub-circuit and it's library PBL3736.LIB.
**Calculating SLIC Transfer Functions**

**Example:** If you have a model of SLIC No.1 in the file KSLICK1.LIB and a model of SLIC No.2 in the file KSLICK2.LIB, you could do simulations of the respective SLICs by exchanging the expression "KSLICK1.LIB" for the expression "KSLICK2.LIB" (and vice versa) in the file KSLIC.LIB.

KSLIC.CIR contains the test circuits that do the necessary ac-analyses. The result is a SPICE output file. This file has to be changed depending on the line impedance and the generator impedance in your application. For an example see Appendix B: The test circuit file 'KSLIC.CIR'.

The SPICE program analyzes the test circuits and calculates voltages and currents from which the K-parameters are deduced.

The program KCONVERT.EXE then converts the output of SPICE into the file KSLIC.SLI which is compatible with the SICOFI Coefficients Program and which contains the transmission characteristics of the SLIC in the form of the K-parameters.

For easy use, the SPICE program and the conversion programs are combined in a batch file KSPICE.BAT.

This batch file is run as follows:

```
KSPICE KSLIC <Enter> (Without the .CIR suffix)
```

KSLIC.SLI is a transfer file (output/input file) between the SLIC program and the SICOFI program to introduce the SLIC circuit data (K-parameters) into the SICOFI program.

**Auxiliary Files:**

COUNTRY.SPE is an input file of the SICOFI program describing the customer specification (CCITT etc. ...) and measurement configuration parameters (e.g. terminating impedance). The actual names used are BRD.SPE and USA.SPE for the German and US-American specifications respectively.

REF.BYT indicates the name of the reference byte file. This file is used as a frame to generate a new byte file. The newly calculated coefficients are written in this frame together with predefined commands. These commands are required for sending the SICOFI coefficients from the Peripheral Board Controller PBC (PEB 2051) to the SICOFI.

KSICOFI.CTL is the control file of the SICOFI program. It contains the data controlling the optimization and simulation processes.

The SICOFI program generates the SICOFI coefficients and simulates the theoretical transfer functions of the set SLIC + SICOFI.

RESULT.RES is the output file of the SICOFI program. It contains the coefficients for programming the SICOFI and a list of the calculated results corresponding to various measurements on the set SICOFI + SLIC (e.g. return loss, frequency response, echo return loss, etc....). The actual names used are K_BRD.RES and K_USA.RES containing the calculation results according to the German and US-American specifications respectively.
3 The Conversion Program KCONVERT.EXE

3.1 Features

- The Conversion Program is written in MICROSOFT FORTRAN and runs on an IBM PC AT or compatible.

- INPUT: The circuit description file 'KSLIC.OUT' which is generated by SPICE (or a file generated from measurement data) serves as an input file for the Conversion Program. The file 'KSLIC.OUT' contains the resulting voltages of the AC-analysis executed by the SPICE program. The AC-analysis is done in steps of 10 Hz, starting at a frequency of 10 Hz and ending at a frequency of 3990 Hz. In order to reduce the calculation time frequency steps larger than 10 Hz may be used. In this case the missing values are interpolated.

- OUTPUT: The program converts the SPICE output file into a SLIC file (with suffix .SLI). This *.SLI file describing the characteristics of a SLIC is used as an input file for the SICOFI Coefficients Program. The *.SLI file contains the parameter ZSLI (minimal attenuation of the SLIC at the four wire side) and the K-parameters of the SLIC for each frequency from 10 Hz up to 3990 Hz in steps of 10 Hz.

- BATCH MODE Facility: The program can be started by the batch file KSPICE.BAT. Just type:
  KSPICE KSLIC <enter> (without the suffix .CIR)

or else it can be started from the keyboard by typing:

PSPICE1 KSLIC.CIR KSLIC.OUT <enter>
KCONVERT KSLIC.OUT KSLIC.SLI <enter>

- Flexibility: The program recognizes keywords in the SPICE output file. That is:
  - the order of the various AC-analyses does not make a difference
  - the ZSLI analysis can be missing in order to reduce the calculation time (ZSLI is then set to the default value of 0.5).
  - The program recognizes three kinds of circuits: two for the K-parameters and one for the ZSLI parameter calculation. Since the ZSLI value is calculated from different load impedances (e.g. 600 Ω, open/short circuit) there are several circuits available for the ac-analysis of ZSLI.
3.2 Batch File KSPICE.BAT

For a convenient use of the software, the sequence of steps necessary to run a complete analysis and to do the conversion of the SPICE output file into a SICOFI input file has been combined in a batch file. Thus by starting KSPICE.BAT for the circuit description file KSLIC.CIR, the resulting output file KSLIC.SLI can directly be used as an input for the SICOFI program. Circuit analysis and conversion of the intermediate results is performed by starting the batch file ‘KSPICE.BAT’ with the proper argument.

![Figure 5](ITS02501)

Contents of Program KSPICE.BAT

3.3 SLIC Description by K-Parameters

According to its functionality the SLIC operates as a three port. To describe its electrical properties five parameters are used in the SICOFI program: The four K-parameters and the ZSLI-value.

The ERICSSON SLIC PBL 3736 has a current output. Therefore we need to work with K-Parameters (not M-parameters!) which do not require to short-circuit the output of the SLIC.

3.3.1 K-Parameters

A SLIC with a generator $V_g$ and a line impedance $Z_g$ across the a/b lines can be considered as a three port. It can be described by the currents and voltages at these three ports: $V_1, I_1, V_2, I_2, V_3, I_3$ (see figure 6).

![Figure 6](ITS02502)

SLIC and its External Circuitry as a Three Port
Three equations are sufficient to describe the SLIC completely and any linear combination of the variables is possible.

Taking account of the symmetry at the a/b port let us take the following substitution:

(1) \( a_1 = V_1 + Z_g \times I_1 \)
(2) \( b_1 = V_1 - Z_g \times I_1 \)

Using these new variables the following equations can now be written:

(3) \( b_1 = K_{11} \times a_1 + K_{12} \times V_3 + K_{13} \times I_2 \)
(4) \( V_2 = K_{21} \times a_1 + K_{22} \times V_3 + K_{23} \times I_2 \)
(5) \( I_3 = K_{31} \times a_1 + K_{32} \times V_3 + K_{33} \times I_2 \)

When the SLIC is connected to the SICOFI, we can assume that:

- \( I_2 = 0 \) because the input impedance of the SICOFI is very high.
- \( I_3 \) is not relevant in the SICOFI calculations because the SICOFI works as an ideal voltage generator.

According to these remarks, the equations system can be simplified as follows:

(6) \( b_1 = K_{11} \times a_1 + K_{12} \times V_3 \)
(7) \( V_2 = K_{21} \times a_1 + K_{22} \times V_3 \)
Calculating SLIC Transfer Functions

Figure 7
Definition of SLIC K11-Parameter

\[ K_{11} = \frac{Z_{in} - Z_g}{Z_{in} + Z_g} \text{ for } V_3 = 0 \]

Figure 8
Definition of SLIC K12-Parameter

\[ K_{12} = 2 \times \frac{V_1}{V_3} \text{ for } V_1 = -Z_g \times I_1 \]

Figure 9
Definition of SLIC K21-Parameter

\[ K_{21} = \frac{V_2}{V_g} \text{ for } V_3 = 0 \]
ZSLI is the minimal attenuation (resp. maximal gain) of the SLIC 4-wire side while the a/b lines are terminated by the terminal impedance $Z_t$ (see section 4.4).

The value is in dB and is expressed as attenuation:

$$\text{ZSLI} = -20 \times \log \left( \frac{V_2}{V_3} \right)$$

→ Please verify that as $V_2$ is larger than $V_3$, ZSLI is a negative quantity.

In practice the attenuation of the loop “SLIC input to SLIC output” is measured over the whole frequency band 0 – 16 kHz for different terminating impedances $Z_t$. The worst case (the smallest attenuation resp. the greatest gain) then is taken for ZSLI.

The use of SPICE allows to obtain the ZSLI value without doing measurements.

Note: According to the Nyquist criteria, the attenuation of the closed loop “Z filter – SLIC” must be greater than 1 (gain < 0 dB) in the frequency band 0 – 16 kHz in order to avoid any oscillation.
4 Example
To exemplify the synthesis of SPICE and the SICOFI program, a circuitry consisting of the ERICSSON SLIC PBL 3736 and a SICOFI is analyzed. While the SLIC is a real circuit of fixed properties, the SICOFI is tuned by the SICOFI program as to meet particular specifications imposed by country specific requirements.

The results of the simulation and of the measurements of a sample circuit are compared.

4.1 Basic Set-up of SICOFI® and SLIC PBL 3736

![Figure 12: Basic Set-Up of SICOFI® and ERICSSON SLIC PBL 3736]
The values of the components in figure 12 are:

**Capacitors:**
- \( C_R = 2.2 \text{ nF} \)
- \( C_T = 2.2 \text{ nF} \)
- \( C_{HP} = 0.2 \text{ µF} \)
- \( C_{DC} = 0.15 \text{ µF} \)
- \( C_{TX} = 1 \text{ µF} \)

**Resistors:** (1/4 W, 10% unless specified otherwise)
- \( R_F = 20 \text{ Ω} \)
- \( R_T = 560 \text{ kΩ} 0.5\% \)
- \( R_{RX} = 300 \text{ kΩ} 0.5\% \)
- \( R_{DC1} = 20 \text{ kΩ} \)
- \( R_{DC2} = 20 \text{ kΩ} \)
- \( R_{IX} = 22 \text{ kΩ} \)

**Note:** No attention has been paid to the overvoltage protection, signaling and loop monitoring functions in this Application Note because they should not influence the transmission characteristics.

The B-filters of the SICOFI allow for the adjustment of the transhybrid balance. Therefore we do not need to utilize the resistor \( R_b \) (connected between VIN and VOUT) for the transhybrid function (see data sheet of the ERICSSON SLIC PBL 3736).
4.2 Model of the SLIC PBL 3736

The simplified model of the SLIC is shown inside the dashed line in figure 13. This SLIC model as well as the external circuitry that is connected to the SLIC is listed in the SPICE file 'PBL3736.LIB' (see Appendix A).

Figure 13
SLIC Model and External Circuitry
The values of the different components of **figure 13** are listed below:

\[ \begin{align*}
    R_F &= 20 \ \Omega \quad \text{fuse resistors} \\
    C_T &= 2.2 \ \text{nF} \\
    C_R &= 2.2 \ \text{nF} \\
    R_{DC1} &= 20 \ \text{k}\Omega \quad \text{DC path} \\
    R_{DC2} &= 20 \ \text{k}\Omega \quad \text{DC path} \\
    C_{DC} &= 0.15 \ \mu\text{F} \quad \text{DC path} \\
    C_{HP} &= 0.2 \ \mu\text{F} \quad \text{high pass filter in transmit direction} \\
    R_T &= 560 \ \text{k}\Omega \quad \text{matching impedance} \\
    R_{RX} &= 300 \ \text{k}\Omega \quad \text{gain impedance} \\
    C_{TX} &= 1 \ \mu\text{F} \quad \text{high pass filter} \\
    R_{IX} &= 22 \ \text{k}\Omega \quad \text{high pass filter}
\end{align*} \]
4.3 How to Edit the Library File PBL3736.LIB

This chapter describes how to define a SLIC-circuit in a library file. The library file can be edited with any text editor, unless it creates embedded control characters. For this example we refer to the file PBL3736.LIB, which is listed in the appendix.

The rules for the format of SPICE files are:

- The first line is a title line, which is not part of the circuit but is used only for documentation purposes or comment.
- The last line is the .END statement.
- comment lines start with an '*' in the first column.
- continuation lines start with a '+' in the first column.

The names of parts in the circuit must begin with a letter. The following characters can be letters or numbers (example: 'RXY123' is the name of a resistor).

The nodes to which the parts are attached to can be names made up of letters and/or numbers (example: VOUT, VIN, 1, 2, 3).
Nodes "0" stand for ground.

Component values may be written in floating-point notation (example: 1.2E–6, 1.8E6) or with a scale suffix (example: 1.2 µ, 1.8 MEG).

Valid scale suffixes are:

\[ \begin{align*}
F & = 10^{-15} & \text{femto} \\
P & = 10^{-12} & \text{pico} \\
N & = 10^{-9} & \text{nano} \\
U & = 10^{-6} & \text{micro} \\
M & = 10^{-3} & \text{milli} \\
K & = 10^3 & \text{kilo} \\
MEG & = 10^6 & \text{ mega} \\
G & = 10^9 & \text{giga} \\
T & = 10^{12} & \text{tera}
\end{align*} \]

The SLIC circuit described in the file PBL3736.LIB is written in the subcircuit ERICSSONSLIC:

```
.SUBCKT ericssonslic ring tip +12 V –12 V vin vout
```

The number of nodes (here: ring, tip, +12 V, –12 V, vin, vout) in the calling program must be the same as in the subcircuit itself.

The .SUBCKT statement is followed by a listing of the components in the SLIC circuit. Itemized below are the components that can be used with the demo version of PSPICE. Elements like transistors, diodes etc. are not available. To simulate more elaborate SLIC circuits you will need the full-featured version of PSPICE.

Notation:

(name) Comment
[item] Optional item
[item]* Zero or several items
<item> Required item
<item>* One or several items
Calculating SLIC Transfer Functions

The most commonly used parts are:

**Capacitor**

general form:
C<name> <(+node) <(-node) <value>

example:
* Capacitor (first letter "C") situated between
  * | node tipx
  * | and ground
  * | | value of the capacitor (in Farad)
  * CT tipx 0 2.2 nF

**Voltage-Controlled Voltage Source** (Ideal Operational Amplifier)

general form:
E<name> <(+node) <(-node) <(+ controlling) node> + <(- controlling) node> <gain>

example:
* E(name) (+)node (-)node (+controlling) node (-controlling) node gain
  * | | | | | |  | gain
  * | | | | | |  | 1 | 1.0E4
  * | | | | | |  | E1 2 0 3

**Current-Controlled Current Source**

general form:
PF<name> <(+node) <(-node) <(controlling V device) name> <gain>

example:
* F(name) (+)node (-)node (controlling V device)name
  * | | | | | |  | gain
  * | | | | | |  | 2 | | |
  * | | | | | |  |  VRSN 0 3 F1

**Inductor Coupling**

general form:
K<name> L<(inductor) name> <L<(inductor)name>* + <(coupling) value>

example:
* inductive coupling between
  * | inductance L2 and
  * | inductance L3 with the
  * | | coupling factor K23
  * | | | K23 L2 L3 0.997

the coupling factor must be between 0 and 1.
**Inductor**
general form:
\[ L<\text{name}> <(+)\text{node}> <(-)\text{node}> [\text{(model) name}] <\text{value}> \]
example:
* Inductor (first letter "L") situated between
  * | node 1 and
  * | node 2
  * | value of the inductance (in Henry)
  * | 
\[ L2 >1<2<1.23H \]

**Resistor**
general form:
\[ R<\text{name}> <(+\text{node})> <(-\text{node})> [\text{(model) name}] <\text{value}> \]
example:
* Resistor (first letter "R") situated between
  * | node tip and
  * | node tipx
  * | value of the resistor (in Ohm)
  * | 
\[ RF1 >tip<tipx<20 \]

**Independent Voltage Source**
general form:
\[ V<\text{name}> <(+\text{node})> <(-\text{node})> [\text{DC} <\text{value}>][\text{AC} <\text{magnitude} \text{ value}> [\text{(phase) value}] \]
example:
* V(name) (+node) (−node) (dc) value
  * | | | |
  * | | | |
\[ VRSN :RSN 0 DC2 \]
4.4 The SPICE Input File 'KSLIC.CIR'

The circuit description file KSLIC.CIR is the input file from which SPICE generates all the output variables necessary for the Conversion Program.

According to chapter 3.3 two circuits are simulated, one circuit for the parameters K11 and K21 (figures 7 and 9), and one circuit for calculating the parameters K12 and K22 (figures 8 and 10).

The K11 and K21 parameters are calculated from the frequency response of the complex variables
\[ V_1 \text{, the voltage between "ring" and "tip" (port 1 of the SLIC)}, \]
\[ V_2 \text{, the voltage at VIN (port 2 of the SLIC)}, \]
\[ V_{(1a,ring)} \text{, voltage across line/generator AC impedance (across } Z_g). \]

The K12 and K22 parameters are calculated from the frequency response of the complex variables
\[ V_1 \text{, the voltage between "ring" and "tip" (port 1 of the SLIC)}, \]
\[ V_2 \text{, the voltage at VIN (port 2 of the SLIC)}, \]
\[ V_3 \text{, the voltage at VOUT (port 3 of the SLIC)}. \]

The SPICE listing of these two circuits can be found in the first part of the file 'KSLIC.CIR' (Appendix B).

In order to find the minimal attenuation of the SLIC at the four wire side (ZSLI), three circuits are simulated with the following terminating conditions at port 1:
- one with a short circuit between "ring" and "tip",
- one with a 600 \( \Omega \) or a complex load between "ring" and "tip",
- and
- one with an open circuit between "ring" and "tip".

This yields three values for
\[ Z_{SLI} = -20 \times \log(V_2/V_3) \]

The magnitudes of the voltages \( V_2 \) and \( V_3 \) at VIN and VOUT result from a SPICE AC-analysis. The smallest attenuation value out of these ZSLI's is then used for the calculations.

The SPICE listing of these three circuits are found in the second part of the file 'KSLIC.CIR' (Appendix B).
4.5 Format of the SPICE Output File

The output file of SPICE generated by the circuit description file ‘KSLIC.CIR’ consists of the AC-analyses for the K-parameters and the AC-analyses for the ZSLI values.

Each of these AC-analyses is arranged as follows (keywords which are recognized by the Conversion Program are printed in bold types):

a) A title line with one or two keywords to identify the circuit. The keywords can be one of the following:
   - K11 and K21
   - K12 and K22
   - ZSLI

b) Name of the library with the SLIC
   .lib <name of library with the SLIC>

c) description of test circuit
   XSLIC ring tip + 5 V – 5V VIN VOUT <name of SLIC>
   commands for starting analysis
   .
   .end

d) AC-analysis output of SPICE
   AC ANALYSIS
   one of these lines:
   FREQ VR(VIN) VI(VIN) VR(ring,tip) VI(ring,tip) or
   FREQ VR(VIN) VI(VIN) VR(VOUT) VI(VOUT) or
   FREQ VR(1a,ring) VI(1a,ring) or
   FREQ VR(ring,tip) VI(ring,tip) or
   FREQ V(VOUT) V(VIN) depending on the part of the output
   empty line
   empty line
   1.000E+01 1.000E+00 7.167E- 08 ...........
   all points of ac analysis
   1.600E+04 1.000E+00 1.993E- 04 ...........
   line without scientific reals.
End of file or next part of SPICE output.

The first column of the AC-analysis shows the frequency value, the adjacent columns contain the corresponding real and imaginary parts of the variable for that particular frequency.

The Conversion Program will use this Spice output data to calculate the four K-parameters. The SPICE output contains only voltages. All K-parameters can easily be calculated from these voltages. As K11 originally is represented by impedances (see figure 7), the equivalence of the representation by voltages and impedances is shown below.

\[
K_{11} = \frac{V_{\text{ring,tip}} - V_{\text{1a,ring}}}{V_{\text{ring,tip}} + V_{\text{1a,ring}}} = \frac{V_1 - V_{\text{1a,ring}}}{I_1} - \frac{V_{\text{1a,ring}}}{I_1} = \frac{Z_\text{in} - Z_\text{g}}{Z_\text{in} + Z_\text{g}}
\]
4.6 How to Use the Conversion Program ‘KCONVERT.EXE’

To calculate the parameters of a SLIC, proceed as follows:

1. Set up a library file containing the SLIC data.
2. Prepare a library file with the description of the SLIC subcircuit for SPICE.
3. Put the name of this library file and of the subcircuit to the proper place in the 'KSLIC.LIB' file.
4. Execute the SPICE program with the 'KSLIC.CIR' file as argument.
5. Execute the Conversion Program 'KCONVERT.EXE' with the arguments 'KSLIC.OUT KSLIC.SLI'
6. Then run the SICOFI program. An example of a control file is given in 'KSICOFI.CTL'

Note: Steps 3 and 4 are put together in the batch file 'KSPICE.BAT'.
(Type: 'KSPICE KSLIC' <enter> without extension).

Example:
Calculation of the SLIC 'PBL3736' in the library file 'PBL3736.LIB' (for more information on how to use this file, please refer to the manual of PSPICE [2]).
Words to be edited in the file 'KSLIC.LIB' are printed in **bold** types (see figure 14).

**Figure 14**
The File 'KSLIC.LIB' Before Editing. The spaces for xxxxxxxx.LIB and yyyyyyyyy are to be filled with the correct library file name and the particular SLIC subcircuit name.

```
* file for accessing the proper SLIC with no changes in the
* KSLIC.CIR file
*
* change "xxxxxxx.LIB" into the name of the library file
* with your particular SLIC subcircuit
.LIB xxxxxxxx.LIB
*
* change the model name "yyyyyyyy" into the name of your
* particular subcircuit
.subckt SLIC ring tip +5V -5V VIN VOUT
xownSLIC ring tip +5V -5V VIN VOUT   YYYYYY
.ENDS KSLIC
```
After editing, the file looks as follows (see figure 15):

**Figure 15**
The File 'KSLIC.LIB' After Editing. The bold typed words have been changed.

```plaintext
* file for accessing the proper SLIC with no changes in the *
KSLIC.CIR file
*
* change "KSLIC.LIB" into the name of the library file with *
* your particular SLIC subcircuit

.LIB KSLIC.LIB

* change the model name "ERICSSONSLIC" to the name of your *
* particular subcircuit

.subckt SLIC ring tip +5V -5V VIN VOUT
xownSLIC ring tip +5V -5V VIN VOUT   ERICSSONSLIC

.ENDS KSLIC
```

Now the batch file 'KSPICE.BAT' can be executed and unless errors are reported, the output file 'KSLIC.SLI' can be used in the SICOFI program.
For the use of the SICOFI program please refer to the Software Description of the STS 2060 SICOFI COEFFICIENTS PROGRAM [3]
### 4.7 Format of the SICOFI® Input File

The SICOFI input file is listed below (keywords are set in bold type):

```
* PSPICE library used for calculating | comment
* .lib KSLIC.lib | lines
* PSPICE model used for calculating    | start
* K-parameters                     | with "*
* xSLIC ring tip +5v -5v Vin 0 SLIC

ZSLI .41905

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Real Part</th>
<th>Imaginary Part</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.000000</td>
<td>2.978000E-03</td>
<td>-8.219000E-04</td>
</tr>
<tr>
<td>20.000000</td>
<td>2.856892E-03</td>
<td>-7.672104E-04</td>
</tr>
<tr>
<td>3980.000000</td>
<td>1.671095E-03</td>
<td>-9.220666E-05</td>
</tr>
<tr>
<td>3990.000000</td>
<td>1.671000E-03</td>
<td>-9.240000E-05</td>
</tr>
</tbody>
</table>

K12-TABLE

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Real Part</th>
<th>Imaginary Part</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.000000</td>
<td>5.185000E-04</td>
<td>1.064000E-03</td>
</tr>
<tr>
<td>20.000000</td>
<td>6.787197E-04</td>
<td>9.931213E-04</td>
</tr>
<tr>
<td>3980.000000</td>
<td>2.234000E-03</td>
<td>-1.258381E-04</td>
</tr>
<tr>
<td>3990.000000</td>
<td>2.234000E-03</td>
<td>-1.262000E-04</td>
</tr>
</tbody>
</table>

K21-TABLE

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Real Part</th>
<th>Imaginary Part</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.000000</td>
<td>1.864000E-01</td>
<td>-3.890000E-01</td>
</tr>
<tr>
<td>20.000000</td>
<td>3.144297E-02</td>
<td>-3.902608E-01</td>
</tr>
<tr>
<td>3980.000000</td>
<td>-1.515000</td>
<td>9.331572E-02</td>
</tr>
<tr>
<td>3990.000000</td>
<td>-1.515000</td>
<td>9.361000E-02</td>
</tr>
</tbody>
</table>

K22-TABLE

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Real Part</th>
<th>Imaginary Part</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.000000</td>
<td>5.157000E-01</td>
<td>-2.201000E-01</td>
</tr>
<tr>
<td>20.000000</td>
<td>3.803514E-01</td>
<td>-2.266998E-01</td>
</tr>
<tr>
<td>3980.000000</td>
<td>-1.515000</td>
<td>9.331572E-02</td>
</tr>
<tr>
<td>3990.000000</td>
<td>-1.515000</td>
<td>9.361000E-02</td>
</tr>
</tbody>
</table>
```

The leading comment lines (starting with an "*") document which SLIC is being used. The first column of the K-parameter tables indicates the frequency value, running from 10 Hz to 3990 Hz in steps of 10 Hz. The second column gives the values of the real parts and the third column the values of the imaginary parts of the K-parameters. The three values listed in one line are separated by at least one space character. Each real number must contain a decimal point. (FORTRAN "REAL" format.)
4.8 Results

After simulating the SLIC, listed in the file PBL3736.LIB, the SICOFI Coefficients Program calculates the programming bytes. The result files of the SICOFI program are stored in 'K_USA.RES' and 'K_BRD.RES'; the calculated programming bytes are stored in the files 'K_USA.BYT' and 'K_BRD.BYT'.

With these bytes the SICOFI has been programmed and measurements have been taken with the Ericsson SLIC PBL3736 plugged into the STUT 2060 test board as shown in Appendix C. The measurements comprise the levels in transmit direction (AD) and in receive direction (DA), the attenuation distortion (AD and DA), the transhybrid loss (DD), and the 2-wire impedance return loss.

The plots of the measurements can be found in Appendix D. The plot masks for the return loss correspond to the German and the US-American specifications, respectively. In our example these two different country specifications are met with just one hardware setup.

4.9 Comparison between Measurement Results and Simulation Results

In Appendix D simulation results of the return loss and the transhybrid loss are compared with the measurement results.

For the Z-filter switched off, the calculated curves for the return loss are in very good agreement with the measured curves. With the Z-filters switched on, there are differences between the simulated curves and the measured curves. The same is true for the transhybrid loss. When the B-filter is switched off, the measured transhybrid loss is close to the calculated curve. With the B-filter switched on, the measured result differs from the calculated result.

The differences between the respective curves may be due to the fact that a simplified transmission model of the SLIC was used.

Conclusion:

- Using the SPICE simulation program one can model a SLIC efficiently. In combination with the Conversion Program 'KCONVERT.EXE' the K-parameters are calculated. With the K-parameters as an input to the SICOFI Coefficients Program one can compute coefficients for the SICOFI.
- A single hardware setup can meet the specifications of different countries just by programming the SICOFI with the corresponding sets of coefficients.
5 Literature

[1] PSPICE
   Microsim Corporation
   20 Fairbanks, Irvine, California 92718

[2] Software Description STS 2060, SICOFI Coefficients Program
   Version 3.x, January 1989
   Siemens A.G.
Appendix A
Library File 'PBL3736.LIB'

ERICSSON Slic PBL3736

* Version 1.0 by M. Beck (based on simulations done by T. Selden (Rolm)
  and M. van Buuren)

* If you want to change the external circuitry of the SLIC PBL 3736, you have to make
  changes in this file (see external circuitry)
  example: instead of having a 299 kΩ resistor between the nodes RSN and VOUT
  you would like to have a 200 kΩ resistor. In this case you would
  replace the line
  RRX rsn vout 299 k
  by the line
  RRX rsn vout 200 k

* RING TIP VCC VEE VIN VOUT
  |||||||
  .SUBCKT ericssonslic ring tip +12 V -12 V vin vout

* Resistances to avoid "floating nodes"

Rdummy1 +12 V 0 10G
Rdummy2 -12 V 0 10G

* External Circuitry

* Resistor (first letter "R") situated between
  node1
  and node2
  value of the resistor (in Ω)

RF1 tip tipx 20
RF2 ring ringx 20
RDC1 rdc 9 20 k
RDC2 9 rsn 20 k
RT vtx rsn 560 k
RIX vin 0 21.92 k
RRX rsn vout 299 k

*
Calculating SLIC Transfer Functions

* Capacitor (first letter "C") situated between
  * node1
  * and node2
  * value of the capacitor (in Farad)
* CT  tipx  0  2.2 nF
* CR  ringx  0  2.2 nF
* CDC  9  0  0.15 µF
* CTX  vtx vin  0.981 µF
* CHP  10  0  0.2205 µF

* simplified ac transmission circuit of the SLIC

* Resistor (first letter "R") situated between
  * node1
  * and node2
  * value of the resistor (in Ω)
* RF1a  tipx  1  20
* RF2a  ringx  4  20
* ROP1  1  2  1
* ROP2  4  5  1
* ROP3  tipx  3  9.98 k
* ROP4  ringx  6  9.98 k
* RHP  7  10  401.9 k
* RLP1  7  7a  20

* Capacitor (first letter "C") situated between
  * node1
  * and node2
  * value of the capacitor (in Farad)
* C7  1  0  6000 µF
* C8  4  0  6000 µF
* C9  7a  0  6000 µF

* Independent Voltage Source

* V(name)  (+)node  (–)node  (dc)value
* VRSN  RSN  0  DC 0

* Current controlled Current Source
### Calculating SLIC Transfer Functions

* F(name)  (+)node  (–)node  (controlling V device) name
* | | | | gain
* | | | | |
F1  3  0  VRSN  2
F2  0  6  VRSN  2

* Voltage-controlled Voltage Sources
* E(name)  (+)node  (–)node
* | | | (+controlling) node
* | | | | (–controlling) node
* | | | | gain
* | | | | |
E1  2  0  3  1  1.0E4
E2  5  0  6  4  1.0E4
E3  7  0  tipx  ringx  1.0
E4  rdc  0  7a  0  0.05
E5  vtx  0  7  10  1.0

.ENDS ericsson slic
.END
Appendix B
Test Circuit 'KSLIC.CIR'

circuit for calculating K-parameters

* This program does an ac-analysis of the SLIC circuit. The results of the ac-analysis are
* used to calculate the K-parameters of the SLIC circuit (see chapter 3.3.1 K-parameters).

* Version 3.1 by Ed van Leeuwen
* Version 3.2 by Mark van Buuren
* Version 3.3 by Klaus Kliese, Manfred Beck

* Note:
* This ac-analysis is valid for a 600 Ω impedance (USA requirements). If you wish to
* do calculations for other country specifications, you have to change the generator
* impedance Rg and the load impedance Rload. To give you an example, the
* generator and the load impedances according to the German requirements (complex
* impedances) are written as comment lines below the impedances of the US-American
* requirements

* circuit for calculating K-parameters K11 K21 (vout = 0)
  .lib kslic.lib
  vcc +12V 0 12V
  vee 0 –12V 12V
  xslic ring tip +12V –12V vin vout SLIC
  vg 1a tip ac 1.0
  vosc vout 0 dc 0
  * generator impedance according to US-American requirements
  Rg 1a ring 600
  * generator impedance according to German requirements
  * Rgs 1a 1b 220
  * Rgp 1b ring 820
  * Cgp 1b ring 115 nF
  .ac lin 399 10 3990
  .print ac vr([vin]) vi([vin]) vr([ring],[tip]) vi([ring],[tip])
  .print ac vr([1a,ring]) vi([1a,ring])
  .options nomod
  .probe ; *ipsp*
  .end

circuit for calculating K-parameters K12 K22 (V1 = –Zg.i1)
  .lib kslic.lib
  vcc +12V 0 12V
  vee 0 –12V 12V
  xslic ring tip +12v –12v vin vout slic
  vosc vout 0 ac 1.0
  * generator impedance according to US-American requirements
Calculating SLIC Transfer Functions

Rg ring tip 600
* generator impedance according to German requirements
* Rgs ring 1a 220
* Rgp 1a tip 820
* Cgp 1a tip 115 nF
.ac lin 399 10 3990
.print ac vr([vin]) vi([vin]) vr([vout]) vi([vout])
.print ac vr([ring],[tip]) vi([ring],[tip])
.options nomod
.probe
.end

circuit for calculating ZSLI0 (ring and tip short circuit)
.lib kslic.lib
Vcc +12v 0 12v
Vee 0 –12v 12v
xslic ring tip +12v –12v vin vout slic
vosc vout 0 ac 1.0
vload ring tip 0
.ac lin 30 10 16.0E3
.print ac v([vout]) v([vin])
.options nomod
.probe
.end

circuit for calculating ZSLIload (load impedance between ring and tip)
.lib kslic.lib
Vcc +12v 0 12v
Vee 0 –12v 12v
xslic ring tip +12v –12v vin vout slic
vosc vout 0 ac 1.0
* load impedance according to US-American requirements
rload ring tip 600
* load impedance according to German requirements
* Rloads ring 1a 220
* Rloadp 1a tip 820
* Cloadp 1a tip 115 nF
.ac lin 30 10 16.0E3
.print ac v([vout]) v([vin])
.options nomod
.probe
.end

circuit for calculating ZSLIopen (ring and tip open circuit)
.lib kslic.lib
Vcc +12v 0 12v
Vee 0 –12v 12v
xslic ring tip +12v –12v vin vout slic
vosc vout 0 ac 1.0
rload ring tip 10T ; for rejecting 'floating' errors from spice, see spicemanual
.ac lin 30 10 16.0E3
.print ac v([vout]) v([vin])
.options nomod
.end
Appendix C

Diagram of the Measurement System
Plots of Measurements | USA Specification: Return Loss

1. Measured, Filters ON
2. Calculated, Filters ON
3. Measured, Filters OFF
4. Calculated, Filters OFF
<table>
<thead>
<tr>
<th>FREQ/Hz</th>
<th>RES/dBm0</th>
<th>FREQ/Hz</th>
<th>RES/dBm0</th>
</tr>
</thead>
<tbody>
<tr>
<td>201</td>
<td>-0.38</td>
<td>2208</td>
<td>-0.16</td>
</tr>
<tr>
<td>301</td>
<td>-0.06</td>
<td>2309</td>
<td>-0.19</td>
</tr>
<tr>
<td>402</td>
<td>-0.12</td>
<td>2409</td>
<td>-0.20</td>
</tr>
<tr>
<td>502</td>
<td>-0.10</td>
<td>2509</td>
<td>-0.19</td>
</tr>
<tr>
<td>602</td>
<td>-0.08</td>
<td>2610</td>
<td>-0.20</td>
</tr>
<tr>
<td>703</td>
<td>-0.06</td>
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<td>-0.21</td>
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USA Specification: Transmit Level (A–D)
USA Specification: Deviation from Reference Level (0 dB), Transmit Direction
### USA Specification: Level in Receive Direction (D–A)

#### FREQ/Hz | RES/dBm0
---|---
201 | -0.01
301 | 0.01
402 | -0.01
502 | 0.01
602 | 0.02
703 | 0.03
803 | 0.03
903 | 0.03
1004 | 0.03
1104 | 0.03
1205 | 0.02
1305 | 0.01
1405 | 0.00
1506 | -0.01
1606 | -0.02
1706 | -0.03
1807 | -0.04
1907 | -0.06
2008 | -0.07
2108 | -0.08
2208 | -0.09
2309 | -0.10
2409 | -0.11
2509 | -0.13
2610 | -0.14
2710 | -0.15
2811 | -0.16
2911 | -0.18
3011 | -0.20
3112 | -0.22
3212 | -0.26
3312 | -0.31
3413 | -0.41
3513 | -0.56

**Notes:**
- Δ = 100Hz
- The table above lists the frequency and level specifications for the receive direction (D–A) of the SLIC transfer functions.
USA Specification: Deviation from Reference Level (0 dB), Receive Direction
USA Specification: Transhybrid Loss (D–D)

1. Measured
2. Calculated
German Specification: Return Loss

1. Measured, Filters ON
2. Calculated, Filters ON
3. Measured, Filters OFF
4. Calculated, Filters OFF
German Specification: Transmit Level (A–D)

<table>
<thead>
<tr>
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<th>FREQ/Hz</th>
<th>RES/µV</th>
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German Specification: Deviation from Reference Level (0 dB), Transmit Direction
### Calculating SLIC Transfer Functions

**German Specification: Level in Receive Direction (D–A)**

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<tr>
<td>502</td>
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<td>602</td>
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<td>803</td>
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</tr>
<tr>
<td>903</td>
<td>-7.04</td>
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<tr>
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<tr>
<td>1104</td>
<td>-7.02</td>
</tr>
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<td>1205</td>
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<td>2008</td>
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</tr>
<tr>
<td>2108</td>
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</table>

**Modus A11 Pegelmessung**

- **SE:** +0.00 dBm0
- **FREQ:** 201 Hz
- **Δ:** 100 Hz

**Specifications:**

- **dBm0**
- **EM:**
  - ZKAN 2
- **RESULT**
  - 1004

**Diagram:**

- **A-A**
- **A-D**
- **D-A**
- **D-D**
- **WOB/E**
- **FREQ.**
German Specification: Deviation from Reference Level (−7 dB), Receive Direction

German Specification: Transhybrid Loss (D–D)

1  Measured
2  Calculated
German Specification: Transhybrid Loss (D–D)

1  Measured
2  Calculated
### Calculating SLIC Transfer Functions

**Appendix E**

**SICOFI® File 'USA.SPE'**

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</tr>
<tr>
<td>AT+</td>
<td>23</td>
</tr>
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</table>

- **FR** are frequencies in Hz.
- **AT-** and **AT+** are attenuation values in dB.
- **Z** are impedances in ohms.
- **GD** are group delays in seconds.
- **DD** are delay denominators.

#### Frequency Response Tables

**DA, UPPER**

<table>
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**DA, LOWER**

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**DA, DELAY**

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<td>.085</td>
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**DD**

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### SICOFi® File 'BRD.SPE'

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#### DA, UPPER
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#### DA, LOWER
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#### DA, DELAY
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#### AD, UPPER
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<th>Value</th>
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</thead>
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#### AD, LOWER
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#### AD, DELAY
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<th>Value</th>
<th>Value</th>
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</thead>
<tbody>
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<td>1k</td>
<td>2.6k</td>
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<tr>
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#### DD
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<th>Value</th>
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</thead>
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<td>23</td>
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Appendix F
Control File 'KSICOFI.CTL'

SPEC = USA.SPE  SLIC = KSLIC.SLI
BYTE = REF1.BYT  CHNR = 0,A
PEB = 2060  VERSION = 4.4  REL = Y
ON = ALL
OPT = Z+X+R+B  ZXRB = NNNN
PZIN = 11  PSP = 3
FZP =
   300.0  500.0  1000.0  1300.0  1500.0
   2000.0  2500.0  2900.0  3000.0  3200.0
   3400.0  7000.0  10000  14000.
WFZ =
   0.100  1.00  2.00  1.50  1.00
   3.00  1.00  1.00  1.00  3.00
   2.80  1.00  1.00  1.00
ZAUTO = Y  FZ = 300 3400
FR 300.00  3400.0
RDISP = N  RREFQ = N
FX 300.00  3400.0
XDISP = N  XREFQ = N
PB = 10  GWFB = 0.500E-01  BDF = 1
FBP =
   300.0  500.0  700.0  1000.0  1500.0
   2100.0  2300.0  2900.0  3200.0  3300.0
WFB =
   4.000  2.000  1.000  5.000  1.000
   2.000  1.000  5.000  1.000  1.000
BAUTO = Y  FB = 300 3400
APRE = 0.0  DPRE = 0.0  APOF = 0.0  DPOF = 0.0
AGR = 00  AGX = 00  TM3 = 000
Calculating SLIC Transfer Functions

Appendix G
Result File 'K_USA.RES'

Input_file_name: KSICOFI.CTL Date:13.03.91 09:37

SPEC = USA.SPE  SLIC = KSLIC.SLI
BYTE = REF.BYT  CHNR = 0,A
PLQ = N
ON = ALL  PEB = 2060  VERSION = 4.4  SHORT = N
OPT = Z+X+R+B  ZXRB = NNNN  REL = Y
ZAUTO = Y  ZREP = N  ZSIGN = 1

FZ = 300.00  3400.0  ZLIM = 2.00
PZIN = 11  PSP = 3

FZP =
  300.00  500.00  1000.0  1300.0  1500.0
  2000.0  2500.0  2900.0  3000.0  3200.0
  3400.0  7000.0 10000.0  14000.

WFZ =
  1.00  1.00  2.00  1.50  1.00
  3.00  1.00  1.00  1.00  3.00
  2.80  1.00  1.00  1.00

FR = 300.00  3400.0
RDISP = N  RREFQ = N  RREF = .31626E-01
FX = 300.00  3400.0
XDISP = N  XREFQ = N  XREF = -.42733
BAUTO = Y  BREP = N  BSIGN = 1

FB = 300.00  3400.0  BLIM = 2.00  BDF = 1
PB = 10  GWFB = .500E-01

FBP =
  300.00  500.00  700.00  1000.0  1500.0
  2100.0  2300.0  2900.0  3200.0  3300.0

WFB =
  4.0000  2.0000  1.0000  5.0000  1.0000
  2.0000  1.0000  5.0000  1.0000  1.0000

APRE = .00  DPRE = .00  APOF = .00  DPOF = .00
AGX = 00  AGR = 00  TM3 = 000

XZQ =
 -1.1523440E+00  .22656250E+00  .34179690E-01
 -2.1093750E+00  .93994140E-01

XRQ =
 .97265630E+00  .31250000E-01  -.29296880E-02
 .48828130E-03  -.19531250E-02

XXQ =
 .10273440E+01  .30883790E-01  -.19531250E-02
 .97656250E-03  -.19531250E-02

XBQ =
 -.14453130E+00  -.71875000E+00  -.25341800E+00
 .15234380E+00  .52734380E-01
 -.97656250E-01  .13183590E-01  .78613280E-01
 -.80078130E-01  .37109380E-01

XGQ =
 .53808590E+00  .21562500E+01

;
Calculating SLIC Transfer Functions

Bytes for Z-Filter (13): 30,FA,BA,52,14,C2,B1,2C
Bytes for R-Filter (2B): F0,19,87,FC,29,16,00,BD
Bytes for X-Filter (23): F0,19,87,FB,19,E5,0A,B5
Bytes for Gain-factors (30): 41,B2,00,23
2nd part of bytes B-Filter (0B): 00,35,C1,32,24,65,2B,AB
1st part of bytes B-Filter (03): 4B,2B,23,AB,B6,19,BB,23
Bytes for B-filter delay (18): 19,19,11,19
* PSPICE simulation of SLIC using K-parameters
* converted with the program KCONVERT V1.1

Run # 1
Z-FILTER calculation results

Reference impedance for optimization:
ZIRP1 = .000  ZICP1 = .000  ZIRP2 = .000  ZICP2 = .000
ZIRS  = 600.  ZICS  = .000

Calculated and quantized coefficients:
XZ  =   –.11501   .22666   .03412   –.20779   .09395
XZQ =   –.11523   .22656   .03418   –.21094   .09399
Bytes for Z-Filter (13) 30,FA,BA,52,14,C2,B1,2C

RETURN LOSS

<table>
<thead>
<tr>
<th>FREQ</th>
<th>loss</th>
<th>FREQ</th>
<th>loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Hz)</td>
<td>(dB)</td>
<td>(Hz)</td>
<td>(dB)</td>
</tr>
<tr>
<td>100.</td>
<td>32.313</td>
<td>2000.</td>
<td>32.204</td>
</tr>
<tr>
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<td>2100.</td>
<td>32.181</td>
</tr>
<tr>
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<td>2200.</td>
<td>32.157</td>
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<td>2500.</td>
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<tr>
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<td>3600.</td>
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<tr>
<td>1800.</td>
<td>32.361</td>
<td>3700.</td>
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<tr>
<td>1900.</td>
<td>32.299</td>
<td>3800.</td>
<td>27.550</td>
</tr>
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</table>

Min. Z-loop reserve: 26.008 dB at frequency: 8500.0 Hz
Min. Z-loop mirror reserve: 30.692 dB at frequency: 9000.0 Hz
Run # 1

X-FILTER calculation results

Reference impedance for optimization:
ZIRP1 = .000  ZICP1 = .000  ZIRP2 = .000  ZICP2 = .000
ZIRS  = 600.  ZICS  = .000

Calculated and quantized coefficients:
XX = 1.02808   .03087   –.00199   .00098   –.00187
XXQ = 1.02734   .03088   –.00195   .00098   –.00195

Bytes for X-Filter (23):            F0,19,87,FB,19,E5,0A,B5

GX results:
All attenuation values (in dB) refer to FREF = 1014. Hz

RLX  SLIC+Z  AGX  VREF/VSIC  XREF  TM3  GX
.00  – .78  – .00  – 6.17  –  –.43  – .00  =  –6.70 ideal
.03  = .78  + .00  + 6.17  +  –.43  + .00  =  –6.67 quant

Second byte for PEB 2060 transmit gain: ,00,23
Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGref CA = .052 ms   TGref CB = .065 ms

<table>
<thead>
<tr>
<th>FREQ</th>
<th>loss</th>
<th>GD</th>
<th>FREQ</th>
<th>loss</th>
<th>GD</th>
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<td>(dB)</td>
<td>(msec)</td>
<td>(Hz)</td>
<td>(dB)</td>
<td>(msec)</td>
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</table>
Calculated and quantized coefficients:

\[ \begin{align*}
XR &= \phantom{-}0.97294 \phantom{.}0.03127 \phantom{.}0.00286 \phantom{.}0.00037 \phantom{.}0.00198 \\
XRQ &= \phantom{-}0.97266 \phantom{.}0.03125 \phantom{.}0.00293 \phantom{.}0.00049 \phantom{.}0.00195
\end{align*} \]

Bytes for R-Filter (2B): \( F0,19,87,FC,29,16,00,BD \)

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
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<td>.039</td>
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<td>.073</td>
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<td>1.060</td>
</tr>
</tbody>
</table>
Run # 1

B-FILTER calculation results

Reference impedance for optimization:

\[ \text{ZLRP1} = .000 \quad \text{ZLCP1} = .000 \quad \text{ZLRP2} = .000 \quad \text{ZLCP2} = .000 \]
\[ \text{ZLRS} = 600. \quad \text{ZLCS} = .000 \]

Calculated and quantized coefficients:

\[ \text{XB} = -0.14825 \quad -0.71061 \quad -0.25357 \quad 0.15054 \quad 0.05259 \]
\[ -0.09832 \quad 0.01320 \quad 0.07862 \quad -0.07985 \quad 0.03775 \]
\[ \text{XBQ} = -0.14453 \quad -0.71875 \quad -0.25342 \quad 0.15234 \quad 0.05273 \]
\[ -0.09766 \quad 0.01318 \quad 0.07861 \quad -0.08008 \quad 0.03711 \]

2nd part of bytes B-Filter (0B):

\[ 00,35,C1,32,24,65,2B,AB \]

1st part of bytes B-Filter (03):

\[ 4B,2B,23,AB,B6,19,BB,23 \]

**TRANS HYBRID LOSS**

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>32.162</td>
</tr>
</tbody>
</table>

Additional B-filter delay (in seconds): .625E-04

Bytes for B-filter delay (18): 19,19,11,19
Calculating SLIC Transfer Functions

Result File 'K_BRD.RES'
Input_file_name:    KSICOFI.CTL           Date: 13.03.91   09:51
SPEC = BRD.SPE  SLIC = KSLIC.SLI
BYTE = REF.BYT  CHNR = 0,A
PLQ = N
ON = ALL  PEB = 2060  VERSION = 4.4 SHORT = N
OPT = Z+X+R+B  ZXRB = NNNN  REL = Y
ZAUTO = Y  ZREP = N  ZSIGN = 1
FZ = 300.00  3400.0  ZLIM = 2.00
PZIN = 11  PSP = 3
FZP = 300.00  500.00  1000.0  1300.0  1500.0
2000.0  2500.0  2900.0  3000.0  3200.0
3400.0  7000.0  10000  14000.
WFZ = .100  1.00  2.00  1.50  1.00
3.00  1.00  1.00  1.00  3.00
2.80  1.00  1.00  1.00
FR = 300.00  3400.0
RDISP = N  RREFQ = N  RREF = 5.6169
FX = 300.00  3400.0
XDISP = N  XREFQ = N  XREF = -.12375E-01
BAUTO = Y  BREP = N  BSIGN = 1
FB = 300.00  3400.0  BLIM = 2.00  BDF = 1
PB = 10  GWFB = .500E-01
FBP = 300.00  500.00  700.00  1000.0  1500.0
2100.0  2300.0  2900.0  3200.0  3300.0
WFB = 4.0000  2.0000  1.0000  5.0000  1.0000
2.0000  1.0000  5.0000  1.0000  1.0000
APRE = .00  DPRE = .00  APOF = .00  DPOF = .00
AGX = 00  AGR = 01  TM3 = 000
XZQ = -.37695310E+00  -.32812500E+00  .61279300E-01
.22656250E+00  -.89843750E-01
.68750000E+00  -.27343750E+00  .59082030E-01
-.21484380E-01  .92773440E-02
XRQ = .10175780E+01  -.26367190E-01  .18554690E-01
-.63476560E-02  .19531250E-02
XXQ = -.66894530E-01  -.32031250E+00  -.30468750E+00
-.10925290E+00  -.22460940E-01
XBQ = .68359380E+00  .16875000E+01
XGQ = .68359380E+00  .16875000E+01
Calculating SLIC Transfer Functions

Bytes for Z-Filter (13): C0,B1,C2,41,2E,2A,92,EA
Bytes for R-Filter (2B): 70,13,2E,41,BC,4A,11,12
Bytes for X-Filter (23): 70,19,BF,61,13,BD,02,36
Bytes for Gain-factors (30): 21,C1,10,12
2nd part of bytes B-Filter (0B): 00,B6,DB,DB,B5,E1,B1,AC
1st part of bytes B-Filter (03): EC,B1,BB,A7,B2,2A,C3,34
Bytes for B-filter delay (18): 9,19,11,19
* PSPICE simulation of SLIC using K-parameters
* converted with the program KCONVERT V1.1

Run # 1
Z-FILTER calculation results

Reference impedance for optimization:
ZIRP1 = 820.  ZICP1 = .000  ZIRP2 = .000  ZICP2 = .115E–06
ZIRS = 220.  ZICS = .000

Calculated and quantized coefficients:
XZ  =   –.37740   –.32749   .06130   .22499   –.08919
XZQ =   –.37695   –.32813   .06128   .22656   –.08984
Bytes for Z-Filter (13): C0,B1,C2,41,2E,2A,92,EA

RETURN LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>27.280</td>
<td>2000.</td>
<td>29.735</td>
</tr>
<tr>
<td>200.</td>
<td>28.873</td>
<td>2100.</td>
<td>29.978</td>
</tr>
<tr>
<td>300.</td>
<td>29.137</td>
<td>2200.</td>
<td>30.346</td>
</tr>
<tr>
<td>400.</td>
<td>29.107</td>
<td>2300.</td>
<td>30.692</td>
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<tr>
<td>500.</td>
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<td>2400.</td>
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<td>600.</td>
<td>28.887</td>
<td>2500.</td>
<td>31.257</td>
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<td>700.</td>
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<td>2600.</td>
<td>31.418</td>
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<tr>
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<td>28.615</td>
<td>2700.</td>
<td>31.409</td>
</tr>
<tr>
<td>900.</td>
<td>28.492</td>
<td>2800.</td>
<td>31.322</td>
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<tr>
<td>1000.</td>
<td>28.400</td>
<td>2900.</td>
<td>31.025</td>
</tr>
<tr>
<td>1100.</td>
<td>28.374</td>
<td>3000.</td>
<td>30.598</td>
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<tr>
<td>1200.</td>
<td>28.354</td>
<td>3100.</td>
<td>30.020</td>
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<tr>
<td>1300.</td>
<td>28.399</td>
<td>3200.</td>
<td>29.324</td>
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<tr>
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<td>28.444</td>
<td>3300.</td>
<td>28.584</td>
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<tr>
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<td>27.795</td>
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<tr>
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<td>26.976</td>
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<tr>
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<td>28.913</td>
<td>3600.</td>
<td>26.197</td>
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<tr>
<td>1800.</td>
<td>29.144</td>
<td>3700.</td>
<td>25.398</td>
</tr>
<tr>
<td>1900.</td>
<td>29.395</td>
<td>3800.</td>
<td>24.658</td>
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</table>

Min. Z-loop reserve: 27.109 dB at frequency: 6000.0 Hz
Min. Z-loop mirror reserve: 30.685 dB at frequency: 6000.0 Hz
Calculating SLIC Transfer Functions

Run # 1

X-FILTER calculation results

Reference impedance for optimization:

<table>
<thead>
<tr>
<th>ZIRP1</th>
<th>ZICP1</th>
<th>ZIRP2</th>
<th>ZICP2</th>
</tr>
</thead>
<tbody>
<tr>
<td>820.</td>
<td>.000</td>
<td>.000</td>
<td>.115E-06</td>
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<tr>
<td>220.</td>
<td>.000</td>
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</table>

Calculated and quantized coefficients:

<table>
<thead>
<tr>
<th>XX</th>
<th>XXQ</th>
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<tr>
<td>1.01740</td>
<td>1.01758</td>
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<tr>
<td>-.02620</td>
<td>-.02637</td>
</tr>
<tr>
<td>.01872</td>
<td>.01855</td>
</tr>
<tr>
<td>-.00629</td>
<td>-.00635</td>
</tr>
<tr>
<td>.00217</td>
<td>.00195</td>
</tr>
</tbody>
</table>

Bytes for X-Filter (23): 70,19,BF,61,13,BD,02,36

GX results:

All attenuation values (in dB) refer to FREF = 1014. Hz

<table>
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<tr>
<th>RLX</th>
<th>SLIC+Z</th>
<th>AGX</th>
<th>VREF/VSIC</th>
<th>XREF</th>
<th>TM3</th>
<th>GX</th>
</tr>
</thead>
<tbody>
<tr>
<td>.00</td>
<td>-.01</td>
<td>-.00</td>
<td>4.41</td>
<td>-.01</td>
<td>.00</td>
<td>-4.58</td>
</tr>
<tr>
<td>-03</td>
<td>-.01</td>
<td>.00</td>
<td>4.41</td>
<td>-.01</td>
<td>.00</td>
<td>-4.54</td>
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Second byte for PEB 2060 transmit gain: ,10,12

Calculation of transmit transfer function (AD)

All attenuation values (in dB) refer to FREF = 1014.0 Hz

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<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
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<tr>
<td>200.</td>
<td>.340</td>
<td>2.019</td>
<td>2100.</td>
<td>.036</td>
<td>.212</td>
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<tr>
<td>300.</td>
<td>.010</td>
<td>.798</td>
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<td>.042</td>
<td>.216</td>
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<tr>
<td>400.</td>
<td>.034</td>
<td>.488</td>
<td>2300.</td>
<td>.049</td>
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</tr>
<tr>
<td>500.</td>
<td>.036</td>
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<td>2400.</td>
<td>.054</td>
<td>.229</td>
</tr>
<tr>
<td>600.</td>
<td>.028</td>
<td>.298</td>
<td>2500.</td>
<td>.060</td>
<td>.237</td>
</tr>
<tr>
<td>700.</td>
<td>.019</td>
<td>.261</td>
<td>2600.</td>
<td>.063</td>
<td>.250</td>
</tr>
<tr>
<td>800.</td>
<td>.010</td>
<td>.238</td>
<td>2700.</td>
<td>.064</td>
<td>.266</td>
</tr>
<tr>
<td>900.</td>
<td>.005</td>
<td>.223</td>
<td>2800.</td>
<td>.067</td>
<td>.277</td>
</tr>
<tr>
<td>1000.</td>
<td>.001</td>
<td>.212</td>
<td>2900.</td>
<td>.071</td>
<td>.297</td>
</tr>
<tr>
<td>1100.</td>
<td>-.003</td>
<td>.206</td>
<td>3000.</td>
<td>.079</td>
<td>.319</td>
</tr>
<tr>
<td>1200.</td>
<td>-.005</td>
<td>.201</td>
<td>3100.</td>
<td>.095</td>
<td>.346</td>
</tr>
<tr>
<td>1300.</td>
<td>-.008</td>
<td>.195</td>
<td>3200.</td>
<td>.126</td>
<td>.379</td>
</tr>
<tr>
<td>1400.</td>
<td>-.007</td>
<td>.199</td>
<td>3300.</td>
<td>.181</td>
<td>.423</td>
</tr>
<tr>
<td>1500.</td>
<td>-.006</td>
<td>.193</td>
<td>3400.</td>
<td>.274</td>
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<tr>
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<td>-.001</td>
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<td>.438</td>
<td>.564</td>
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<tr>
<td>1700.</td>
<td>.005</td>
<td>.200</td>
<td>3600.</td>
<td>.738</td>
<td>.680</td>
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<td>1800.</td>
<td>.010</td>
<td>.197</td>
<td>3700.</td>
<td>1.350</td>
<td>.878</td>
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<tr>
<td>1900.</td>
<td>.018</td>
<td>.202</td>
<td>3800.</td>
<td>2.829</td>
<td>.000</td>
</tr>
</tbody>
</table>
Calculating SLIC Transfer Functions

Run #1

R-FILTER calculation results

Reference impedance for optimization:

\[
\begin{align*}
Z_{IRP1} &= 820. \\
Z_{ICP1} &= 0.000 \\
Z_{IRP2} &= 0.000 \\
Z_{ICP2} &= 0.115E-06 \\
Z_{IRS} &= 220. \\
Z_{ICS} &= 0.000
\end{align*}
\]

Calculated and quantized coefficients:

\[
\begin{align*}
XR &= 0.69865 \\
XRQ &= 0.68750 \\
\text{Bytes for R-Filter (2B):} &= 70, 13, 2E, 41, BC, 4A, 11, 12
\end{align*}
\]

GR results:

All attenuation values (in dB) refer to FREF = 1014. Hz

\[
\begin{align*}
-R&L R & S L I C + Z & A G R & V S I C / V R E F & R R E F & G R \\
7.00 & -3.54 & -6.03 & -4.41 & - & 5.62 & = & 3.31 \text{ ideal} \\
7.00 & -3.54 & +6.03 & +4.41 & + & 5.62 & + & 3.30 \text{ quant}
\end{align*}
\]

First byte for PEB 2060 receive gain (30): 21, C1

Calculation of receive transfer function (DA)

All attenuation values (in dB) refer to FREF = 1014.0 Hz

\[
\begin{align*}
\text{TGREF CA} &= 0.212 \text{ ms} \\
\text{TGREF CB} &= 0.195 \text{ ms}
\end{align*}
\]

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
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<td>0.050</td>
<td>2000.</td>
<td>-0.040</td>
<td>0.047</td>
</tr>
<tr>
<td>200.</td>
<td>-0.077</td>
<td>0.013</td>
<td>2100.</td>
<td>-0.024</td>
<td>0.053</td>
</tr>
<tr>
<td>300.</td>
<td>-0.050</td>
<td>0.006</td>
<td>2200.</td>
<td>-0.008</td>
<td>0.056</td>
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<td>400.</td>
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<td>0.003</td>
<td>2300.</td>
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<td>0.066</td>
</tr>
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<td>0.074</td>
</tr>
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<td>0.010</td>
<td>0.000</td>
<td>2500.</td>
<td>0.010</td>
<td>0.085</td>
</tr>
<tr>
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<td>0.098</td>
</tr>
<tr>
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<td>0.002</td>
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<td>0.113</td>
</tr>
<tr>
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<td>0.004</td>
<td>2800.</td>
<td>-0.013</td>
<td>0.129</td>
</tr>
<tr>
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<td>0.013</td>
<td>0.005</td>
<td>2900.</td>
<td>-0.021</td>
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<tr>
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<td>0.010</td>
<td>3000.</td>
<td>-0.021</td>
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<tr>
<td>1200.</td>
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<td>0.206</td>
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<td>3200.</td>
<td>0.028</td>
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<td>3300.</td>
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<td>-0.076</td>
<td>0.025</td>
<td>3400.</td>
<td>0.222</td>
<td>0.349</td>
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<tr>
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<td>-0.075</td>
<td>0.028</td>
<td>3500.</td>
<td>0.430</td>
<td>0.429</td>
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<tr>
<td>1700.</td>
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<td>0.038</td>
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<td>3700.</td>
<td>1.478</td>
<td>0.747</td>
</tr>
<tr>
<td>1900.</td>
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<td>0.039</td>
<td>3800.</td>
<td>3.051</td>
<td>1.086</td>
</tr>
</tbody>
</table>
Run # 1

B-FILTER calculation results

Reference impedance for optimization:
ZLRP1 = 820.  ZLCP1 = .000  ZLRP2 = .000  ZLCP2 = .115E-06
ZLRS = 220.  ZLCS = .000

Calculated and quantized coefficients:
XB  =   –.06671   –.32085   –.30579   –.10920   –.02212
     –.04818   –.02290   .02514   –.02751    .01381
XBQ =   –.06689   –.32031   –.30469   –.10925   –.02246
     –.04785   –.02246   .02539   –.02747    .01392
2nd part of bytes B-Filter (0B):     00,B6,DB,DB,B5,E1,B1,AC
1st part of bytes B-Filter (03):     EC,B1,BB,A7,B2,2A,C3,34

TRANS HYBRID LOSS

<table>
<thead>
<tr>
<th>FREQ</th>
<th>loss</th>
<th>FREQ</th>
<th>loss</th>
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<tr>
<td>(Hz)</td>
<td>(dB)</td>
<td>(Hz)</td>
<td>(dB)</td>
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<tr>
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<td>58.078</td>
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<tr>
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<td>3800.</td>
<td>39.487</td>
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</tbody>
</table>

Additional B-filter delay (in seconds):  .625E-04
Bytes for B-filter delay (18):          19,19,11,19
Appendix H
The Batch File 'K.BAT'

IF EXIST *.IND DEL *.IND

PSPICE1 %1.cir %1.out

| | |
| | SPICE output file |
| | SPICE input file |

SPICE program

KCONVERT %1.out %1.sli

| | |
| | Conversion program output |
| | = SLIC input file for SICOFI program |
| | Conversion program input |

Conversion program
### Contents

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<th>Description</th>
<th>Page</th>
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<td>SLIC Connectors CON6 and CON7</td>
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<td>Solder Straps for EPROM and SICOFI®</td>
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<td>Connecting SICOFI® Testboard to PCM4</td>
<td>335</td>
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<td>2.8</td>
<td>PCM4 Programming</td>
<td>340</td>
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<td>Starting the Board</td>
<td>341</td>
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<td>4</td>
<td>Programming the Board</td>
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<td>Command PSR (Phase Shift Register)</td>
<td>342</td>
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<td>4.2</td>
<td>Command CAM (Content Addressable Memory)</td>
<td>343</td>
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<td>4.3</td>
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<td>4.4</td>
<td>Control Byte for CIW Command</td>
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<td>SOP Command</td>
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<td>357</td>
</tr>
</tbody>
</table>
1 Introduction

Using the SICOFI Testboard STUT 2060 facilitates measurement of the transfer functions of the SLIC in connection with the SICOFI. Via a RS 232 interface to a microprocessor programming the PBC or PIC, the SICOFI and SLIC is made possible. The SLIC circuit is placed on a separate board which can be connected through 64-pins connectors CON6 and CON7 to the testboard. This set-up aids in making the following investigations:

- testing the SLIC hardware
- verifying the programmed coefficients, which have been calculated with the SICOFI coefficients program
- speeding up evaluation of different SLICs

2 Hardware

The SICOFI Testboard can be broken down into the functional parts:

- power supply section
- clock supply section
- microprocessor section
- PBC/PIC section
- SICOFI section including SLIC Connectors CON6 and CON7, and CON5
Figure 1
Floor Plan of the SICOFI® Testboard STUT 2060
2.1 Power Supply Section

The board needs an external power supply. On board there is a connector (CON 1) with the following pinning:

<table>
<thead>
<tr>
<th>pin</th>
<th>terminal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+ 5 V</td>
</tr>
<tr>
<td>2</td>
<td>digital ground (DGND)</td>
</tr>
<tr>
<td>3</td>
<td>+ 12 V</td>
</tr>
<tr>
<td>4</td>
<td>analog ground (AGND)</td>
</tr>
<tr>
<td>5</td>
<td>– 48 V</td>
</tr>
<tr>
<td>6</td>
<td>battery ground (BGND)</td>
</tr>
<tr>
<td>7</td>
<td>– 5 V</td>
</tr>
<tr>
<td>8</td>
<td>ring ground (RGND) not connected</td>
</tr>
<tr>
<td>9</td>
<td>– 70 V</td>
</tr>
<tr>
<td>10</td>
<td>ring (NC)</td>
</tr>
<tr>
<td>11</td>
<td>– 70 V</td>
</tr>
</tbody>
</table>

2.2 Clock Supply Section

The clock supply provides several modes:
- external clock, external frame
- external clock, internal frame
- internal clock, internal frame

With the switch DIL 2 of the clock part, you can set up these 3 modes:

<table>
<thead>
<tr>
<th>DIL2</th>
<th>ON</th>
<th>OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>internal clock</td>
<td>external clock</td>
</tr>
<tr>
<td>S2</td>
<td>internal frame</td>
<td>external frame</td>
</tr>
</tbody>
</table>

By switching-on S1 of DIL2 (internal clock) the LED D2 is ON. External clock may be supplied at 1.536 MHz, 2.048 MHz, 3.072 MHz, or 4.096 MHz.

<table>
<thead>
<tr>
<th>DIL2</th>
<th>Clock 1.5 MHz</th>
<th>Clock 2 MHz</th>
<th>Clock 3 MHz</th>
<th>Clock 4 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>S3</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>S4</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>S5</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
</tr>
</tbody>
</table>

When just using external clock and external frame, only DIL-switches S1 and S2 are to be set (both to position OFF). – The DIL-switches S6, S7 and S8 are not connected.
2.3 Microprocessor Section

There is a 8031 microprocessor, a 16 Kbyte EPROM, 8 Kbyte RAM and a RS232 interface on the board. The RAM is not used in this version. You can also use different types of EPROMs (8 K, 16 K, 32 K bytes). In that case you have to change a few solder straps. Further information can be found in chapter 2.7 Solder Straps.

In the microprocessor part there are two switches S1 and S2 and a DIL-switch (DIL1). Switch S1 changes the direction receive/transmit of the RS232-interface. Switch S2 performs the hardware-reset.

The microprocessor is connected via the MAX 232-IC to the RS232-interface. With the four DIL1-switches the parity is set. The DIL1-switches S1 and S2 are switched to ON. The switches S3 and S4 have the following functions:

<table>
<thead>
<tr>
<th>DIL1</th>
<th>OFF</th>
<th>ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>S3</td>
<td>no parity</td>
<td>parity</td>
</tr>
<tr>
<td>S4</td>
<td>odd parity</td>
<td>even parity</td>
</tr>
</tbody>
</table>

We only work with even parity and therefore both switches are in ON position.

The microprocessor program has an autobaud, which has to be to started first. We recommend to use only a transmission rate of 9600 Baud. All examples given refer to 9600 Baud.

Additional information can be found in chapter 3. Starting the Board.
2.4 PBC/PIC Section

The PBC or PIC has a PCM highway 0 and 1, both with highway drivers. These drivers may be optimized by using external resistors. You may connect the receive and transmit paths of highway 0 and 1 to connector CON4 (see figure 1) in using jumpers. This allows for a speech connection of subscriber 0 (SICOFI0 and SLIC0) to subscriber 1 (SICOFI1 and SLIC1). Via the connector CON3 you can connect the board to the older PBC board (STU 2050). The LED D1 indicates an interrupt from the PBC. In this case you have to check the clock and frame and you have to restart the system.

The SIP-lines SIP0 and SIP1 are connected to SICOFI 0 and 1. The SIP-line SIP3 is connected to the SLIC-connectors CON6 and CON7.

2.5 SICOFI® Section

There are two SICOFIs on the board. They are connected via the SLD-interface to the PBC.

If you have connected external hardware at the SIP-line in addition to the SICOFI, and there is a timing collision of these both circuits, a series resistor protects the SICOFI. In this case cut the solder strap near the SICOFI at the soldering side and connect the other solder point of pin 17 of the SICOFI (see figure 4 in chapter 2.7 Solder Straps), then you have added the resistor to the circuit.

All SICOFI signaling pins are connected to the pertining SLIC connectors. On board the analog input/output line have both a banana- and a BNC-plug for measurement, and they are connected to the SLIC connectors, too.
2.5.1 **SLIC Connectors CON6 and CON7 (pin-outs)**

The connectors CON6 and CON7 have 64 pins.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Connection</th>
<th>Pin</th>
<th>Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>A 1</td>
<td>Bridge to other SLIC board</td>
<td>C 1</td>
<td></td>
</tr>
<tr>
<td>A 2</td>
<td>Bridge to other SLIC board</td>
<td>C 2</td>
<td>– 12 V</td>
</tr>
<tr>
<td>A 3</td>
<td>Bridge to other SLIC board</td>
<td>C 3</td>
<td></td>
</tr>
<tr>
<td>A 4</td>
<td>Bridge to other SLIC board</td>
<td>C 4</td>
<td>+ 12 V</td>
</tr>
<tr>
<td>A 5</td>
<td>Bridge to other SLIC board</td>
<td>C 5</td>
<td></td>
</tr>
<tr>
<td>A 6</td>
<td>DIR</td>
<td>C 6</td>
<td></td>
</tr>
<tr>
<td>A 7</td>
<td>SCLK</td>
<td>C 7</td>
<td>Port 1.4</td>
</tr>
<tr>
<td>A 8</td>
<td>SIGS</td>
<td>C 8</td>
<td>Port 1.5</td>
</tr>
<tr>
<td>A 9</td>
<td>MCLK</td>
<td>C 9</td>
<td>Port 1.6</td>
</tr>
<tr>
<td>A 10</td>
<td>SYP</td>
<td>C 10</td>
<td>Port 1.7</td>
</tr>
<tr>
<td>A 11</td>
<td>SIP-wire</td>
<td>C 11</td>
<td></td>
</tr>
<tr>
<td>A 12</td>
<td>Digital ground (DGND)</td>
<td>C 12</td>
<td>Port 0.0</td>
</tr>
<tr>
<td>A 13</td>
<td>+ 5 V</td>
<td>C 13</td>
<td>Port 0.1</td>
</tr>
<tr>
<td>A 14</td>
<td>Ring AC 65 V</td>
<td>C 14</td>
<td>Port 0.2</td>
</tr>
<tr>
<td>A 15</td>
<td>– 5 V</td>
<td>C 15</td>
<td>Port 0.3</td>
</tr>
<tr>
<td>A 16</td>
<td>RESET</td>
<td>C 16</td>
<td>Port 0.4</td>
</tr>
<tr>
<td>A 17</td>
<td>– 70 V</td>
<td>C 17</td>
<td>Port 0.5</td>
</tr>
<tr>
<td>A 18</td>
<td></td>
<td>C 18</td>
<td>Port 0.6</td>
</tr>
<tr>
<td>A 19</td>
<td>– 48 V</td>
<td>C 19</td>
<td>Port 0.7</td>
</tr>
<tr>
<td>A 20</td>
<td>SIP3</td>
<td>C 20</td>
<td></td>
</tr>
<tr>
<td>A 21</td>
<td>SO1</td>
<td>C 21</td>
<td>SA</td>
</tr>
<tr>
<td>A 22</td>
<td>SO2</td>
<td>C 22</td>
<td>SB</td>
</tr>
<tr>
<td>A 23</td>
<td>SO3</td>
<td>C 23</td>
<td>SC</td>
</tr>
<tr>
<td>A 24</td>
<td>SI1</td>
<td>C 24</td>
<td>SD</td>
</tr>
<tr>
<td>A 25</td>
<td>SI2</td>
<td>C 25</td>
<td></td>
</tr>
<tr>
<td>A 26</td>
<td>SI3</td>
<td>C 26</td>
<td></td>
</tr>
<tr>
<td>A 27</td>
<td></td>
<td>C 27</td>
<td></td>
</tr>
<tr>
<td>A 28</td>
<td>Analog ground (AGND)</td>
<td>C 28</td>
<td></td>
</tr>
<tr>
<td>A 29</td>
<td>VIN (SICOFI input)</td>
<td>C 29</td>
<td></td>
</tr>
<tr>
<td>A 30</td>
<td>Analog ground (AGND)</td>
<td>C 30</td>
<td></td>
</tr>
<tr>
<td>A 31</td>
<td>VOUT (SICOFI output)</td>
<td>C 31</td>
<td></td>
</tr>
<tr>
<td>A 32</td>
<td>Analog ground (AGND)</td>
<td>C 32</td>
<td></td>
</tr>
</tbody>
</table>
2.5.2 Connector CON5

The ports 1.4 ... 1.7 of the microprocessor are used as inputs. Ports 0.0 ... 0.7 are switched by the microprocessor via a latch and may be programmed in bidirectional mode. The addresses of the latch range from 32 K to 64 K. If you want to use these 12 ports you have to modify the EPROM and write some new routines for the program.

With the connector CON5 you can cut the connection (no jumper) or set the connection (set jumper) between pins A1 ... A5 of SLIC-connectors CON6 and CON7.

<table>
<thead>
<tr>
<th>Bridge</th>
<th>Jumper</th>
</tr>
</thead>
<tbody>
<tr>
<td>A 1</td>
<td>1 - 10</td>
</tr>
<tr>
<td>A 2</td>
<td>2 - 9</td>
</tr>
<tr>
<td>A 3</td>
<td>3 - 8</td>
</tr>
<tr>
<td>A 4</td>
<td>4 - 7</td>
</tr>
<tr>
<td>A 5</td>
<td>5 - 6</td>
</tr>
</tbody>
</table>

Via this connection you may send signals from one SLIC-board to the other. In this case you need the external hardware only on a single SLIC-board. For programming external SLIC hardware you may use SIP-line 3.

2.5.3 SICOFI®-2 Adaptor

There is also an adaptor available which fits into the SICOFI sockets SIP0 and SIP1 to connect a SICOFI-2.

![SICOFI®-2 Adaptor](image_url)
2.6 Solder Straps for EPROM and SICOFI®

On the board at the soldering side there are several solder straps. These lead to the EPROM pins 26 and 27 and to the SICOFI pins 3 and 5. The EPROM type is set with solder straps.

<table>
<thead>
<tr>
<th>EPROM</th>
<th>Pin 26</th>
<th>Pin 27</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 Kbyte</td>
<td>+5 V</td>
<td>+5 V</td>
</tr>
<tr>
<td>16 Kbyte</td>
<td>A13</td>
<td>A13</td>
</tr>
<tr>
<td>32 Kbyte</td>
<td>A13</td>
<td>A14</td>
</tr>
</tbody>
</table>

Figure 3

Solder straps underneath the EPROM to set the EPROM: Left 8 K EPROM (2764), middle 16 K EPROM (27128), right 32 K EPROM (27256)

With version 3.1 of the SICOFI you may connect analog and digital ground with a solder strap between pins 3 and 5 of the SICOFI. The solder straps for the resistor in the SIP-line are close to the SICOFI (see figure 4).
2.7 Connecting SICOFI® Testboard to PCM4

For setting up a measurement system with the Wandel & Goltermann PCM4 you have access to following BNC-plugs:

- CLOCK IN
- FRAME OUT – SYP IN
- HIGHWAY 0 TRANSMIT
- HIGHWAY 0 RECEIVE
- SICOFI IN 1/2
- SICOFI OUT 1/2

The SICOFI input, output and the analog ground also have a banana-plug. It is possible to set up the system in two different timing modes. In the first mode the PCM4 (Master) sends FRAME and CLOCK signals to the SICOFI testboard.

The alternative mode uses the internal CLOCK and FRAME of the SICOFI board (Master) to synchronize the PCM4.
The PCM4 (Wandel & Goltermann) is the measurements system to measure the transfer functions from an analog line card. The system has at the digital side a PCM input and output and on the analog side a 4-wire and a 2-wire in- and output. It delivers or needs the clocks to or from the test object. When the system gets the clocks it is the slave and at the other way it is the master. Both ways are possible with our SICOFI testboard (STUT 2060). The SICOFI testboard is able to generate the clock signals (frame and SCLK) or gets them from the PCM4.

**Clock generation on the testboard**

The DIP-switches on the testboard are set to

- DIL 2.1 closed
- DIL 2.2 closed
- DIL 2.3 closed
- DIL 2.4 closed
- DIL 2.5 open

The PCM4 input for the frame is the plug 64 (external frame) on the backplane. Additionally a bridge from frame trigger output (plug 61) to external frame (plug 63) is set. The BNC2 plug (PCM highway input of testboard) has to be connected to the output of the PCM highway of the PCM4 and the input of the PCM-highway of PCM4 with the BNC1 of the SICOFI testboard.

The analog front end is connected with the analog input or output of the PCM4.

The phase shift for the PBC is PSR = 36.

**Clock generation in the PCM4**

The DIP-switches on the testboard are set to

- DIL 2.1 open
- DIL 2.2 open
- DIL 2.3 closed
- DIL 2.4 closed
- DIL 2.5 open

The PCM4 output for the frame is the plug 61 (frame trigger output) on the backplane. Additionally a bridge from frame trigger output (plug 61) to external frame (plug 63) is set. The BNC2 plug (PCM highway input) has to be connected to the output of the PCM highway of the PCM4 and the input of the PCM-highway of PCM4 with the BNC1 of the SICOFI testboard.

The analog front end is connected with the analog input or output of the PCM4.

The phase shift for the PBC is in this case PSR = 2D.
Figure 6
PCM4 Rear View
Figure 7
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:
1 PC IBM AT or compatible
1 PCM4 (Measuring set of Wandel & Goltermann)
1 SICOFI Testboard STUT 2060
1 SLIC Babyboard
### 2.8 The PCM4 Programming

The PCM4 has to be programmed as following:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCM interface</td>
<td>2Mbit/s</td>
</tr>
<tr>
<td>Digital loop</td>
<td>open</td>
</tr>
<tr>
<td>Time-slot assignment</td>
<td>32 time slots</td>
</tr>
<tr>
<td>CRC 4 frame</td>
<td>out</td>
</tr>
<tr>
<td>Code</td>
<td>NRZ (receiver and transmitter)</td>
</tr>
<tr>
<td>Output impedance</td>
<td>75 Ω unsymmetrical</td>
</tr>
<tr>
<td>Clock</td>
<td>internal 2048 kHz, when PCM4 is master</td>
</tr>
<tr>
<td></td>
<td>external 8 kHz, when PCM4 is slave</td>
</tr>
<tr>
<td>Input impedance</td>
<td>&gt; 3 kΩ</td>
</tr>
<tr>
<td>Words</td>
<td>standard</td>
</tr>
<tr>
<td>Transmit signal</td>
<td>in the addressed channel</td>
</tr>
<tr>
<td>Input</td>
<td>no mistake</td>
</tr>
<tr>
<td>Law</td>
<td>A- or μ-law</td>
</tr>
<tr>
<td>NF-input and -output</td>
<td>1</td>
</tr>
<tr>
<td>Level</td>
<td>in dBm0</td>
</tr>
<tr>
<td>Two wire (D-D)</td>
<td>open</td>
</tr>
<tr>
<td>Digital channel no.</td>
<td>time channel</td>
</tr>
<tr>
<td>PCM highway output</td>
<td>channel 1</td>
</tr>
<tr>
<td>PCM highway input</td>
<td>channel 2</td>
</tr>
</tbody>
</table>
Starting the Board

The board is started in the following way:
– Set the DIL-switches in the right position (see chapter 2.x)
– Connect the transmit and receive highways to the PCM4
– Plug the external CLOCK and FRAME (SYP) (if used)
– Connect the RS232 interface to your computer
– Provide power supply via the power supply connector CON1
– Plug your SLIC to the connectors CON6 or CON7
– Use a terminal or a personal computer with a transfer program (9600 Baud, even parity)
– Switch ON the power supply
– Press the <BLANK> key at your computer (terminal) keyboard to start the autobaud

After this your computer (terminal) shows the title screen:

```
SIEMENS
MUENCHEN      BALANSTR. 73      BAUELEMENTE
PPPPP          BBBB            CCC
P   P          B   B           C   C
P   P          B   B           C
PPPPP          BBBB            C
P                B   B           C
P                B   B           C   C
P                BBBB           CCC
```

THE KEY TO DIGITAL COMMUNICATIONS SYSTEMS
SYNTAX OF AN INPUT-LINE
WRITE: NAME = HEXDATA CR
READ: NAME CR
I-FRAME: RI PBC-COMMAND, DATA, DATA, ... CR
RR-FR.: RR CR
RQ-FR.: RQ CR

– Program the PBC, SICOFI and SLIC
The coefficients are stored in a file (XXX.byt) generated by the SICOFI coefficients program
(see the succeeding section).
4 Programming the Board

You can program the PBC, SICOFI, and SLIC via the RS232-interface to a microprocessor. Following commands are possible:

- **PSR = 2D**: phase 7 for PBC
- **CAM00 = 41**: receive CHA, SIP 0, time slot 1, highway 0
- **CAM20 = 40**: transmit CHA, SIP 0, time slot 1, highway 0
- **CAM01 = 41**: receive CHA, SIP 1, time slot 1, highway 0
- **CAM21 = 40**: transmit CHA, SIP 1, time slot 1, highway 0
- **CIW0 = 26, F4, 80**: SICOFI SIP 0, Power up, all filters OFF
- **CIW0 = 26, F4, 78**: SICOFI SIP 0, Power up, all filters ON
- **CIW1 = 26, F4, 80**: SICOFI SIP 1, Power up, all filters OFF
- **SIG0 = C0**: signaling byte to program SICOFI at SIP0

In the following the commands are treated in detail.

### 4.1 Command PSR (Phase Shift Register)

The PSR is used to shift the clock on the PCM-highways relative to the synchronization pulse (SYP). By this way different delays in a system are compensated for. The shifted clock can be used separately for transmit and receive direction and is the same on highway 0 and 1. PSR can only be written; after reset it is 00H.

<table>
<thead>
<tr>
<th>PSR-byte</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**X-shift**: clock shift on transmit highway 0 and 1, value 0 ... 7
**R-shift**: clock shift on receive highway 0 and 1, value 0 ... 7

**X**: do not care

Correspondence between the programmable values of X-shift and R-shift and the clock shift on the highway is as follows:

<table>
<thead>
<tr>
<th>X-Shift or R-Shift</th>
<th>Clock Shift</th>
<th>X-Shift or R-Shift</th>
<th>Clock Shift</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>2</td>
<td>1 0 0</td>
<td>6</td>
</tr>
<tr>
<td>0 0 1</td>
<td>3</td>
<td>1 0 1</td>
<td>7</td>
</tr>
<tr>
<td>0 1 0</td>
<td>4</td>
<td>1 1 0</td>
<td>0</td>
</tr>
<tr>
<td>0 1 1</td>
<td>5</td>
<td>1 1 1</td>
<td>1</td>
</tr>
</tbody>
</table>

For example:
If the first time slot of a frame in both directions (transmit and receive) should start at the same time as the SYP signal you have to write the value 36H in the PSR (see table).
4.2 Command CAM (Contents Addressable Memory)

A connection between subscriber and PCM-Highway is set up by programming the proper CAM-register.

\[
\text{CAM00} = \begin{array}{c|c}
\text{MS1} & \text{MS0} \\
\hline
0 & 0 \\
0 & 1 \\
1 & 0 \\
1 & 1 \\
\end{array}
\]

SIP-line 0 ... 7

0 channel A, receive direction
1 channel B, receive direction
2 channel A, transmit direction
3 channel B, transmit direction

<table>
<thead>
<tr>
<th>MS1</th>
<th>MS2</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>no transfer</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>normal transfer, highway 1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>normal transfer, highway 0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>µP-transfer</td>
</tr>
</tbody>
</table>

You have to write the following value into the lower 6 bits of the CAM-register:

<table>
<thead>
<tr>
<th>Desired</th>
<th>Input value in the</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCM-Time-Slot</td>
<td>Clock Shift</td>
</tr>
<tr>
<td>N</td>
<td>0</td>
</tr>
<tr>
<td>N</td>
<td>1</td>
</tr>
<tr>
<td>N</td>
<td>2</td>
</tr>
<tr>
<td>N</td>
<td>3</td>
</tr>
<tr>
<td>N</td>
<td>4</td>
</tr>
<tr>
<td>N</td>
<td>5</td>
</tr>
<tr>
<td>N</td>
<td>6</td>
</tr>
<tr>
<td>N</td>
<td>7</td>
</tr>
</tbody>
</table>

* PCM-highway 0, 1

For example:
channel A, SIP-line 4, transmit highway 0, clock shift 5
CAM24 = 4E\(_H\)

channel B, SIP-line 7, receive highway 1, clock shift 7
CAM17 = 89\(_H\)
4.3 Command SIGS (Signaling Strobe)

The Signaling Strobe is a programmable frame-synchronous signal, which you get at the SIGS-pin (A8) of connectors CON6 and CON7. With this signal you can drive an expansion logic for the SICOFI. As the PBC sends 16 signaling bits, and the SICOFI uses only 10, with an active SIGS the remaining 6 bits are switched to the expansion logic. The active SIGS-signal is programmed in the Signaling Configuration Register (SCR). You can write and read it; after Reset it is 00\text{H} and not active.

The SS-bit (Strobe Select):
\begin{itemize}
  \item SS = 0: Strobe via channel A and/or B
\end{itemize}

The strobe is active (high), if RS and/or XS together with AS and/or BS are set.

The next table shows the strobe as a function of the bits RS, XS, AS and BS. '1' means high level (active).

\begin{table}[h]
\begin{tabular}{cccccccc}
\hline
RS & XS & AS & BS & Transmit & ChA & ChB & Receive & ChA & ChB \\
\hline
0 & 0 & X & X & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
1 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 \\
1 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 \\
0 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\
1 & 1 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\
1 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 \\
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
X & X & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\hline
\end{tabular}
\end{table}
SS = 1: strobe via bits of the signaling byte

<table>
<thead>
<tr>
<th>SCR</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D</td>
<td>C</td>
<td>B</td>
<td>A</td>
<td>1</td>
<td>FPC</td>
<td>X</td>
</tr>
</tbody>
</table>

FPC = 1 The strobe covers 6 bits of the signaling byte. With bit 0 the strobe is always high in receive and transmit direction.

FPC = 0 The strobe covers 9 bits of the signaling byte. The strobe is always active in transmit direction with bits 2 ... 0 and in receive direction with bits 1 ... 0.

A, B, C, D set the other bit-positions, at which the strobe is active. The strobe is active in receive direction with the A-, B-, C-, D-bits being set to '1' in the SCR-register. The strobe is low in transmit direction with the A-, B-, C-, D-bits being set to '1' in the SCR-register.

**Strobe**

The strobe is used to drive an external Tri-State-Driver, which sends some bits to the SIP-line. You have to continue programming the strobe in transmit direction to avoid overlapping of both transmitters. This is valid for the following combination:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
4.4 Control Byte for CIW Command

The following description of the programming bytes is only valid for the SICOFI PEB 2060.
If the SICOFI-2 adaptor is used, you have to program the corresponding bytes for the SICOFI-
2 (PEB 2260).

There are three classes of the CIW command for the SICOFI which are defined by bits 2 and
3 in each control byte:

– NOP NORMAL OPERATION
  no status modification or data exchange
  control byte: bit 3 = 1
  bit 2 = 1

– SOP STATUS OPERATION
  contains information about the SICOFI status and use of signaling expansion logic
  control byte: bit 3 = 0
  bit 2 = 1

– COP COEFFICIENT OPERATION
  contains information about data exchange
  control byte: bit 3 = X
  bit 2 = 0

SOP and COP contain additional address information which is valid if 2 SICOFIIs are
connected to one and the same PBC port.

4.4.1 SOP Command

If the SICOFI status has to be changed, a status operation byte is transferred containing the
following information:

<table>
<thead>
<tr>
<th>AD</th>
<th>R/W</th>
<th>PU</th>
<th>TR</th>
<th>0</th>
<th>1</th>
<th>LSEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

AD  Address information which is relevant if 2 SICOFIIs are connected to one and the same
     PBC port. Here: always AD = 0

R/W  Read/write information
     Enables reading from the SICOFI or writing information to the SICOFI (read = 1, write
     = 0)

PU  Power-up/power-down
    PU = 1 Power-up (operating)
    PU = 0 Power-down (standby)

TR  Three-party conferencing
    If TR = 1, the received voice bytes of channel A and B are added

LSEL Length select
    Defines the number of the subsequent data bytes
4.4.1.1 SOP Write

If the SICOFI status has to be defined initially or changed, the SOP command looks like

```
7 0
AD 0 PU TR 0 1 LSEL
```

and the subsequent configuration bytes are written into one or both configuration registers CR1, CR2.

In this case, the meaning of LSEL is:
- 0 0 status setting is completed (no bytes following)
- 1 1 one byte will follow and is stored in CR1
- 1 0 two bytes will follow and are stored in CR2 and CR1
- 0 1 not used

Corresponding to the configuration bytes transmitted, the information contained in the configuration registers is

```
7 0
CR1 DB RZ RX RR RG TM TM TM
```

where
- DB disable B filter (DB = 1), restore B filter (DB = 0)
- RZ disable Z filter (RZ = 0), restore B filter (RZ = 1)
- RX disable X filter (RX = 0), restore B filter (RX = 1)
- RR disable R filter (RR = 0), restore B filter (RR = 1)
- RG disable G filter (RG = 0), restore B filter (RG = 1)

<table>
<thead>
<tr>
<th>Test Modes</th>
<th>DB</th>
<th>RZ</th>
<th>RX</th>
<th>RR</th>
<th>RG</th>
<th>TM</th>
<th>TM</th>
<th>TM</th>
</tr>
</thead>
<tbody>
<tr>
<td>No test mode</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>analog loop back via Z-filter</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>disable high pass</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>cut off receive path (HP active)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Not used</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Not used</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Digital loop back via B-filter</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Digital loop back via PCM-reg.</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

and

```
7 0
CR2 D C B A EL AM µ/A PCS
```
where
- D signaling pin SD is input (D = 1) or output (D = 0)
- C signaling pin SC is input (C = 1) or output (C = 0)
- B signaling pin SB is input (B = 1) or output (B = 0)
- A signaling pin SA is input (A = 1) or output (A = 0)
- EL signaling expansion logic connected (EL = 1) or not connected (EL = 0)
- AM Address Mode
  one SICOFI: AM = 1
  two SICOFIs: AM = 0; SA is input automatically
- μ/A μ-law: \( μ/A = 1 \), A-law: \( μ/A = 0 \)
- PCS Programmed B-filter coefficients (PCS = 0) or fixed coefficients for B-filter (PCS = 1)

**Note:** The power-on reset or a hardware reset via RS pin resets all CR1 bits to 0 and sets all CR2 bits to 1.

### 4.4.1.2 SOP Read

If the SICOFI status has to be evaluated, using the SOP command

```
7 0
```

<table>
<thead>
<tr>
<th>AD</th>
<th>PU</th>
<th>TR</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

the contents of CR2 and CR1 is read back to SIP. The meaning of the SOP bits is as described in the SOP write section.

### 4.4.2 COP Command

With a COP command, programmable filter coefficients can be written into or read from the coefficients RAM. With the following bytes you can write into the RAM:

<table>
<thead>
<tr>
<th></th>
<th>SICOFI A</th>
<th>SICOFI B</th>
</tr>
</thead>
<tbody>
<tr>
<td>B-filter part 1</td>
<td>03</td>
<td>83</td>
</tr>
<tr>
<td>B-filter part 2</td>
<td>0B</td>
<td>8B</td>
</tr>
<tr>
<td>B-filter delay</td>
<td>18</td>
<td>98</td>
</tr>
<tr>
<td>Z-filter</td>
<td>13</td>
<td>93</td>
</tr>
<tr>
<td>X-filter</td>
<td>23</td>
<td>A3</td>
</tr>
<tr>
<td>R-filter</td>
<td>2B</td>
<td>AB</td>
</tr>
<tr>
<td>GR-/GX-filter</td>
<td>30</td>
<td>B0</td>
</tr>
</tbody>
</table>
4.4.3 CIW Command

The CIW command writes data in the SICOFI like filter coefficients, power-up, status of the four signaling pins, number of SICOFIs at the SIP-line.

CIW0 = 26, F4, 80
    └── CR1
    └── CR2
       └── SIP0

CIW1 = 13, 20, 1D, AA, 9B, CB, 2C, 13, B4
    └── filter coefficients
       └── Z-filter coefficients following
          └── SIP1

4.4.4 CIR Command

The CIR command reads data out of the SICOFI which have been written into the SICOFI with the CIW command.

CIR0 = 66
    └── COP command to read the SICOFI status
       └── SIP-line

You can read out the filter coefficients with the following byte:

<table>
<thead>
<tr>
<th>SICOFI A</th>
<th>SICOFI B</th>
</tr>
</thead>
<tbody>
<tr>
<td>B-filter part 1</td>
<td>43</td>
</tr>
<tr>
<td>B-filter part 2</td>
<td>4B</td>
</tr>
<tr>
<td>B-filter delay</td>
<td>58</td>
</tr>
<tr>
<td>Z-filter</td>
<td>53</td>
</tr>
<tr>
<td>X-filter</td>
<td>63</td>
</tr>
<tr>
<td>R-filter</td>
<td>6B</td>
</tr>
<tr>
<td>GR-/GX-filter</td>
<td>70</td>
</tr>
</tbody>
</table>

The coefficients are followed by the values of CR2 and CR1 register.
4.5 Command SIG

With the SIG command you can write the signaling byte. This byte is used by the signaling interface of SICOFI. It has:
3 transmit signaling inputs (SI1, SI2, SI3),
3 receive signaling outputs (SO1, SO2, SO3), and
4 signaling pins (SA, SB, SC, SD), which are individually programmable as either transmit input or receive output.
The signaling field format is generally

in transmit direction

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SI1</td>
<td>SI2</td>
<td>SI3</td>
<td>SD</td>
<td>SC</td>
<td>SB</td>
<td>SA</td>
<td>SEL</td>
</tr>
</tbody>
</table>

in receive direction

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SO1</td>
<td>SO2</td>
<td>SO3</td>
<td>SD</td>
<td>SC</td>
<td>SB</td>
<td>SA</td>
<td>SEL</td>
</tr>
</tbody>
</table>

where SEL is the signaling expansion bit if EL = 1 in CR2

For the 6 different cases possible, the signaling byte format at SIP is for

<table>
<thead>
<tr>
<th>Receive Signaling Byte</th>
<th>Transmit Signaling Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case</td>
<td>Bit</td>
</tr>
<tr>
<td>1</td>
<td>A SICOFI</td>
</tr>
<tr>
<td>2</td>
<td>B SICOFI</td>
</tr>
<tr>
<td>3</td>
<td>A SICOFI</td>
</tr>
<tr>
<td>4</td>
<td>B SICOFI</td>
</tr>
</tbody>
</table>

Z High-impedance state
Y Do not care
Cases:
1. A single SICOFI connected to a single PBC port; EL = 0 (no expansion logic): SA, SB, SC, SD programmed as transmit signaling inputs.
2. A single SICOFI; EL = 1 (expansion logic provided; SA, SB, SC, SD programmed as in case 1).
3. A single SICOFI; EL = 0; SA, SB, SC, SD programmed as receive signaling outputs.
4. A single SICOFI; EL = 1; SA, SB, SC, SD programmed as in case 3.
5. Two SICOFIs connected to one and the same PBC port; SD programmed as transmit signaling input.
6. Two SICOFIs, SD programmed as receive signaling output. If two SICOFIs are connected to one and the same PBC port, no expansion logic is provided. SA is programmed as input automatically and defines the addressed SICOFI:
   - SA = 0: A SICOFI
   - SA = 1: B SICOFI

Example:

\[ \text{SIG0} = C0 \]

signaling byte

SIP-line

**4.6 Microprocessor Ports**

If you want to use the ports of the microprocessor, than you have to extend the microprocessor software and to change the EPROM.
4.7 Program Examples

a) If you want to do measurements with a PCM4 from 'Wandel & Goltermann' you may program the following example:

The PCM4 is the master. It sends the data in time slot 1 and receives from time slot 2. The SLIC is a HARRIS HC 5502A. Due to the clock shift of the PCM4 (– 1 bit) we program the clock shift with 7 to the preceding time slot. In this case:

- PSR = 2D phase 7 for PBC
- CAM00 = 41 receive ChA, SIP0, time slot 1, hw0
- CAM20 = 40 transmit ChA, SIP0, time slot 1, hw0
- CIW0 = 26, F4, 80 SICOFI power up, all filters off
- CIW0 = 13, 20, DA, CA, 2B, 23, 41, C2, 2B Z-filter
- CIW0 = 23, 50, C8, B5, 49, C2, 21, 04, 90 X-filter
- CIW0 = 2B, C0, C8, 96, C2, CA, B4, 01, 1D R-filter
- CIW0 = 03, C4, 25, 13, 3D, 6B, A9, BC, BB B-filter part 1
- CIW0 = 0B, 00, 36, D2, C2, B6, 41, 74, 2C B-filter part 2
- CIW0 = 18, 19, 11, 19 B-filter delay
- CIW0 = 30, 41, B0, 20, 92 GR-/GX-filter
- SIG0 = C0 SLIC Power up, conversation
- CIW0 = 26, F4, 78 SICOFI power up, all filters on

b) The board is the master. The PCM4 sends the data in time slot 1 and receives the data from time slot 2. The SLIC is a HARRIS HC 5502A. You have to connect the BNC-plug No. 64 of the PCM4 (external clock) to the Frame-out plug (Clock section). The parameter 3 of the PCM4 (digital generator) is programmed with 33 (external clock (8 kHz)). The shifted clock is exactly 0. In this case we have to program:

- PSR = 36 phase 0 for PBC
- CAM00 = 41 receive ChA, SIP0, time slot 1, hw0
- CAM20 = 40 transmit ChA, SIP0, time slot 2, hw0
- CIW0 = 26, F4, 80 SICOFI power up, all filters OFF
- CIW0 = 13, 20, DA, CA, 2B, 23, 41, C2, 2B Z-filter
- CIW0 = 23, 50, C8, B5, 49, C2, 21, 04, 90 X-filter
- CIW0 = 2B, C0, C8, 96, C2, CA, B4, 01, 1D R-filter
- CIW0 = 03, C4, 25, 13, 3D, 6B, A9, BC, BB B-filter part 1
- CIW0 = 0B, 00, 36, D2, C2, B6, 41, 74, 2C B-filter part 2
- CIW0 = 18, 19, 11, 19 B-filter delay
- CIW0 = 30, 41, B0, 20, 92 GR-/GX-filter
- SIG0 = C0 SLIC Power-up, conversation
- CIW0 = 26, F4, 78 SICOFI power-up, all filters ON
c) Example for communication between SICOFL at SIP0 and electronic-SLIC (HARRIS HC 5502A) and between SICOFL at SIP1 and transformer-SLIC.

CAM01 = 82 receive ChA, SIP1, time slot 1, hw1
CAM21 = 81 transmit ChA, SIP1, time slot 2, hw1
CIW0 = 26, F4, 80
CIW0 = 13, 20, 1D, AA, 9B, CB, 2C, 13, B4
CIW0 = 23, 50, 2B, AE, B1, 24, B2, 02, 42
CIW0 = 2B, 50, 9B, 26, 32, A8, 32, 1B, 22 (TRAFO-SLIC)
CIW0 = 03, 91, 22, 39, 02, 2B, C3, 22, C1
CIW0 = 0B, 00, 2A, 02, BB, 38, 12, BA, 21
CIW0 = 18, 19, 19, 11, 19
CIW0 = 30, 31, 2A, 10, 33
CIW0 = 26, F4, 78

CAM00 = 83 receive ChA, SIP0, time slot 2, hw1
CAM20 = 80 transmit ChA, SIP0, time slot 1, hw1
CIW0 = 26, F4, 80
CIW0 = 13, 20, DA, CA, 2B, 23, 41, C2, 2B (HARRIS-SLIC HC 5502A)
CIW0 = 23, 50, C8, B5, 49, C2, 21, 04, 90
CIW0 = 2B, C0, C8, 96, C2, CA, B4, 01, 1D
CIW0 = 03, C4, 25, 13, 3D, 6B, A9, BC, BB
CIW0 = 0B, 00, 36, D2, C8, 32, 74, 2C
CIW0 = 18, 19, 19, 11, 19
CIW0 = 30, 41, B0, 20, 92
SIG0 = C0
CIW0 = 26, F4, 78
4.8 Programming Differences of PEB 2060 and PEB 2260

If the SICOFI testboard is used with the SICOFI-2 adaptor the programming commands are different (refer to the SICOFI and SICOFI-2 datasheet).

The programming bytes for the different SICOFI filters remain the same with the exception of the gain programming GX and GR.

SICOFI PEB 2060:

\[ \text{CIW0} = 30, \text{GR}, \text{GR}, \text{GX}, \text{GX} \] for GR and GX programming

SICOFI-2 PEB 2260:

\[ \text{CIW0} = 30, \text{GX}, \text{GX}, \text{GX}, 80, 80 \] for GX programming

\[ \text{CIW0} = 3A, \text{GR}, \text{GR} \] for GR programming

If you want to use our SICOFI-SLIC programming examples please note that the programming of the signaling is only valid for the SICOFI PEB 2060. If you use the SICOFI-2 PEB 2260 the command for the signaling must be changed.
5 Appendix

5.1 List of Replaceable Parts

IC 1 TL 7702  IC 11 SAB 27128
IC 2 μP 8031  IC 12 PEB 2050
IC 3 74LS241  IC 13 74LS157
IC 4 74LS155  IC 14 74LS161
IC 5 MAX 232  IC 15 74LS04
IC 6 SAB 8282  IC 16 74LS112
IC 7 74LS157  IC 17 HM 6264
IC 8 74LS241  IC 18 PEB 2060
IC 9 74HC125  IC 19 PEB 2060
IC 10 74LS393  IC 20 74LS245

Resistors
$R_1, R_3, R_4$  10 kΩ
$R_2$  27 kΩ
$R_5, R_6$  3.3 kΩ

Dekade of resistors
$R_{a1}, R_{a2}, R_{a3}, R_{a4}$  4.7 kΩ

Capacitors
$C_1, C_{12} \ldots C_{18}, C_{27}, C_{28}, C_{40}, C_{41}$  100 nF
$C_2, C_4, \ldots C_8, C_{25}, C_{35}, C_{36}$  1 μF
$C_3$  27 pF
$C_{21} \ldots C_{24}$  22 μF

Others
S1  Reset switch
S2  dual DIL switch
DIL 1  8 pole DIL-switch
DIL 2  16 pole DIL-switch
Bu0, Bu1 \ldots Bu4, Bu6, Bu8, Bu10, Bu12  BNC-plugs
Bu5, Bu7, Bu9, Bu11, Bu13, Bu14  Banana plugs
CON1  power supply connector
CON2  D-SUB connector 25 pins
CON3  D-SUB connector 37 pins
CON6, CON7  64 pins connector male (or female)
5.2 Floor Plan of the SICOFi® Testboard
5.3 Circuit Diagram of the SiCOFI® - 2 Adaptor

![Circuit Diagram](image-url)
## Contents

<table>
<thead>
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</tr>
</tbody>
</table>
1 Introduction

The development of Analog Subscriber Line Cards for voice transmission in ISDN networks poses enormous efforts to the engineer in implementing the very strict requirements of the specifications to the system, thus problems that cannot be solved by experience must be settled by lengthy trial and error procedures.

The SICOFI-2 Module SIPB 5135 helps in developing the analog line card.

In an ISDN the analog line card consists of a codec filter circuit and an analog part comprising a hybrid and the line drivers and means for ringing and testing. With the SICOFI-2 integrated circuit the SICOFI-2 Module already provides a ready-to-use codec filter and interfaces to two subscriber line circuits (SLICs). Thus this board offers the outstanding advantage of enabling immediate starting with experiments on the analog line card, and to measure very comfortably various transmission functions using the PCM4 measuring device of Wandel & Goltermann.

The integration of the SICOFI-2 Module into the SIPB-system using the Menu Software renders the development and the adaptation of a voice transmission path to an ISDN to simply connecting a single board.

2 Features

- Compatible to SIPB 5000 userboard system
- Two interfaces for connecting customer specific SLIC boards
- Enables measurements of various transfer functions of the SLMA such as
  - return loss
  - gain
  - transhybrid loss
  - noise
  - gain tracking
- Same SLIC connector as on the SICOFI Testboard (STUT 2060)
- Operating in two different interfaces modes SLD or IOM-2
3 Use

The SICOFI-2 Module SIPB 5135 is developed to be used in connection with the Line Card Module SIPB 5121. If at the secondary side of the Line Card Module a PCM4 Adaptor SIPB 5311 is connected, a very useful development and testing tool for the analog line card results (figure 1).

Using a PCM4 of Wandel & Goltermann the following measurements are possible:

- return loss
- level in A/D- and D/A-direction
- gain tracking in A/D- and D/A-direction
- noise in A/D- and D/A-direction
- echo return loss

![Figure 1](image)

**Figure 1**

**Measuring Set-Up**

With very sensitive noise measurements power (5 V) may be supplied externally to the SICOFI-2 Board.
4 Circuitry

4.1 Block Diagram

Figure 2
Block Diagram of the SICOFL®-2 Module
4.2 Connector Pin-Outs

4.2.1 Service Access Connector SAC (ST2)

![Service Access Connector SAC](ITC02533)

Figure 3
Service Access Connector SAC

<table>
<thead>
<tr>
<th>Pin</th>
<th>Use</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>–</td>
<td>Not connected</td>
</tr>
<tr>
<td>2</td>
<td>O</td>
<td>Identifier (SLD = “0”, IOM = “1”)</td>
</tr>
<tr>
<td>3</td>
<td>I</td>
<td>RESET</td>
</tr>
<tr>
<td>4</td>
<td>O</td>
<td>DU (IOM mode)</td>
</tr>
<tr>
<td></td>
<td>I/O</td>
<td>SIP4 (SLD mode)</td>
</tr>
<tr>
<td>5</td>
<td>I</td>
<td>DD (IOM mode)</td>
</tr>
<tr>
<td></td>
<td>I/O</td>
<td>SIP0 (SLD mode)</td>
</tr>
<tr>
<td>6</td>
<td>I</td>
<td>FSC</td>
</tr>
<tr>
<td>7</td>
<td>I</td>
<td>DCL</td>
</tr>
<tr>
<td>8</td>
<td>I</td>
<td>+ 5 V</td>
</tr>
<tr>
<td>9</td>
<td>I</td>
<td>GND</td>
</tr>
</tbody>
</table>

4.2.2 SLIC Connector SLC (ST1, ST4)

To connect the SLICs, a 64-pin connector is used.

![SLIC Connector SLC](ITC02535)

Figure 4
SLIC Connector SLC
## Pin Definition and Function

<table>
<thead>
<tr>
<th>Pin</th>
<th>Row</th>
<th>Use</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A</td>
<td>I/O</td>
<td>Bridge to other SLIC connector</td>
</tr>
<tr>
<td>2</td>
<td>A</td>
<td>I/O</td>
<td>Bridge to other SLIC connector</td>
</tr>
<tr>
<td>3</td>
<td>A</td>
<td>I/O</td>
<td>Bridge to other SLIC connector</td>
</tr>
<tr>
<td>4</td>
<td>A</td>
<td>I/O</td>
<td>Bridge to other SLIC connector</td>
</tr>
<tr>
<td>5</td>
<td>A</td>
<td>I/O</td>
<td>Bridge to other SLIC connector</td>
</tr>
<tr>
<td>6</td>
<td>A</td>
<td>O</td>
<td>FSC</td>
</tr>
<tr>
<td>7</td>
<td>A</td>
<td>O</td>
<td>CLK 512 kHz</td>
</tr>
<tr>
<td>11</td>
<td>A</td>
<td>I/O</td>
<td>SIP4 (only in SLD – interface mode)</td>
</tr>
<tr>
<td>12</td>
<td>A</td>
<td>O</td>
<td>GND</td>
</tr>
<tr>
<td>13</td>
<td>A</td>
<td>O</td>
<td>+ 5 V</td>
</tr>
<tr>
<td>14</td>
<td>A</td>
<td>O</td>
<td>RING AC 65 V</td>
</tr>
<tr>
<td>15</td>
<td>A</td>
<td>O</td>
<td>– 5 V</td>
</tr>
<tr>
<td>16</td>
<td>A</td>
<td>O</td>
<td>RESET (high active)</td>
</tr>
<tr>
<td>17</td>
<td>A</td>
<td>O</td>
<td>– 70 V</td>
</tr>
<tr>
<td>19</td>
<td>A</td>
<td>O</td>
<td>– 48 V</td>
</tr>
<tr>
<td>20</td>
<td>A</td>
<td>O</td>
<td>SIP0 (only in SLD – interface mode)</td>
</tr>
<tr>
<td>21</td>
<td>A</td>
<td>O</td>
<td>SO1 (SLD) / C1 (IOM-2)</td>
</tr>
<tr>
<td>22</td>
<td>A</td>
<td>O</td>
<td>SO2 (SLD) / C2 (IOM-2)</td>
</tr>
<tr>
<td>23</td>
<td>A</td>
<td>O</td>
<td>SO3 (SLD) / C3A (IOM-2)</td>
</tr>
<tr>
<td>24</td>
<td>A</td>
<td>I</td>
<td>SI1 (SLD) / I1 (IOM-2)</td>
</tr>
<tr>
<td>25</td>
<td>A</td>
<td>I</td>
<td>SI2 (SLD) / CI1 (IOM-2)</td>
</tr>
<tr>
<td>26</td>
<td>A</td>
<td>I</td>
<td>SI3 (SLD) / CI2 (IOM-2)</td>
</tr>
<tr>
<td>28</td>
<td>A</td>
<td>O</td>
<td>GND analog</td>
</tr>
<tr>
<td>29</td>
<td>A</td>
<td>I</td>
<td>VIN (SICOFI analog input)</td>
</tr>
<tr>
<td>30</td>
<td>A</td>
<td>O</td>
<td>GND analog</td>
</tr>
<tr>
<td>31</td>
<td>A</td>
<td>O</td>
<td>VOUT (SICOFI analog output)</td>
</tr>
<tr>
<td>32</td>
<td>A</td>
<td>O</td>
<td>GND analog</td>
</tr>
<tr>
<td>2</td>
<td>C</td>
<td>O</td>
<td>– 12 V</td>
</tr>
<tr>
<td>4</td>
<td>C</td>
<td>O</td>
<td>+ 12 V</td>
</tr>
<tr>
<td>21</td>
<td>C</td>
<td>I/O</td>
<td>SB (SLD) / CI1 (IOM-2)</td>
</tr>
<tr>
<td>22</td>
<td>C</td>
<td>I/O</td>
<td>CI2 (IOM-2)</td>
</tr>
</tbody>
</table>
Bridges between both SLIC connectors are provided at the SICOFL-2 Module to allow for direct signaling between the SLICs. These connections are established by jumpers.

The signaling pins CI1 and CI2 are connected to pins C21 and C22 or to A25 and A26 respectively. Selection is done by DIL switch S. This selection is needed to provide additional input pins at row A when operating in the IOM-2 interface mode.

4.2.3 Power Supply Plug PSC (ST3)

![Power Supply Connector PSC](image)

**Figure 5**
Power Supply Connector PSC

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+ 5 V</td>
</tr>
<tr>
<td>2</td>
<td>Digital Ground (DGND)</td>
</tr>
<tr>
<td>3</td>
<td>+ 12 V</td>
</tr>
<tr>
<td>4</td>
<td>Analog Ground (AGND)</td>
</tr>
<tr>
<td>5</td>
<td>– 48 V</td>
</tr>
<tr>
<td>6</td>
<td>Battery Ground (BGND)</td>
</tr>
<tr>
<td>7</td>
<td>– 5 V</td>
</tr>
<tr>
<td>8</td>
<td>Ring Ground (RGND; not used)</td>
</tr>
<tr>
<td>9</td>
<td>– 12 V</td>
</tr>
<tr>
<td>10</td>
<td>Ring signal (not used)</td>
</tr>
<tr>
<td>11</td>
<td>Not used</td>
</tr>
</tbody>
</table>
4.3 List of Replaceable Parts

<table>
<thead>
<tr>
<th>Component</th>
<th>Type/Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>PEB 2260</td>
</tr>
<tr>
<td>IC2</td>
<td>74 HC 147</td>
</tr>
<tr>
<td>IC3</td>
<td>74 HC 4052</td>
</tr>
<tr>
<td>IC4</td>
<td>74 HC 4052</td>
</tr>
<tr>
<td>IC5</td>
<td>74 HC 4053</td>
</tr>
<tr>
<td>IC6</td>
<td>74 HC 4316</td>
</tr>
<tr>
<td>IC7</td>
<td>74 HC 4053</td>
</tr>
<tr>
<td>IC8</td>
<td>74 HC 93</td>
</tr>
<tr>
<td>IC9</td>
<td>74 HC 4053</td>
</tr>
<tr>
<td>IC10</td>
<td>74 HC 04</td>
</tr>
<tr>
<td>IC11</td>
<td>74 HC 125</td>
</tr>
<tr>
<td>IC12</td>
<td>74 HC 126</td>
</tr>
<tr>
<td>IC13</td>
<td>74 HC 00</td>
</tr>
<tr>
<td>T1, T2</td>
<td>BC 237A</td>
</tr>
<tr>
<td>D1, D2</td>
<td>1 N 4007</td>
</tr>
<tr>
<td>$R_1 \ldots R_7$</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>$R_8$</td>
<td>$7 \times 10$ kΩ</td>
</tr>
<tr>
<td>$C_1, C_2$</td>
<td>10 μF</td>
</tr>
<tr>
<td>$C_3, C_4$</td>
<td>10 nF</td>
</tr>
<tr>
<td>$C_5$</td>
<td>100 nF</td>
</tr>
<tr>
<td>S1</td>
<td>10 × 1</td>
</tr>
<tr>
<td>S2 – S5</td>
<td>DIP 8 pol.</td>
</tr>
<tr>
<td>Relay K1</td>
<td>DS4E-SL2 5 V</td>
</tr>
<tr>
<td>Relay K2</td>
<td>DS2E-SL2 5 V</td>
</tr>
</tbody>
</table>
Figure 6
Floor Plan of the SICOFI®-2 Module
5 Operational Information

5.1 Configuring the SICOFI®-2 Module

Before power is applied to the SICOFI-2 Module, it has to be configured by means of switch and jumper settings for a given application.

Possible configurations of the SICOFI-2 Module are:

– selecting the interface mode (SLD- or IOM modes)
– selecting the signaling pins at the SLIC connectors SLC.

Selection of the interface mode is done by means of rotary switch S1, and of the signaling pins in using the DIP switch S2.

Switch S1

The 10-position rotary switch S1 selects the interface modes SLD or IOM. An identifier signal is transmitted to the configuration register of the Line Card Module for indicating the actual interface mode. This configuration register is readable by the Menu Software.

In the IOM mode, 9 different modes are possible. Only a single IOM mode works at a 512 kHz clock frequency (slow IOM). All other IOM modes (fast IOM) operate at 4096 MHz, and 8 different channels at the interface are selectable. All existing possibilities are summarized in the following table.

<table>
<thead>
<tr>
<th>S1 Position</th>
<th>Interface Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SLD mode</td>
</tr>
<tr>
<td>1</td>
<td>IOM (DCL = 512 kHz)</td>
</tr>
<tr>
<td>2</td>
<td>IOM channel 0 (DCL = 4096 kHz)</td>
</tr>
<tr>
<td>3</td>
<td>IOM channel 1 (DCL = 4096 kHz)</td>
</tr>
<tr>
<td>4</td>
<td>IOM channel 2 (DCL = 4096 kHz)</td>
</tr>
<tr>
<td>5</td>
<td>IOM channel 3 (DCL = 4096 kHz)</td>
</tr>
<tr>
<td>6</td>
<td>IOM channel 4 (DCL = 4096 kHz)</td>
</tr>
<tr>
<td>7</td>
<td>IOM channel 5 (DCL = 4096 kHz)</td>
</tr>
<tr>
<td>8</td>
<td>IOM channel 6 (DCL = 4096 kHz)</td>
</tr>
<tr>
<td>9</td>
<td>IOM channel 7 (DCL = 4096 kHz)</td>
</tr>
</tbody>
</table>
5.1.1 SLD Interface Mode

In the SLD interface mode the pertining identifier signal is logical "0". The SIP-line 4 is connected to the SICOFI-2. The SIP-line 0 is connected to the SLIC connectors 1 and 2. In the SLD interface mode the DIP-switches have no function (don’t care).

5.1.2 IOM® Interface Mode

There are two different timing modes, 512 kHz (slow IOM) and 4096 kHz (fast IOM). In both modes the identifier is logical "1". Both bidirectional pins CI1 and CI2 of both SICOFI channels (A and B) are switchable between row A and C of the SLIC connector. This is necessary, because some SLICs have more signaling outputs at the connector row A than the SICOFI-2 board has inputs. Selection of the signaling paths is described in the following table 1.

DIP Switch S2

The module has four DIP-switches to select the pin assignment at the SLIC-connector. Selection is only possible in the IOM mode and affects the two bidirectional pins CI1A/B and CI2A/B of the SICOFI-2 Board.

Table 1
DIP Switch Settings for Pin Assignment of CI1A/B and CI2A/B

<table>
<thead>
<tr>
<th>DIP – Switch</th>
<th>Pin – Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>S2</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
</tr>
</tbody>
</table>

X = open, high impedance
5.2 Programming

Being in the **IOM interface mode**, the clock generator, the interface mode, and the EPIC configuration are programmed first. Then the SICOFI-2 is to follow. The corresponding track files for programming the EPIC and SICOFI-2 are found in **chapter 6**.

After this procedure the system is ready for measuring the transfer functions using the PCM4.

5.3 Power Supply

The PC does not provide all necessary voltages to supply the connected boards accordingly. That is why the SICOFI-2 Module is equipped with a connector for additional external power supply.

The voltage + 5 V is selectable internal or external by jumper J1. External 5 V power supply is choosen if sensitive noise measurements are done. With all other measurements the internal voltage source is used.
# Glossary

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARCOFI®</td>
<td>Audio Ringing COdec FIltter</td>
</tr>
<tr>
<td>B</td>
<td>64 kbit/s voice and data channel not frame oriented</td>
</tr>
<tr>
<td>D</td>
<td>16 kbit/s packetized data and control transmission channel</td>
</tr>
<tr>
<td>DD</td>
<td>Data Downstream (at IOM interface)</td>
</tr>
<tr>
<td>DIR</td>
<td>Direction signal (same as FSC)</td>
</tr>
<tr>
<td>DTMF</td>
<td>Dual Tone Multi Frequency</td>
</tr>
<tr>
<td>DU</td>
<td>Data Upstream (at IOM interface)</td>
</tr>
<tr>
<td>EPIC®</td>
<td>Extended PCM Interface Controller</td>
</tr>
<tr>
<td>FSC</td>
<td>Frame Signal</td>
</tr>
<tr>
<td>ICC</td>
<td>ISDN Communication Controller</td>
</tr>
<tr>
<td>IEC-Q</td>
<td>ISDN Echo Cancellation circuit 2B1Q</td>
</tr>
<tr>
<td>IOM®</td>
<td>ISDN Oriented Modular</td>
</tr>
<tr>
<td>IOS</td>
<td>IOM Software</td>
</tr>
<tr>
<td>ISAC®-S</td>
<td>ISDN Subscriber Access Controller on S-bus</td>
</tr>
<tr>
<td>ISDN</td>
<td>Integrated Services Digital Network</td>
</tr>
<tr>
<td>LT/S</td>
<td>Line Termination Simulator</td>
</tr>
<tr>
<td>PC</td>
<td>Personal Computer</td>
</tr>
<tr>
<td>PCM</td>
<td>Pulse Code Modulation</td>
</tr>
<tr>
<td>S</td>
<td>Double wire pair (2 × B + D)</td>
</tr>
<tr>
<td>SAC</td>
<td>Service Access Connector</td>
</tr>
<tr>
<td>SICOFI®</td>
<td>Signal COdec FIltter</td>
</tr>
<tr>
<td>SIP</td>
<td>Serial Interface Port</td>
</tr>
<tr>
<td>SLC</td>
<td>SLIC connector</td>
</tr>
<tr>
<td>SLD</td>
<td>Subscriber Line Digital</td>
</tr>
<tr>
<td>SLIC</td>
<td>Subscriber line interface card</td>
</tr>
<tr>
<td>TE</td>
<td>Terminal Equipment</td>
</tr>
<tr>
<td>2B1Q</td>
<td>Transmission code requiring 120-kHz bandwidth</td>
</tr>
</tbody>
</table>
7 Menu Software Track Files

This section contains track files for connecting the Line-Card Module and the SICOFI-2. The Line-Card Module is configured just by software. The pertinent track file LISISLD.TRK contains the Line Card configuration, when the SICOFI-2 board is operated in the **SLD interface mode**. When working in the **IOM mode** (4096 kHz), the correct track file is LISIIOM2.TRK.

7.1 Track Files for SLD Interface Mode

LISISLD.TRK

```
C *****************************************
C                 lc_sld2
C *****************************************
C application: initialization of the
C              line card module
C              for an sld architecture
C additional modules: sicofi2 board
C                     (sipb 5135)
C
C configuration:
C pcm interface:  4 hws with 32 ts each
C cfi interface:  8 bi.ports with 8 ts
C                  each (8 sld lines)
C
C configuration of the lc module:
C config register bits:
C id,cks/tc2/tc1/tc0/dch/dma/cts/res
C clock mode 7 (xtal 2048 khz)
C * reset of on board devices
C * cks=1  (3rd slot may be occupied by
C an audio module v2.0)
W /LINECA/CONFIG/CONFIG/CONFIG F1
W /LINECA/CONFIG/CONFIG/CONFIG F0
C
C configuration of the pcm interface:
C * pcm mode 0, single clock rate
C * pfs evaluated with falling edge
C * no comparison function
W /LINECA/EPIC/PCMCFI/PMOD 00
C * pcm bit number is 256
W /LINECA/EPIC/PCMCFI/PBNR FF
C * pcm offset is 2 bits (pfs marks
C bit 5 of ts 0) in up and downstream
C direction
```
W /LINECA/EPIC/PCMCFI/POFD EF
W /LINECA/EPIC/PCMCFI/POFU 17
C * transmit with rising edge, receive
C with falling edge of pcl
W /LINECA/EPIC/PCMCFI/PCSR 01
C
C configuration of the cfi interface:
C * cfi mode 3, clock source: pcl/pfs
C * pfs evaluated with falling edge
C * prescaler = 1
W /LINECA/EPIC/PCMCFI/CMD1 2C
C * fsc output: fc mode 6
C * dc output: single rate
C * xmit rising, rec falling edge
W /LINECA/EPIC/PCMCFI/CMD2 C0
C * cfi bit number is 64
W /LINECA/EPIC/PCMCFI/CBNR 3F
C * pfs marks cfi ts0, bit7
C * no shift between xmit and rec
W /LINECA/EPIC/PCMCFI/CTAR 02
W /LINECA/EPIC/PCMCFI/CBSR 20
C * subchannel position: 64kbps=bits7.0
C                        32kbps=bits7.4
C                        16kbps=bits7.6
W /LINECA/EPIC/PCMCFI/CSCR 00
C
C initialization of cm ctrl field:
C * cm reset mode
W /LINECA/EPIC/MARSCR/OMDR 00
C * ff is copied to all positions of
C * the cm ctrl field
W /LINECA/EPIC/MARSCR/OMDR FF
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MACR 70
C
C cfi configuration for sld:
C * cm init mode
W /LINECA/EPIC/MARSCR/OMDR 80
C cfi time slots 2 and 3 of port 4 are
C programmed as downstream feature
C control and signaling channels,
C time slots 6 and 7 as upstream
C feature ctrl and signaling channels
C cfi ts 0-7 of port 4 represent thus
C sld port 4 (amc pin 10c)
C * ts 2 downstream:
C sig value ff is transmitted
W /LINECA/EPIC/MARSCR/OMDR FF
W /LINECA/EPIC/MARSCR/MAAR 18
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 3 downstream:
W /LINECA/EPIC/MARSCR/OMDR 00
W /LINECA/EPIC/MARSCR/MAAR 19
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 6 upstream:
C ff is init value for sig receive
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR B8
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 7 upstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR B9
W /LINECA/EPIC/MARSCR/MACR 7B
C
C * pcm status is
R /LINECA/EPIC/MARSCR/STAR 05
C * not synchronized (pss=0)
C
C setting epic to normal mode
W /LINECA/EPIC/MARSCR/OMDR C0
R /LINECA/EPIC/MARSCR/ISTA 08
R /LINECA/EPIC/MARSCR/STAR 25
C pcm status: synchronized (pss=1)
C
C initialization of the pcm tristate
C field, all ch. to high impedance
W /LINECA/EPIC/MARSCR/MADR 00
W /LINECA/EPIC/MARSCR/MACR 68
C
C activation epic:
C * normal mode, pcm and cfi active
C * cfi output drivers push-pull
C * mf ch. handshake protocol disabled
W /LINECA/EPIC/MARSCR/OMDR E2
C
C mask of idecl interrupts:
W /LINECA/IDEC/COMMON/VISM 0F
C
C programming of sicofi2:
C power down, 3bytes will follow:
W /LINECA/EPIC/MCHSTR/MFFIFO 05
C transmit signaling bits to tristate:
W /LINECA/EPIC/MCHSTR/MFFIFO 10
C tone generator off
W /LINECA/EPIC/MCHSTR/MFFIFO 00
C all filters off, a-law, sb input:
W /LINECA/EPIC/MCHSTR/MFFIFO 00
C address for sld port 4:
W /LINECA/EPIC/MCHSTR/MFSAR 0C
C transmit command:
W /LINECA/EPIC/MCHSTR/CMDR 04
R /LINECA/EPIC/MCHSTR/ISTA 20
C mffi interrupt: fc transfer complete
C
C read back from sicofi:
R /LINECA/EPIC/MCHSTR/STAR 25
C mffifo: empty and may be written
C read back command for sicofi:
C power up, read back cr2, cr1:
W /LINECA/EPIC/MCHSTR/MFFIFO 66
C address of sld port 4, 8 bytes are
C expected
W /LINECA/EPIC/MCHSTR/MFSAR 8C
C transmit+receive same line command:
W /LINECA/EPIC/MCHSTR/CMDR 0C
R /LINECA/EPIC/MCHSTR/ISTA 20
C mffi interrupt: fc transfer complete
R /LINECA/EPIC/MCHSTR/STAR 26
C mffifo is not empty and may be read
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/MCHSTR/STAR 26
C mffifo is not empty and may be read
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 26
R /LINECA/EPIC/MCHSTR/MFFIFO DF
C nop command received i.e. no further
C bytes will follow!
C reset mffifo:
W /LINECA/EPIC/MCHSTR/CMDR 01
R /LINECA/EPIC/MCHSTR/STAR 25
C mffifo empty and may be written
C
digital loop back via pcm-register
C in sicofi2 b1 channel:
W /LINECA/EPIC/MCHSTR/MFFIFO 25
W /LINECA/EPIC/MCHSTR/MFFIFO 11
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFSAR 0C
W /LINECA/EPIC/MCHSTR/CMDR 04
R /LINECA/EPIC/MCHSTR/ISTAR 20
C
transmission of idle code "aa" in b1
W /LINECA/EPIC/MARSCR/MADR AA
W /LINECA/EPIC/MARSCR/MAAR 08
W /LINECA/EPIC/MARSCR/MACR 79
C up ch. setup for b1 receive:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR 79
C reading received b1 value:
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR C8
R /LINECA/EPIC/MARSCR/MADR AA
C change value to "12":
W /LINECA/EPIC/MARSCR/MADR 12
W /LINECA/EPIC/MARSCR/MAAR 08
W /LINECA/EPIC/MARSCR/MACR 48
C reading received value:
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR C8
R /LINECA/EPIC/MARSCR/MADR 12
C
C removing digital pcm loop:
W /LINECA/EPIC/MCHSTR/MFFIFO 25
W /LINECA/EPIC/MCHSTR/MFFIFO 10
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFSAR 0C
W /LINECA/EPIC/MCHSTR/CMDR 04
R /LINECA/EPIC/MCHSTR/ISTA 20
C
C transmission of idle codes in pcm
time slots 0 and 31 of port0:
C * "99" in ts 0:
W /LINECA/EPIC/MARSCR/MADR 99
W /LINECA/EPIC/MARSCR/MAAR 80
W /LINECA/EPIC/MARSCR/MACR 08
C * ts 0 to low impedance:
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 80
W /LINECA/EPIC/MARSCR/MACR 0F
W /LINECA/EPIC/MARSCR/MACR 60
C * "88" in ts 31:
W /LINECA/EPIC/MARSCR/MADR 88
W /LINECA/EPIC/MARSCR/MAAR F9
W /LINECA/EPIC/MARSCR/MACR 08
C * ts 31 to low impedance:
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR F9
W /LINECA/EPIC/MARSCR/MACR 60
C
C switching of b channels between sld
and pcm interface:
C (u=upstream, d=downstream)
C
C * u: sip4, b1 to pcm port0, ts1:
W /LINECA/EPIC/MARSCR/MADR 81
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR 71
C * pcm port0, ts1 to low impedance:
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 81
W /LINECA/EPIC/MARSCR/MACR 60
C * d: pcm port0, ts1 to sip4, b1:
W /LINECA/EPIC/MARSCR/MADR 01
C the connection sld b1 <-> pcm ts 1
C is established, a loop back can be
C realized by a short circuit at sac
C (pins 6 and 7) or by using the pcm
C test loop bit (pt1) in omdr:
W /LINECA/EPIC/MARSCR/OMDR F2
C removing the test loop:
W /LINECA/EPIC/MARSCR/OMDR E2
C
C transmission of signaling byte to
C subscriber:
C write value in madr (e.g. 34h)
W /LINECA/EPIC/MARSCR/MADR 34
C write subscr. address into maar
C (e.g. 18h for sip4)
W /LINECA/EPIC/MARSCR/MAAR 18
C write moc=1001 in macr:
W /LINECA/EPIC/MARSCR/MACR 48
C change value to "00":
W /LINECA/EPIC/MARSCR/MADR 00
W /LINECA/EPIC/MARSCR/MAAR 18
W /LINECA/EPIC/MARSCR/MACR 48

7.2 Track File for Fast IOM® Interface Mode

LISIOM2.TRK
C *********************************************
C                     lc_iom2
C *********************************************
C application: initialization of the
C              line card module
C              for an iom2 line card
C
C setup: line card module sipb 5121
C optional: s-access or layer-1
C modules in 3rd amc slot and/
C or external layer-1 modules
C connected to sac
C for the configuration of the
C additional modules please
C refer to the pertaining
C module descriptions
C the layer-1 modules should be
C set to lt mode, iom2 mode
C with an appropriate iom chan.
assignment as indicated
below

note: this track file exists also in
a non commented version:
nc_iom2

iom2 channel assignment:
* ch0: dig. subsc. decentral d
* ch1: dig. subsc. central d
* ch2: dig. subsc. mixed d
* ch3: analog subscriber (sicof12)

interface characteristics:
pcm interface: 2 hws with 64 ts each
cfi interface: 4 hws with 32 ts each

configuration of the lc module:
config register bits:
id,cks/tc2/tc1/tc0/dch/dma/cts/res
* clock mode 6 (xtal 4096khz)
* reset of on board devices
* cks=0: 3rd slot may be s-access
or p-access module
W /LINECA/CONFIG/CONFIG/CONFIG 61
W /LINECA/CONFIG/CONFIG/CONFIG 60
* note: if 3rd slot should be layer-1
module please program:
  config e1
  config e0

configuration of the pcm interface:
* pcm mode 1, single clock rate
* pfs evaluated with falling edge
* port assignment: port0=txd0,rxd0
  port1=txd2,rxd3
* no comparison function
W /LINECA/EPIC/PCMCFI/PMOD 44
* pcm bit number is 512
W /LINECA/EPIC/PCMCFI/PBNR FF
* no pcm offset, output with rising,
* input with falling edge
W /LINECA/EPIC/PCMCFI/POFD F0
W /LINECA/EPIC/PCMCFI/POFU 18
W /LINECA/EPIC/PCMCFI/PCSR 45

configuration of the cfi interface:
* cfi mode 0, clock source: pcl/pfs
* pfs evaluated with falling edge
* prescaler = 1
W /LINECA/EPIC/PCMCFI/CMD1 20
C * fsc output: fc mode 6
C * dcl output: double rate
C * xmit rising, rec falling edge
W /LINECA/EPIC/PCMCFI/CMD2 D0
C * cfi bit number is 256
W /LINECA/EPIC/PCMCFI/CBNR FF
C * pfs marks cfi ts31, bit1
W /LINECA/EPIC/PCMCFI/CTAR 02
C * no shift between xmit and rec
W /LINECA/EPIC/PCMCFI/CBSR 00
C * subchannel position: 64kbps=bits7.0
C 32kbps=bits7.4
C 16kbps=bits7.6
W /LINECA/EPIC/PCMCFI/CSCR 00
C
C initialization of cm ctrl field:
C * cm reset mode
W /LINECA/EPIC/MARSCR/OMDR 00
C * ff is copied to all positions of
C * the cm ctrl field
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MACR 70
C
C cfi configuration for iom2:
C * cm init mode
W /LINECA/EPIC/MARSCR/OMDR 80
C
C cfi time slots 2 and 3 of port 0
C are programmed as monitor and c/i
C channels, decentral d ch. handling
C (d ch. not switched to pcm)
C cfi ts 0-3 represent thus iom2 ch.0
C with b1, b2, monitor and d/ci/mr,mx
C * ff is copied to all addressed
C * positions of the cm data field
W /LINECA/EPIC/MARSCR/MADR FF
C * ts 2 downstream:
W /LINECA/EPIC/MARSCR/MAAR 08
W /LINECA/EPIC/MARSCR/MACR 78
C * ts 3 downstream:
W /LINECA/EPIC/MARSCR/MAAR 09
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 2 upstream:
W /LINECA/EPIC/MARSCR/MAAR 08
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 3 upstream:
W /LINECA/EPIC/MARSCR/MAAR 89
W /LINECA/EPIC/MARSCR/MACR 70
C
C cfi time slots 6 and 7 of port 0 are
C programmed as monitor and c/i
C channels, central d ch. handling
C (d ch. is switched to pcm port 0,
C ts 5, bits 1..0 in up and downstream
C direction
C cfi-ts 4-7 represent thus iom2 ch. 1
C * ts 6 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 18
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 7 downstream:
W /LINECA/EPIC/MARSCR/MADR 09
W /LINECA/EPIC/MARSCR/MAAR 19
W /LINECA/EPIC/MARSCR/MACR 74
C * ts 6 upstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 98
W /LINECA/EPIC/MARSCR/MACR 78
C * ts 7 upstream:
W /LINECA/EPIC/MARSCR/MADR 89
W /LINECA/EPIC/MARSCR/MAAR A9
W /LINECA/EPIC/MARSCR/MACR 75
C

C cfi time slots 10 and 11 of port 0
C are programmed as monitor and c/i
C channels, mixed d ch. handling
C upstream the d ch. is switched to
C pcm port 0, ts 5, bits 3..2
C downstream the d ch. is not switched
C directly to cfi port 0, ts 11 but
C is switched to cfi port 3, ts 1,
C bits 7..6 which is connected to cdr
C of the decentralized idec
C cfi ts 8-11 represent thus iom2 ch.2
C * ts 10 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 28
W /LINECA/EPIC/MARSCR/MACR 78
C * ts 11 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 29
W /LINECA/EPIC/MARSCR/MACR 78B
C * ts 10 upstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR 78
C * ts 11 upstream:
W /LINECA/EPIC/MARSCR/MADR 89
W /LINECA/EPIC/MARSCR/MAAR A9
W /LINECA/EPIC/MARSCR/MACR 75
C * downstream connection d ch.:
W /LINECA/EPIC/MARSCR/MADR 09
W /LINECA/EPIC/MARSCR/MAAR 07
W /LINECA/EPIC/MARSCR/MACR 75
C
C cfi time slots 14 and 15 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C cfi ts 12-15 represent thus iom2 ch3
C * ts 14 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 38
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 15 downstream:
W /LINECA/EPIC/MARSCR/MAAR 39
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 14 upstream:
W /LINECA/EPIC/MARSCR/MAAR B8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 15 upstream:
W /LINECA/EPIC/MARSCR/MAAR B9
W /LINECA/EPIC/MARSCR/MACR 7A
C * pem status is
R /LINECA/EPIC/MARSCR/STAR 05
C * not synchronized (pss=0)
C
C setting epic to normal mode
W /LINECA/EPIC/MARSCR/OMDR C0
R /LINECA/EPIC/MARSCR/ISTA 08
R /LINECA/EPIC/MARSCR/STAR 25
C pcm status: synchronized (pss=1)
C
C initialization of the pcm tristate
C field, all ch. to high impedance
W /LINECA/EPIC/MARSCR/MADR 00
W /LINECA/EPIC/MARSCR/MACR 68
C
C activation epic:
C * normal mode, pcm and cfi active
C * cfi output drivers push-pull
C * mf ch. handshake protocol enabled
W /LINECA/EPIC/MARSCR/OMDR E6
C
C reset cififo:
W /LINECA/EPIC/MARSCR/CMDR 10
C
C setting pcm port0, ts 5 to low
C impedance:
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 89
W /LINECA/EPIC/MARSCR/MACR 60
C
C mask of idec1 interrupts:
W /LINECA/IDEC/COMMON/VISM 0F
C
C initialization of idec1
C * single connection iom mode
C * cha assigned to iom ch0, uncond.
C  transmission, no address compare
C  (completely decentral d channel
C  handling)
C * chb not used (central d handling)
C * chc assigned to iom ch2, master
C  mode, sapi s compare (mixed d ch.
C  handling)
C * chd not used (analog iom)
C
C common registers:
W /LINECA/IDEC/COMMON/CCR 82
W /LINECA/IDEC/COMMON/ACR 4A
C
C cha registers:
W /LINECA/IDEC/CHA_A/MODE 0C
C
C chc registers:
W /LINECA/IDEC/CHA_C/TSR 04
W /LINECA/IDEC/CHA_C/MODE 6C
C
C * enabling interrupts, reset cha,c
W /LINECA/IDEC/COMMON/VISM 0A
W /LINECA/IDEC/CHA_A/CMDR C1
R /LINECA/IDEC/CHA_A/ISTA 10
R /LINECA/IDEC/CHA_A/STAR 11
W /LINECA/IDEC/CHA_C/CMDR C1
R /LINECA/IDEC/CHA_C/ISTA 50
R /LINECA/IDEC/CHA_C/STAR 51
C
C initialization of idec2
C * single connection ts mode
C * ch b is assigned to pcm port0, ts5
C  bits 1..0, uncond. transmission
C  no address compare (the d ch. of
C  iom ch1 is handled centralized)
C * chc is assigned to pcm port0, ts5
C  bits 3..2, uncond., tr., sapi p
C  address compare (the p data of iom
C  ch2 is handled centralized)
C
C * common registers:
W /LINECA/IDEC_2/COMMON/CCR 04
W /LINECA/IDEC_2/COMMON/ACR 49
C
C * chb registers
W /LINECA/IDEC_2/CHA_B/TSR 17
W /LINECA/IDEC_2/CHA_B/MODE 0C
C
C * chc registers:
W /LINECA/IDEC_2/CHA_C/TSR 16
W /LINECA/IDEC_2/CHA_C/MODE 0C
C
C * enabling interrupts, reset chb,c
W /LINECA/IDEC_2/COMMON/VISM 09
W /LINECA/IDEC_2/CHA_B/CMDR C1
R /LINECA/IDEC_2/CHA_B/ISTA 30
R /LINECA/IDEC_2/CHA_B/STAR 31
W /LINECA/IDEC_2/CHA_C/CMDR C1
R /LINECA/IDEC_2/CHA_C/ISTA 50
R /LINECA/IDEC_2/CHA_C/STAR 51
C
C the line card is now ready for use
C in order to test the setup you can
C execute the track file lc_isac
C
C *****************************************
C
C *****************************************
C *               SICOFI2                *
C *****************************************
C
C Hardware: Line Card SIPB 5121
C    SICOFI2 Board SIPB 5135
C    PCM4 Adaptor SIPB 5311
C
C configuration:
C Line Card: via software
C
C    SICOFI 2: S1 in position 5
C
C    PCM4 Adaptor: J1 is open
C *****************************************
C
C SICOFI2 set up in channel 3 of IOM2
C
C    S1 in position 5
C
C *****************************************
C
C please run the track file
C    LC_IOM2.TRK
C first to configure the Line Card
C *****************************************
C
C selecting EPIC to monitor handshake
C in channel 3
W /LINECA/EPIC/MCHSTR/MFSAR 1C
C ******************************************
C in case of channel 0  MFSAR = 04  *
C   S1 position 2  *
C in case of channel 1  MFSAR = 0C  *
C   S1 position 3  *
C in case of channel 2  MFSAR = 14  *
C   S1 position 4  *
C in case of channel 4  MFSAR = 24  *
C   S1 position 6  *
C in case of channel 5  MFSAR = 2C  *
C   S1 position 7  *
C in case of channel 6  MFSAR = 34  *
C   S1 position 8  *
C in case of channel 7  MFSAR = 3C  *
C   S1 position 9  *
C ******************************************
C
C channel 3 B1 to PCM time slot 1
W /LINECA/EPIC/MARSCR/MADR 81
W /LINECA/EPIC/MARSCR/MAAR B0
W /LINECA/EPIC/MARSCR/MACR 71
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 81
W /LINECA/EPIC/MARSCR/MACR 60
C
C PCM time slot 1 to channel 3 B1
W /LINECA/EPIC/MARSCR/MADR 01
W /LINECA/EPIC/MARSCR/MAAR 31
W /LINECA/EPIC/MARSCR/MACR 71
C
C channel 3 B2 to PCM time slot 2
W /LINECA/EPIC/MARSCR/MADR 82
W /LINECA/EPIC/MARSCR/MAAR B1
W /LINECA/EPIC/MARSCR/MACR 71
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 82
W /LINECA/EPIC/MARSCR/MACR 60
C
C PCM time slot 2 to channel 3 B2
W /LINECA/EPIC/MARSCR/MADR 02
W /LINECA/EPIC/MARSCR/MAAR 30
W /LINECA/EPIC/MARSCR/MACR 71
C
C sicofi identification:
C write to SICOFI2 80h, 00h
W /LINECA/EPIC/MCHSTR/MFFIFO 80
W /LINECA/EPIC/MCHSTR/MFFIFO 00
C EPIC enable receive + transmit
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C EPIC received data
R /LINECA/EPIC/MCHSTR/STAR 26
C first byte from SICOFI2
R /LINECA/EPIC/MCHSTR/MFFIFO 80
R /LINECA/EPIC/MCHSTR/STAR 26
C second byte from SICOFI2
R /LINECA/EPIC/MCHSTR/MFFIFO 80
R /LINECA/EPIC/MCHSTR/STAR 27
C reset FIFO
W /LINECA/EPIC/MCHSTR/CMDR 01
R /LINECA/EPIC/MCHSTR/STAR 25
C initialization of sicofi:
C CR4, CR3, CR2, CR1
C 00h, 00h, 00h, 00h
C for both channels of SICOFI2
C
C SICOFI2 address = 81h
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C channel A:
W /LINECA/EPIC/MCHSTR/MFFIFO 05
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
C channel B:
W /LINECA/EPIC/MCHSTR/MFFIFO 85
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 47
C send the initialisation bytes
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C
C C power up both channels
W /LINECA/EPIC/MCHSTR/MFFIFO 24
W /LINECA/EPIC/MCHSTR/MFFIFO E4
C send the bytes
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
W /LINECA/EPIC/MCHSTR/CMDR 01
R /LINECA/EPIC/MCHSTR/STAR 25
C end of power up
C
C end of track file
C
## Contents

<table>
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<th>Page</th>
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</tr>
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<td>396</td>
</tr>
</tbody>
</table>
1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI 2 SIPB 5135
- Analog telephone directly connectable
- Ring relay on board
- Secondary protection circuit on board

2 Use

For one of our SLIC-applications a HARRIS SLIC Babyboard has been designed in order to connect it with the SICOFI Testboard STUT 2060.

With both boards it is possible to measure the transfer functions of the HARRIS SLIC HC 5502A together with the SICOFI and to check the calculations done with SICOFI coefficients program.

The signaling pins of SICOFI are connected with the control interface of the HARRIS SLIC to control the SLIC functions. Therefore it is possible to select the modes power down, power up, ringing, and to read out the status of hook switch (OFF or ON), ring/tip, and ground-key.
For practical use the SLIC Babyboard STUS 5502 is inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up like that shown in figure 1, the transfer functions of an analog line card can be established. For programming, the Byte File is used which is to be found in the HARRIS SLIC HC 5502 Application Note.
3 Circuitry

3.1 Block Diagram

Figure 2
Block Diagram of the SLIC Babyboard STUS 5502

In figure 2 the three functional blocks of the SLIC Babyboard are shown:
- SLIC
- Protection circuit
- Signaling
3.1.1 SLIC

The SLIC requires a few external components for output impedance, echo cancellation, filter capacitors, and power supply. Some of these functions are realized by the SICOFI and hence it was possible to reduce the number of extra components.

The description of the SLIC is to be found in the pertinent Application Note. The SLIC switches the ringer relay and provides a digital parallel interface to control the SLIC modes. These modes are

- power down
- conversation (active)
- ringing.

3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (secondary protection). This is realized by 2 diodes D1, D2 and the fuse resistors $R_{B1} \ldots R_{B4}$. No primary protection, however, e.g. surge arristors, is provided.

3.1.3 Signaling

The signaling lines connect the SICOFI signaling interface to the digital SLIC interface. The SICOFI switches the SLIC into one of the three possible modes and the SLIC provides the corresponding information on the loop status (ground key or on/off-hook) for the SICOFI or SICOFI-2. Actual ringing, however, is not possible because there is no ringer relais installed.

3.1.4 Power Supply

Power is supplied to the SLIC via the SLIC connector SLC.
### 3.2 Connector Pin-Outs

![Diagram of SLIC Babyboard STUS 5502 Connector SLC](image)

**Figure 3**
SLIC Connector SLC

**Note:** Pins not mentioned are not connected

<table>
<thead>
<tr>
<th>Pin</th>
<th>Row</th>
<th>Function</th>
<th>Signal</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>A</td>
<td>I</td>
<td>GND</td>
<td>Power supply</td>
</tr>
<tr>
<td>13</td>
<td>A</td>
<td>I</td>
<td>+5 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>19</td>
<td>A</td>
<td>I</td>
<td>–48 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>21</td>
<td>A</td>
<td>I</td>
<td>SO1</td>
<td>/RC</td>
</tr>
<tr>
<td>22</td>
<td>A</td>
<td>I</td>
<td>SO2</td>
<td>/PD</td>
</tr>
<tr>
<td>24</td>
<td>A</td>
<td>O</td>
<td>SI1</td>
<td>/SHD</td>
</tr>
<tr>
<td>25</td>
<td>A</td>
<td>O</td>
<td>SI2</td>
<td>/GKD</td>
</tr>
<tr>
<td>26</td>
<td>A</td>
<td>I</td>
<td>SI3</td>
<td>/GKD</td>
</tr>
<tr>
<td>28</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>29</td>
<td>A</td>
<td>O</td>
<td>VIN</td>
<td>4-wire analog output</td>
</tr>
<tr>
<td>31</td>
<td>A</td>
<td>I</td>
<td>VOUT</td>
<td>4-wire analog input</td>
</tr>
<tr>
<td>32</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>4</td>
<td>C</td>
<td>I</td>
<td>+12 V</td>
<td>Power supply</td>
</tr>
</tbody>
</table>
3.3 Wiring Diagram

Figure 4
Wiring Diagram
### 3.4 List of Replaceable Parts

<table>
<thead>
<tr>
<th>Component</th>
<th>Type/Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>HC 5502</td>
</tr>
<tr>
<td>D1 … D4</td>
<td>BAY 45</td>
</tr>
<tr>
<td>D5, D6</td>
<td>ZPO3V9</td>
</tr>
<tr>
<td>C₁</td>
<td>470 nF/100 V</td>
</tr>
<tr>
<td>C₂</td>
<td>150 nF/100 V</td>
</tr>
<tr>
<td>C₃</td>
<td>1 µF/100 V</td>
</tr>
<tr>
<td>C₄</td>
<td>330 nF/100 V</td>
</tr>
<tr>
<td>Cₓₓ, Cₓᵣ</td>
<td>470 nF/100 V</td>
</tr>
<tr>
<td>R₁, R₂</td>
<td>1 k Ω</td>
</tr>
<tr>
<td>Rₓ₁ … Rₓ₄</td>
<td>150 Ω</td>
</tr>
<tr>
<td>Rₓ</td>
<td>10 k Ω</td>
</tr>
</tbody>
</table>

### 3.5 Floor Plan

![Floor Plan of the STUS 5502 Babyboard](image)

**Figure 5**

Floor Plan of the STUS 5502 Babyboard
4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be configured by means of setting the jumpers J1 and J2 and switches S1 and S2.

Possible configurations are:

- with or without voltage divider in receive direction
- connection to 4-wire SLIC side

The Babyboard contains two jumpers J1 and J2 to select the voltage divider, and two switches S1 and S2 to establish the connection to the 4-wire SLIC side (see figure 5).

Voltage divider not used \( J1 \) set
Voltage divider used \( J2 \) set
Connection to SICOFI VIN \( S2 \) in position ON
Connection to SICOFI VOUT \( S1 \) in position ON

4.2 Mode Select

The actual modes of the HARRIS SLIC HC 5502 are selected by the digital interface. This interface is connected to the signaling pins of the SICOFI. The signaling commands are different for the SICOFI Testboard STUT 2060 and for the SICOFI-2 Board SIPB 5135.

4.2.1 Mode Select for STUT 2060

Mode selection differs for the Testboard STUT 2060 being equipped with the SICOFI PEB 2060 or with the SICOFI-2 PEB 2260.

Following byte sequences apply to the STUT 2060 using the PEB 2060:

\[
\begin{align*}
\text{SIG0} &= 80 \quad \text{power down} \\
\text{SIG0} &= C0 \quad \text{active, conversation} \\
\text{SIG0} &= 30 \quad \text{ringing (no on-board ring relais)}
\end{align*}
\]

The line status (off-hook/ground-key), which is selected by the above signaling, can be read out via the SICOFI SIP-line:

\[
\begin{align*}
\text{SIG0: 7F} & \quad \text{ON-hook} \\
\text{SIG0: 6F} & \quad \text{OFF-hook and ground-key} \\
\text{SIG0: 0F} & \quad \text{OFF-hook (no ground-key)}
\end{align*}
\]

Following byte sequences apply to the STUT 2060 using the PEB 2260 for both channels:

\[
\begin{align*}
\text{SIG0} &= 11 \quad \text{power down} \\
\text{SIG0} &= 33 \quad \text{active, conversation} \\
\text{SIG0} &= 00 \quad \text{ringing (no on-board ring relais)}
\end{align*}
\]

The line status can be read out via the SICOFI SIP-line:

\[
\begin{align*}
\text{SIG0: 77} & \quad \text{ON-hook} \\
\text{SIG0: 00} & \quad \text{OFF-hook and ground-key} \\
\text{SIG0: 66} & \quad \text{OFF-hook (no ground-key)}
\end{align*}
\]
4.2.2 Mode Select for SIPB 5135

Following byte sequences apply to the SIPB 5135 using the PEB 2260 channel A (channel B = +80H):

- C/I = 07 power down
- C/I = 0F active, conversation
- C/I = 03 ringing (no on-board ring relais)

The loop and ground key information are available from the SICOFI-2 Board for both SLICs at the same time):

- C/I = DB loop detection: OFF-hook, ground key not pushed
- C/I = 03 loop detection: OFF-hook, ground key pushed
- C/I = FF loop detection: ON-hook

5 Glossary

- DIR Direction signal (same as FSC)
- FSC Frame Synchronization Clock
- PC Personal Computer
- PCM Pulse Code Modulation
- SICOFI Signal processing Codec Filter
- SIG SIGnaling byte at the SIP-line
- SIP Serial Interface Port
- SIPB Siemens ISDN PC User Board (system)
- SLD Subscriber Line Data
- STUS Siemens Telecom User Board SLIC
- STUT Siemens Telecom User Board Testboard
- SYP Synchronous Port
6 Application and Example

The Babyboard STUS 5502 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using HARRIS SLICs HC 5502A. To demonstrate its functionality a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in chapter 4. The PCM4 is connected to the Testboard for to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SICOFI PEB 2060 + HARRIS SLIC HC 5502". The byte file (HC5502.BYT) is shown in the following table 1 for the SICOFI Testboard STUT 2060 using the PEB 2060:

Table 1
Byte File to Program the SICOFI®

<table>
<thead>
<tr>
<th>PSR</th>
<th>CAM00</th>
<th>CAM20</th>
<th>CIW0</th>
<th>CIW0</th>
<th>CIW0</th>
<th>CIW0</th>
<th>CIW0</th>
<th>CIW0</th>
<th>CIW0</th>
<th>CIW0</th>
<th>CIW0</th>
<th>CIW0</th>
<th>CIW0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>36</td>
<td>41</td>
<td>40</td>
<td>06, F4, 80</td>
<td>13, 30, BA, EA, 25, 23, 41, C1, BB</td>
<td>23, 50, C8, B5, 4A, C2, 21, 04, 90</td>
<td>2B, D0, C8, 84, DC, B1, 93, 02, 1D</td>
<td>30, A0, 11, 20, 92</td>
<td>03, C4, 12, 23, 32, 72, B9, B2, BA</td>
<td>0B, 00, 97, FD, C8, DD, 4C, C2, BC</td>
<td>18, 19, 19, 11, 19</td>
<td>26, F4, 78</td>
<td>C0</td>
</tr>
</tbody>
</table>

Switch and Jumpers Settings

Before connecting the Testboard to the PCM4 and SLIC Babyboard respectively, make sure that all jumpers and switches are set correctly.

Testboard:  DIL switch 1.1 – 1.4 ON  
DIL switch 2.1 – 2.4 ON

Babyboard:  Voltage divider not used J1 set  
Voltage divider used J2 set  
Connection to SICOFI VIN S2 in position ON  
Connection to SICOFI VOUT S1 in position ON
Figure 6
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:

1. PC IBM AT or compatible
2. PCM4 (Measuring set of Wandel & Goltermann)
3. SICOFI Testboard STUT 2060
4. SLIC Babyboard
SLIC Babyboard STUS 5509 for HARRIS SLIC HC 5509

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2 Use ................................................................. 399

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1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Board SIPB 5135
- Analog telephone directly connectable
- Ring relay on board
- Secondary protection circuit on board

2 Use

For one of our SLIC-applications a HARRIS SLIC Babyboard has been designed in order to connect it with the SICOFI Testboard STUT 2060.

With both boards it is possible to measure the transfer functions of the HARRIS SLIC HC 5509 together with the SICOFI and to check the calculations done with SICOFI coefficients program.

The signaling pins of SICOFI are connected with the control interface of the HARRIS SLIC to control the SLIC functions. Therefore it is possible to select the modes power down, power up, ringing and to read out the status of hook switch (OFF or ON), ring/tip, and ground-key.
For practical use the SLIC Babyboard STUS 5509 is inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up like that shown in figure 1, the transfer functions of an analog line card can be established. For programming, the Byte File is used which is to be found in the HARRIS SLIC HC 5502 Application Note, the SICOFI however has to be switched to the ‘AGR’ with 6 dB attenuation. The reason is that in contrast to the STUS 5502 the STUS 5509 has no voltage devider on board.
3 Circuitry

3.1 Block Diagram

Figure 2
Block Diagram of the SLIC Babyboard STUS 5509

In figure 2 the four functional blocks of the SLIC Babyboard are shown:

- SLIC
- Protection circuit
- Signaling
- Ring detector
3.1.1 SLIC

The SLIC requires a few external components for output impedance, echo cancellation, filter capacitors, and power supply. Some of these functions are realized by the SICOFI and hence it was possible to reduce the number of extra components.

The description of the SLIC is to be found in the HC 5502A Application Note. The SLIC switches the ringer relay and provides a digital parallel interface to control the SLIC modes. These modes are

– power down
– conversation (active)
– ringing.

3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (secondary protection). This is realized by 2 diodes D1, D2 and the fuse resistors $R_{B1} \ldots R_{B4}$. No primary protection, however, e.g. surge arrestors, is provided.

3.1.3 Signaling

The signaling lines connect the SICOFI signaling interface to the digital SLIC interface. The SICOFI switches the SLIC into one of the three possible modes and the SLIC provides the corresponding information on the loop status (ground key or on/OFF-hook) for the SICOFI or SICOFI-2.

3.1.4 Ring Detector

The ring detector provides a signal when the ringing signal crosses 0 V. Only in this moment the SLIC can activate the ring relais, because there is no noise on the line.

3.1.5 Power Supply

Power is supplied to the SLIC via the SLIC connector SLC.
### 3.2 Connector Pin-Outs

![Diagram](ITC02535)

**Figure 3**

SLIC Connector SLC

**Note:** Pins not mentioned are not connected.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Row</th>
<th>Function</th>
<th>Signal</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>A</td>
<td>I</td>
<td>GND</td>
<td>Power supply</td>
</tr>
<tr>
<td>13</td>
<td>A</td>
<td>I</td>
<td>+5 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>19</td>
<td>A</td>
<td>I</td>
<td>–48 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>21</td>
<td>A</td>
<td>I</td>
<td>SO1</td>
<td>/F0</td>
</tr>
<tr>
<td>22</td>
<td>A</td>
<td>I</td>
<td>SO2</td>
<td>/F1</td>
</tr>
<tr>
<td>23</td>
<td>A</td>
<td>I</td>
<td>SO3</td>
<td>/TEST</td>
</tr>
<tr>
<td>24</td>
<td>A</td>
<td>O</td>
<td>SI1</td>
<td>/SHD</td>
</tr>
<tr>
<td>25</td>
<td>A</td>
<td>O</td>
<td>SI2</td>
<td>/GKD</td>
</tr>
<tr>
<td>26</td>
<td>A</td>
<td>I</td>
<td>SI3</td>
<td>/ALARM</td>
</tr>
<tr>
<td>28</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>29</td>
<td>A</td>
<td>O</td>
<td>VIN</td>
<td>4-wire analog output</td>
</tr>
<tr>
<td>31</td>
<td>A</td>
<td>I</td>
<td>VOUT</td>
<td>4-wire analog input</td>
</tr>
<tr>
<td>32</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>4</td>
<td>C</td>
<td>I</td>
<td>+12 V</td>
<td>Power supply</td>
</tr>
</tbody>
</table>
3.3 Wiring Diagram

Figure 4
Wiring Diagram of the SLIC Babyboard STUS 5509
### 3.4 List of Replaceable Parts

<table>
<thead>
<tr>
<th>Component</th>
<th>Type/Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1 … D5</td>
<td>1N4007</td>
</tr>
<tr>
<td>D6</td>
<td>BZX55C3V3</td>
</tr>
<tr>
<td>D7</td>
<td>1N4148</td>
</tr>
<tr>
<td>C₁</td>
<td>300 nF/30 V</td>
</tr>
<tr>
<td>C₂</td>
<td>680 nF/20 V</td>
</tr>
<tr>
<td>C₃, C₄</td>
<td>1 μF/100 V</td>
</tr>
<tr>
<td>C₅</td>
<td>47 nF</td>
</tr>
<tr>
<td>C₆</td>
<td>2.2 μF/40 V</td>
</tr>
<tr>
<td>C₇</td>
<td>100 nF</td>
</tr>
<tr>
<td>C₈</td>
<td>1 μF</td>
</tr>
<tr>
<td>Cₛ₁, Cₛ₂</td>
<td>100 nF</td>
</tr>
<tr>
<td>CₐCensitive</td>
<td>470 nF/100 V</td>
</tr>
<tr>
<td>R₁</td>
<td>3.3 kΩ</td>
</tr>
<tr>
<td>R₂, R₃</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>R₄</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>Rₛ₁ ... Rₛ₄</td>
<td>50 Ω 1 %</td>
</tr>
<tr>
<td>Rₛ₁, Rₛ₂</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>Rₐ, Rₐ₂</td>
<td>100 kΩ</td>
</tr>
<tr>
<td>Rᶠ</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>Z₀</td>
<td>60 kΩ</td>
</tr>
</tbody>
</table>

### 3.5 Floor Plan

![Floor Plan of the STUS 5509 Babyboard](image)

**Figure 5**
Floor Plan of the STUS 5509 Babyboard
4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be connected to the a/b-lines or a telephone and to be plugged to the Testboard.

4.2 Mode Select

The actual modes of the HARRIS SLIC HC 5509 are selected by the digital interface. This interface is connected to the signaling pins of the SICOFI. The signaling commands are different for the SICOFI Testboard STUT 2060 and for the SICOFI-2 Board SIPB 5135. In addition a software reset is required to switch it to the conversation mode.

4.2.1 Mode Select for STUT 2060

Mode selection differs for the Testboard STUT 2060 being equipped with the SICOFI PEB 2060 or with the SICOFI-2 PEB 2260. Following byte sequences apply to the STUT 2060 using the PEB 2060:

SIG0 = 60  power down
SIG0 = 20  active, conversation
SIG0 = 10  ringing
SIG0 = E0  loop power denial active

The line status (OFF-hook/ground-key), which is selected by the above signaling, can be read out via the SICOFI SIP-line:

SIG0: 111x xxxx  ON-hook
SIG0: 001x xxxx  OFF-hook and ground-key
SIG0: 011x xxxx  OFF-hook (no ground-key)
SIG0: xx0x xxxx  thermal protection active

Conversation is programmed as follows:

SIG0 = 20
SIG0 = 60
SIG0 = 20

Following byte sequences apply to the STUT 2060 using the PEB 2260 for both channels:

SIG0 = 66  power down
SIG0 = 44  active, conversation
SIG0 = 33  ringing (no ON-board ring relais)

The line status can be read out via the SICOFI SIP-line (both SLICs have the same status):

SIG0: x111 x111  ON-hook
SIG0: x010 x010  OFF-hook and ground-key
SIG0: x110 x110  OFF-hook (no ground-key)
4.2.2 Mode Select for SIPB 5135

Following byte sequences apply to the SIPB 5135 using the PEB 2260 channel A (channel B = + 80h):

- C/I = 7B: power down
- C/I = 73: active, conversation
- C/I = 0F: ringing (no ON-board ring relais)

The loop and ground key information are available from the SICOFI-2 Board for both SLICs at the same time):

- C/I = DB: loop detection: OFF-hook, ground key not pushed
- C/I = 93: loop detection: OFF-hook, ground key pushed
- C/I = FF: loop detection: ON-hook

5 Glossary

- DIR: Direction signal (same as FSC)
- FSC: Frame Synchronization Clock
- PCM: Pulse Code Modulation
- SICOFI: Signal processing CODEC Filter
- SIG: Signaling byte at the SIP-line
- SIP: Serial Interface Port
- SIPB: Siemens ISDN PC User Board (system)
- SLC: SLIC Interface Connector
- SLD: Subscriber Line Data
- SLIC: Subscriber Line Interface Circuit
- STUS: Siemens Telecom User Board SLIC
- STUT: Siemens Telecom User Board Testboard
- SYP: Synchronous Port
6 Application and Example

The Babyboard STUS 5509 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using HARRIS SLICs HC 5509. To demonstrate its functionality a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in chapter 4. The PCM4 is connected to the Testboard for to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SICOFI PEB 2060 + HARRIS SLIC HC 5509". The byte file (HC5509.byt) is shown in the following table 1 for the SICOFI Testboard STUT 2060 using the PEB 2060:

<table>
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<th>Table 1</th>
<th>Byte File to Program the SICOFI®</th>
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</thead>
<tbody>
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<td>PSR = 36</td>
<td></td>
</tr>
<tr>
<td>CAM00 = 41</td>
<td></td>
</tr>
<tr>
<td>CAM20 = 40</td>
<td></td>
</tr>
<tr>
<td>CIW0 = 06, 04, 80</td>
<td></td>
</tr>
<tr>
<td>CIW0 = 13, 30, BA, EA, 25, 23, 41, C1, BB</td>
<td></td>
</tr>
<tr>
<td>CIW0 = 23, 50, C8, B5, 4A, C2, 21, 04, 90</td>
<td></td>
</tr>
<tr>
<td>CIW0 = 2B, D0, C8, 84, DC, B1, 93, 02, 1D</td>
<td></td>
</tr>
<tr>
<td>CIW0 = 30, A0, 11, 20, 92</td>
<td></td>
</tr>
<tr>
<td>CIW0 = 03, C4, 12, 23, 32, 72, B9, B2, BA</td>
<td></td>
</tr>
<tr>
<td>CIW0 = 0B, 00, 97, FD, C8, DD, 4C, C2, BC</td>
<td></td>
</tr>
<tr>
<td>CIW0 = 18, 19, 19, 11, 19</td>
<td></td>
</tr>
<tr>
<td>SIG0 = 20</td>
<td></td>
</tr>
<tr>
<td>SIG0 = 60</td>
<td></td>
</tr>
<tr>
<td>SIG0 = 20</td>
<td></td>
</tr>
<tr>
<td>CIW0 = 25, 00, 18, 04, 78</td>
<td></td>
</tr>
</tbody>
</table>

Switch and Jumpers Settings

Before connecting the Testboard to the PCM4 and SLIC Babyboard respectively, make sure that all jumpers and switches are set correctly.

Testboard: DIL switch 1.1 – 1.4 ON
           DIL switch 2.1 – 2.4 ON
Figure 6
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:

1  PC IBM AT or compatible
1  PCM4 (Measuring set by Wandel & Goltermann)
1  SICOFI Testboard STUT 2060
1  SLIC Babyboard
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<td>421</td>
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</tbody>
</table>
1 **Features**

- Performs telephone line interface functions
- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Board SIPB 5135
- Analog telephone directly connectable to the SLIC Babyboard
- Ring relay driver provided on board
- Secondary protection circuit on board
- Loop monitoring functions

2 **Use**

For applications of the ERICSSON SLIC PBL 3736 an ERICSSON SLIC Babyboard has been designed. This Babyboard fits to the SICOFI Testboard STUT 2060.

By means of these two boards, namely the SLIC Babyboard and the SICOFI Testboard, the transfer functions, levels, return loss, transhybrid loss, and other properties of the SLIC linked to the SICOFI can be evaluated. This way test results obtained with the PCM4 Measuring Set and calculations performed by the SICOFI Coefficients Program can be compared. By doing so, the validity of the calculations is checked and errors that might have occurred can be eliminated.

To program the SLIC functions the signaling pins of the SICOFI are connected to the control interface of the ERICSSON SLIC. It is possible to select the modes

- power down
- power up
- ringing

and also to read out the status of the loop current detector and the ring/trip comparator.
Connecting the SLIC Babyboard to the SICOFI® Testboard

The SLIC Babyboard STUS 3736 must be inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up as shown in figure 1, the transfer functions of an analog line card can be measured. The programming bytes which have been calculated with the SICOFI Coefficients Program are sent via the RS232 interface to the SICOFI on the testboard.
3 Circuitry

3.1 Block Diagram

Figure 2
Block diagram of the SLIC Babyboard STUS 3736

In figure 2 the four functional blocks of the SLIC Babyboard are shown:

- SLIC
- Protection circuit
- Signaling
- Ringing

3.1.1 SLIC

The SLIC requires some external components for output impedance matching, echo cancellation, filter completion, and power supply. Some of these functions are already provided by the SICOFI and hence it was possible

a) to reduce the number of extra components and
b) to use one SLIC hardware for two different country specifications.

The SLIC is described in the Application Note "Calculating SLIC Transfer Functions of the ERICSSON SLIC PBL 3736 Using K-Parameters and SPICE".

The SLIC switches the ring relay and provides a digital parallel interface to control the SLIC modes. These different modes are

- power-down (stand-by state: the loop current is reduced to 1.5 times the loop current detector threshold)
- conversation (normal state: signal transmission is normal)
- ringing (the ring relay driver is activated).
3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (secondary protection). This is realized by 4 diodes D2 ... D5 and the fuse resistors RF1 and RF2 for energy dissipation. No primary protection, however, e.g. by surge arrestors, is provided.

3.1.3 Signaling

The signaling lines connect the SICOFI signaling interface to the digital SLIC interface (Pins E₀, C₁, C₂, C₃, DET). Via these pins the SICOFI switches the SLIC into one of the three possible modes (power-up, power-down, and ringing). The SLIC performs two different loop monitoring functions, namely loop current detection and ring/trip status detection. The respective detectors report their status through the SLIC output pin DET (pin 13) and thus provide the corresponding information about the loop current or ring/trip status to the SICOFI. The DET output is enabled by the "read enable pin" E₀. A logic HIGH enables the DET pin, a logic LOW disables the DET output. If you want to get information about the loop functions of the SLIC, you have to program the SICOFI with the signaling byte so that the E₀ pin is set to a logic HIGH. Examples are given in chapters 4.2.1 "Mode Select for STUT 2060" and 4.2.2 "Mode Select for SIPB 5135" respectively.

The actual state of operation of the SLIC determines which monitoring function is provided by the DET output, e.g. in the normal state the DET pin provides the loop current status.

For programming the SLIC the configuration registers 1 and 2 of the SICOFI have to be defined correctly in order to match the controlling pins of the SLIC to the signaling pins of the SICOFI. The pins C₃, C₂, C₁, DET, and E₀ of the SLIC are connected to the SICOFI pins SO1, SO2, SA, SI1 and SO3. When the SICOFI is in the SLD mode the signaling byte puts the SLIC to the desired status; being in the IOM mode, the Command/Indicate byte sets the operating state.

3.1.4 Power Supply

Power is supplied to the SLIC via the SLIC connector SLC. A relay switches the ringing voltage from the SLC to the a/b-line.
### 3.2 Connector Pin-Outs

![Diagram of SLIC Connector SLC](image)

**Figure 3**
SLIC Connector SLC

**Note 1:** Pins not mentioned are not connected

**Note 2:** The pin numbering in the list below refers to the numbering on the SICOFI Testboard

<table>
<thead>
<tr>
<th>Pin</th>
<th>Row</th>
<th>Function</th>
<th>Signal</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>A</td>
<td>I</td>
<td>SCLK</td>
<td>Clock</td>
</tr>
<tr>
<td>12</td>
<td>A</td>
<td>I</td>
<td>GND</td>
<td>Power supply</td>
</tr>
<tr>
<td>13</td>
<td>A</td>
<td>I</td>
<td>+5V</td>
<td>Power supply</td>
</tr>
<tr>
<td>14</td>
<td>A</td>
<td>I</td>
<td>65 V AC</td>
<td>Ringer power supply 65 V AC</td>
</tr>
<tr>
<td>15</td>
<td>A</td>
<td>I</td>
<td>–5V</td>
<td>Power supply</td>
</tr>
<tr>
<td>16</td>
<td>A</td>
<td>I</td>
<td>Reset</td>
<td>Reset</td>
</tr>
<tr>
<td>19</td>
<td>A</td>
<td>I</td>
<td>–48 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>21</td>
<td>A</td>
<td>I</td>
<td>SO1</td>
<td>C3</td>
</tr>
<tr>
<td>22</td>
<td>A</td>
<td>I</td>
<td>SO2</td>
<td>C2</td>
</tr>
<tr>
<td>23</td>
<td>A</td>
<td>I</td>
<td>SO3</td>
<td>E0</td>
</tr>
<tr>
<td>24</td>
<td>A</td>
<td>O</td>
<td>SI1</td>
<td>/DET</td>
</tr>
<tr>
<td>25</td>
<td>A</td>
<td>O</td>
<td>+5V</td>
<td>SI2</td>
</tr>
<tr>
<td>26</td>
<td>A</td>
<td>O</td>
<td>+5V</td>
<td>SI3</td>
</tr>
<tr>
<td>28</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>29</td>
<td>A</td>
<td>O</td>
<td>VIN</td>
<td>4 wire analog output</td>
</tr>
<tr>
<td>30</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>31</td>
<td>A</td>
<td>I</td>
<td>VOUT</td>
<td>4 wire analog input</td>
</tr>
<tr>
<td>32</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>21</td>
<td>C</td>
<td>O</td>
<td>SA</td>
<td>C1</td>
</tr>
</tbody>
</table>
3.3 Wiring Diagram

Figure 4
Wiring Diagram
## 3.4 List of Replaceable Parts

<table>
<thead>
<tr>
<th>Component</th>
<th>Type/Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>PBL 3736</td>
</tr>
<tr>
<td>IC2</td>
<td>HC4040</td>
</tr>
<tr>
<td>IC3</td>
<td>HCT125</td>
</tr>
<tr>
<td>D1</td>
<td>1N4448</td>
</tr>
<tr>
<td>D2, D3, D4, D5</td>
<td>BAV 19</td>
</tr>
<tr>
<td>C_D</td>
<td>10 nF</td>
</tr>
<tr>
<td>C_DC</td>
<td>150 nF</td>
</tr>
<tr>
<td>C_HP, C_RT</td>
<td>220 nF</td>
</tr>
<tr>
<td>C_CH1</td>
<td>47 nF</td>
</tr>
<tr>
<td>C_CH2</td>
<td>560 pF</td>
</tr>
<tr>
<td>C_T, C_R</td>
<td>2.2 nF</td>
</tr>
<tr>
<td>C_BAT, C_Q</td>
<td>330 nF</td>
</tr>
<tr>
<td>C_FIL</td>
<td>470 nF</td>
</tr>
<tr>
<td>C_TX</td>
<td>1 µF</td>
</tr>
<tr>
<td>R_1, R_2</td>
<td>390 R</td>
</tr>
<tr>
<td>R_3, R_4</td>
<td>205 kΩ</td>
</tr>
<tr>
<td>R_8, R_9, R_11</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>R_D</td>
<td>51.1 kΩ</td>
</tr>
<tr>
<td>R_DC1, R_DC2</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>R_T</td>
<td>560 kΩ</td>
</tr>
<tr>
<td>R_IX</td>
<td>22 kΩ</td>
</tr>
<tr>
<td>R_F1, R_F2</td>
<td>20 R</td>
</tr>
<tr>
<td>R_CH</td>
<td>680 R</td>
</tr>
<tr>
<td>R_B1, R_B2</td>
<td>249 kΩ</td>
</tr>
<tr>
<td>R_RX</td>
<td>300 kΩ</td>
</tr>
<tr>
<td>K1</td>
<td>Relay 5 V</td>
</tr>
</tbody>
</table>
4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be configured by means of DIP switches S1 and S2.

Possible configurations are:

– Switch S1 for the HCT125
  Switched to the left side (away from switch S2) the HCT 125 puts through the signal from the frequency divider HC4040 to the clock input of the SLIC.
  Switched to the right side, the driver is switched OFF.

– Switch S2 for the HC4040
  Switched to the left side (towards switch S1) the 512 kHz clock frequency coming from the SICOFI is divided by two. Thus the SLIC is provided with the nominal frequency of 256 kHz.
  In case the SICOFI is in the IOM-2 mode and provides a frequency of 4096 kHz, the switch has to be in the right position (away from switch S1). The 4096 kHz frequency from the SICOFI then is divided down to 256 kHz.
Figure 6
SLIC Babyboard with the switches S1 and S2

SIG0 = 20 Open-circuit state: The TIPX and the RINGX power amplifier present a high impedance to the line; loop current detector not active.
SIG0 = 22 Ringing state: Ring relay driver activated, ring trip detector is connected to the detector output (/DET), TIPX and RINGX are in the high-impedance state, and signal transmission is inhibited.
SIG0 = 60 Normal state: TIPX is the terminal closest to GND and sources loop current; signal transmission is normal, loop current detector is ON.
SIG0 = 62 Stand-by state: The loop current is limited to 1.5 times the loop current detector threshold current, loop current detector is ON.
SIG0 = A0 TIPX open-circuit state: The TIPX power amplifier presents a high impedance to the line, loop current detector is ON.
SIG0 = E0 Polarity reversal state: TIPX and RINGX polarity is reversed compared to normal state: RINGX is closest to GND and sources current, TIPX sinks current, loop current detector is ON, signal transmission is normal.
SIG0 = C2 Polarity reversal and stand-by state: See above.

Following byte sequences apply to the STUT 2060 using the PEB 2260 for both channels:
SIG0 = 44 Open-circuit state
SIG0 = CC Ringing state
SIG0 = 66 Normal state
SIG0 = EE Stand-by state
SIG0 = 55 TIPX open-circuit state
SIG0 = 77 Polarity reversal state
SIG0 = FF Polarity reversal and stand-by state.
4.2 Mode Select for SIPB 5135

The following byte sequences apply to the SIPB 5135 using the **PEB 2260** for programming channel A. For programming channel B one has to add 80hex to the C/I commands listed below. E.g. for putting the SLIC to channel B in the normal state, the command would be:  
C/I = CB (4BH + 80H ).  
C/I = 43 Open-circuit state  
C/I = 53 Ringing state  
C/I = 4B Normal state  
C/I = 5B Stand-by state  
C/I = 47 TIPX open-circuit state  
C/I = 4F Polarity reversal state  
C/I = 5F Polarity reversal and stand-by state

When the SICOFI-2 Board output C3A is a detection select output, then the loop and ground key information are available from the SICOFI-2 Board.
5 Application and Example

The Babyboard STUS 3736 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using the ERICSSON SLIC PBL 3736. To demonstrate its functionality, a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in section 4. The PCM4 is connected to the Testboard to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "Calculating SLIC Transfer Functions of the ERICSSON SLIC PBL 3736 Using K-Parameters and SPICE". The byte file for the SICOFI Testboard STUT 2060 using the PEB 2060 is shown below in table 1:

Table 1
Byte File to Program the SICOFI® PEB 2060

| PSR  = 36 |
| CAM00 = 41 |
| CAM20 = 40 |
| CIW0 = 26, 04, 80 |
| CIW0 = 13, 30, FA, BA, 52, 14, C2, B1, 2C |
| CIW0 = 23, F0, 19, 87, FB, 19, E5, 0A, B5 |
| CIW0 = 2B, F0, 19, 87, FC, 29, 16, 00, BD |
| CIW0 = 03, 4B, 2B, 23, AB, B6, 19, BB, 23 |
| CIW0 = 0B, 00, 35, C1, 32, 24, 65, 2B, AB |
| CIW0 = 18, 19, 19, 11, 19 |
| CIW0 = 30, 41, B2, 00, 23 |
| CIW0 = 25, 00, 08, 04, 78 |
| SIG0 = 60 |

Switch Settings

Before connecting the testboard to the PCM4 measuring set and SLIC Babyboard respectively, make sure that all switches are set correctly.

Testboard: DIL switch 1.1 – 1.4 ON  
DIL switch 2.1 – 2.4 ON

Babyboard: S1 in left position (away from switch S2, see figure 6)  
S2 in left position (towards switch S1, see figure 6)
Figure 7
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:
1 PC IBM AT or equivalent
1 PCM4 (Measuring set by Wandel & Goltermann)
1 SICOFI Testboard STUT 2060
1 SLIC Babyboard
SLIC Babyboard STUS 3762 for ERICSSON SLIC PBL 3762/64

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<td>Wiring Diagram</td>
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<td>4.2</td>
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<td>4.2.1</td>
<td>Mode Select for STUT 2060</td>
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<td>4.2.2</td>
<td>Mode Select for SIPB 5135</td>
</tr>
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<td>Glossary</td>
</tr>
<tr>
<td>6</td>
<td>Application and Example</td>
</tr>
</tbody>
</table>
1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Module SIPB 5135
- ERICSSON SLIC PBL 3762 or PBL 3764 to be used on board
- Analog telephone directly connectable
- Ring relay on board
- Secondary protection circuit on board

2 Use

For one of our SLIC-applications a ERICSSON SLIC Babyboard has been designed in order to connect it with the SICOFI Testboard STUT 2060.

With both boards it is possible to measure the transfer functions of the ERICSSON SLICs PBL 3762 or PBL 3764 together with the SICOFI and to check the calculations done with SICOFI coefficients program.

The signaling pins of SICOFI are connected with the control interface of the ERICSSON SLIC to control the SLIC functions. Therefore it is possible to select the modes

- power down
- power up
- ringing

and to read out the status of

- hook switch (OFF or ON),
- ring/tip, and
- ground-key.
Figure 1
Connecting the SLIC Babyboard to the SICOFl® Testboard

For practical use the SLIC Babyboard STUS 3762 is inserted into one of the SLIC connectors SLC of the SICOFl Testboard STUT 2060. Using a set-up like that shown in figure 1, the transfer functions of an analog line card can be established. For programming, the Byte File is used which is to be found in the ERICSSON SLIC PBL 3762/64 Application Note.
3  Circuitry

3.1  Block Diagram

![Block Diagram of the SLIC Babyboard STUS 3762](image)

**Figure 2**
Block Diagram of the SLIC Babyboard STUS 3762

In figure 2 the five functional blocks of the SLIC Babyboard are shown:

- SLIC
- Protection circuit
- Signaling
- Ringing
3.1.1 SLIC

The PBL 3762 and PBL 3764 SLICs are pin and software compatible the only difference being, that the PBL 3762 has resistive feeding and the PBL 3764 has constant current feeding. Thus both may be used with the SLIC Babyboard STUS 3762. The SLIC requires some external components for output impedance, echo cancellation, filter capacitors, and power supply. Some of these functions are realized by the SICOFI and hence it was possible to reduce the number of extra components.

The description of the SLIC is to be found in the pertinent Application Note. The SLIC switches the ringer relay and provides a digital parallel interface to control the SLIC modes. These modes are
- power down
- conversation (active)
- ringing.

3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (secondary protection). This is realized by 4 diodes D3 ... D6 and the fuse resistors $R_{F1}$ and $R_{F2}$. No primary protection, however, e.g. surge arrester, is provided.

3.1.3 Signaling

The signaling lines connect the SICOFI signaling interface to the digital SLIC interface. The SICOFI switches the SLIC into one of the three possible modes and the SLIC provides the corresponding information of the loop status (ground key or on/OFF-hook) for the SICOFI. When the SICOFI-2 is used in the IOM-2 mode, the SLIC sends both information (ground-key and loop status) with the detection select output enabled. In this case the SICOFI-2 changes the logic level at the output C3A every $250 \mu\text{sec}$. Depending on the logic level at the C3A output of the SICOFI-2, the SLIC transmits the ground-key or loop status to a SICOFI-2 input (I1A). The detector output switches the loop information to the signaling bit I1x, and the ground-key information to bit CI1x of the C/I-channel.

3.1.4 Power Supply

Power is supplied to the SLIC via the SLIC connector SLC. A relay switches the ringing voltage from the SLC to the a/b-line.
3.2 Connector Pin-Outs

Figure 3
SLIC Connector SLC

Note: Pins not mentioned are not connected

<table>
<thead>
<tr>
<th>Pin</th>
<th>Row</th>
<th>Function</th>
<th>Signal</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>A</td>
<td>I</td>
<td>GND</td>
<td>Power supply</td>
</tr>
<tr>
<td>13</td>
<td>A</td>
<td>I</td>
<td>+ 5 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>14</td>
<td>A</td>
<td>I</td>
<td>65 V AC</td>
<td>Ringer power supply 65 V AC</td>
</tr>
<tr>
<td>15</td>
<td>A</td>
<td>I</td>
<td>- 5 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>19</td>
<td>A</td>
<td>I</td>
<td>- 48 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>21</td>
<td>A</td>
<td>I</td>
<td>SO1</td>
<td>C2</td>
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<td>22</td>
<td>A</td>
<td>I</td>
<td>SO2</td>
<td>C1</td>
</tr>
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<td>I</td>
<td>SO3</td>
<td>E1</td>
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<td>24</td>
<td>A</td>
<td>O</td>
<td>SI1</td>
<td>/DET</td>
</tr>
<tr>
<td>26</td>
<td>A</td>
<td>I</td>
<td>DGND</td>
<td>Digital ground</td>
</tr>
<tr>
<td>28</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>29</td>
<td>A</td>
<td>O</td>
<td>VIN</td>
<td>4-wire analog output</td>
</tr>
<tr>
<td>30</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>31</td>
<td>A</td>
<td>I</td>
<td>VOUT</td>
<td>4-wire analog input</td>
</tr>
<tr>
<td>32</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>21</td>
<td>C</td>
<td>O</td>
<td>SA</td>
<td>E0</td>
</tr>
</tbody>
</table>
3.3 Wiring Diagram

Figure 4
Wiring Diagram
### 3.4 List of Replaceable Parts

<table>
<thead>
<tr>
<th>Component</th>
<th>Type/Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>PBL 3762 or PBL 3764</td>
</tr>
<tr>
<td>D1, D7</td>
<td>1N4007</td>
</tr>
<tr>
<td>D2</td>
<td>1N4148</td>
</tr>
<tr>
<td>D3, D4, D5, D6</td>
<td>BAY 45</td>
</tr>
<tr>
<td>C₁, C₂</td>
<td>2.2 nF/100 V</td>
</tr>
<tr>
<td>C₃</td>
<td>330 nF/100 V</td>
</tr>
<tr>
<td>Cₓ</td>
<td>1 µF</td>
</tr>
<tr>
<td>C₄</td>
<td>15 nF/100 V</td>
</tr>
<tr>
<td>C₅</td>
<td>3.3 nF/10 V</td>
</tr>
<tr>
<td>C₆</td>
<td>33 nF/100 V</td>
</tr>
<tr>
<td>R₁</td>
<td>5.6 Ω</td>
</tr>
<tr>
<td>R₂</td>
<td>1.2 MΩ</td>
</tr>
<tr>
<td>R₃</td>
<td>910 kΩ</td>
</tr>
<tr>
<td>R₄</td>
<td>200 kΩ</td>
</tr>
<tr>
<td>R₅</td>
<td>150 Ω/2 W</td>
</tr>
<tr>
<td>R₆</td>
<td>200 kΩ</td>
</tr>
<tr>
<td>R₇</td>
<td>0 Ω</td>
</tr>
<tr>
<td>R₈, R₉</td>
<td>4.7 kΩ</td>
</tr>
<tr>
<td>R₈</td>
<td>39 kΩ</td>
</tr>
<tr>
<td>R₁₀</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>R₁₁</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>R₁₂</td>
<td>41.2 kΩ</td>
</tr>
<tr>
<td>R₁₃</td>
<td>41.2 kΩ</td>
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<tr>
<td>Zₜ</td>
<td>598 kΩ</td>
</tr>
<tr>
<td>Zₙ</td>
<td>300 kΩ</td>
</tr>
<tr>
<td>Rₓ</td>
<td>24 kΩ</td>
</tr>
<tr>
<td>Rₛ</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>R₁₄, R₁₅</td>
<td>20 Ω</td>
</tr>
<tr>
<td>K1</td>
<td>Relay 5 V</td>
</tr>
</tbody>
</table>
3.5 Floor Plan

Figure 5
Floor Plan of the STUS 3762 Babyboard
4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be configured by means of DIP switch S1 and setting the jumpers J1 ... J4. Possible configurations are:

- with or without blocking capacitor in transmit direction
- selecting the $R_{dc}$ resistors for PBL 3762 or PBL 3764

The Babyboard contains four jumpers J1 ... J4 to select the $R_{dc}$ resistors for the PBL 3762 (20 k$\Omega$: J1, J2 set) or for the PBL 3764 (41.2 k$\Omega$: J3, J4 set) respectively.

DIP Switch S1 selects the blocking capacitor in transmit direction at the SLIC 4-wire side. When switch S1 points towards the SLIC, then the capacitor is inserted. The capacitor is shunted out, when S1 is at the distant side (see figure 6).

Figure 6
SLIC Babyboard and Switch S1
4.2 Mode Select

The actual modes of the ERICSSON SLICs PBL 3762 or PBL 3764 are selected by the digital interface. This interface is connected to the signaling pins of the SICOFI. The signaling commands are different for the SICOFI Testboard STUT 2060 and for the SICOFI-2 Board SIPB 5135.

4.2.1 Mode Select for STUT 2060

Mode selection differs for the Testboard STUT 2060 being equipped with the SICOFI PEB 2060 or with the SICOFI-2 PEB 2260.

Following byte sequences apply to the STUT 2060 using the PEB 2060:

- SIG0 = E0 stand-by, loop current detector ON
- SIG0 = C0 stand-by, ground key detector ON
- SIG0 = A0 active, loop current detector ON
- SIG0 = 80 active, ground key detector ON
- SIG0 = 60 ringing, ring/tip detector ON

The line status (OFF-hook/ground-key), which is selected by the above signaling, can be read out via the SICOFI SIP-line:

- SIG0: 80 ON-hook or ground key detection

Following byte sequences apply to the STUT 2060 using the PEB 2260 for both channels:

- SIG0 = 77 stand-by, loop current detector ON
- SIG0 = 33 stand-by, ground key detector ON
- SIG0 = 55 active, loop current detector ON
- SIG0 = 11 active, ground key detector ON
- SIG0 = 66 ringing, ring/tip detector ON

The line status (OFF-hook/ground-key), which is selected in the above signaling, can be read out via the SICOFI SIP-line:

- SIG0: 11 ON-hook or ground-key detection
4.2.2 Mode Select for SIPB 5135

Following byte sequences apply to the SIPB 5135 using the PEB 2260 channel A (channel B = +80H):

- C/I = 4F: stand-by, loop current detector ON
- C/I = 0F: stand-by, ground key detector ON
- C/I = 47: active, loop current detector ON
- C/I = 07: active, ground key detector ON
- C/I = 4B: ringing, ring/tip detector ON

When the SICOFI-2 Board output C3A is a detection select output, then the loop and ground key information are available from the SICOFI-2 Board:

- C/I = DB: loop detection OFF-hook, ground key is pushed
- C/I = 93: loop detection ON-hook, ground key is pushed
- C/I = FF: loop detection OFF-hook, ground key not found
- C/I = B7: loop detection ON-hook, ground key not found

5 Glossary

- DIR: Direction signal (same as FSC)
- FSC: Frame Synchronization Clock
- PC: Personal Computer
- PCM: Pulse Code Modulation
- SICOFI: Signal processing COdec Filter
- SIG: SIGnaling byte at the SIP-line
- SIP: Serial Interface Port
- SIPB: Siemens ISDN PC User Board (system)
- SLD: Subscriber Line Data
- STUS: Siemens Telecom User Board SLIC
- STUT: Siemens Telecom User Board Testboard
6 Application and Example

The Babyboard STUS 3762 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using ERICSSON SLICs PBL 3762/64. To demonstrate its functionality a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in chapter 4. The PCM4 is connected to the Testboard to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SICOFI PEB 2060 + ERICSSON SLIC PBL 3762". The byte file (PBL3762.BYT) is shown in the following table 1 for the SICOFI Testboard STUT 2060 using the PEB 2060:

Table 1
Byte File to Program the SICOFI®

<table>
<thead>
<tr>
<th>PSR</th>
<th>CAM00</th>
<th>CAM20</th>
<th>CIW0</th>
<th>CAM01</th>
<th>CIW1</th>
<th>CIW2</th>
<th>CIW3</th>
</tr>
</thead>
<tbody>
<tr>
<td>36</td>
<td>41</td>
<td>40</td>
<td>06</td>
<td>F4, 80</td>
<td>13, 30, 22, 2A, 6B, 2B, 22, B3, 22</td>
<td>23, F0, BC, 37, 72, 49, 36, 0F, A6</td>
<td>2B, F0, 2B, 97, 74, 2A, 27, 02, CE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>03, 35, 12, 52, 91, BE, F9, A9, F4</td>
<td>0B, 00, 33, AB, 23, 32, 73, 39, FA</td>
<td>18, 19, 19, 11, 19</td>
<td>26, F4, 78</td>
<td>A0</td>
</tr>
</tbody>
</table>

Switch and Jumpers Settings

Before connecting the Testboard to the PCM4 and SLIC Babyboard respectively, make sure that all jumpers and switches are set correctly.

**Testboard:**
- DIL switch 1.1–1.4 ON
- DIL switch 2.1–2.4 ON

**Babyboard:**
- PBL 3762 being used: J1, J2 is CLOSED, J3, J4 is OPEN
- PBL 3764 being used: J1, J2 is OPEN, J3, J4 is CLOSED
- Capacitor $C_{Kx}$ is enabled: S1 in position right (figure 6)
- Capacitor $C_{Kx}$ is shorted: S1 in position left (figure 6)
Figure 7
SICOFI® Measurement Set-Up

Required hardware for a measurement set-up:

1. PC IBM AT or compatible
2. PCM4 (Measuring set of Wandel & Goltermann)
3. SICOFI Testboard STUT 2060
4. SLIC Babyboard
### SLIC Babyboard STUS 3030 for STM SLIC L3000/L3030

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<th>Page</th>
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<td>4.1.3 Jumpers J1 ... J6</td>
<td>447</td>
</tr>
<tr>
<td>4.2 Mode Select</td>
<td>448</td>
</tr>
<tr>
<td>4.2.1 Mode Select for STUT 2060</td>
<td>448</td>
</tr>
<tr>
<td>4.2.2 Mode Select for SIPB 5135</td>
<td>449</td>
</tr>
<tr>
<td><strong>5</strong> Glossary</td>
<td>450</td>
</tr>
<tr>
<td><strong>6</strong> Application and Example</td>
<td>450</td>
</tr>
</tbody>
</table>
1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Board SIPB 5135
- Serial or parallel interface selectable
- 4-wire side of the SLIC selectable for internal or external measurements
- Analog telephone directly connectable
- External battery supply of +72 V can be connected via banana plugs

2 Use

For one of our SLIC-applications a SGS-THOMSON SLIC Babyboard has been designed in order to connect it with the SICOFI Testboard STUT 2060. With both boards it is possible to measure the transfer functions of the SGS-THOMSON SLIC L3000/L3030 together with the SICOFI and to check the calculations done with SICOFI coefficients program.

The switches S1 and S2 select the 4-wire side of the SLIC. The control interface of the L3030 is connected to the SLD line via external hardware to control the SLIC functions (serial interface). Therefore it is possible to select the modes:

- power down
- power up
- ringing
- current on the a/b-line

and to read out the status of
- hook switch (OFF or ON),
- ground-key.
Connecting the SLIC Babyboard to the SICOFI® Testboard

For practical use the SLIC Babyboard STUS 3030 is inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up like that shown in figure 1, the transfer functions of an analog line card can be established. For programming, the Byte File is used which is to be found in the SGS-THOMSON L3030 Application Note.
3 Circuitry

3.1 Block Diagram

In *figure 2* the five functional blocks of the SLIC Babyboard are shown:
- SLIC
- Protection circuit
- Signaling
- External power supply
- 4-wire connection

### 3.1.1 SLIC

The SLIC is divided into two parts, a low voltage part (L3030) and a high voltage part (L3000). The high voltage part is connected to the line. It realizes the battery feeding and switches the ringing and the speech signals in both directions through the SLIC. The line current is programmable to 4 threshold values (25 mA, 30 mA, 45 mA, and 70 mA). An internal temperature sensing part shuts the line current off, when the temperature threshold is exceeded. The ringing signal is supplied by the battery on a small AC control-voltage (0.285 Vrms). The ringing signal starts and stops when the control signal crosses zero. The maximum time to switch-on the ringing signal is 1 s. The control signal is amplified and fed in balanced mode to the line with a superimposed DC voltage of 22 V.
The low voltage part synthesizes the DC characteristics. Echo cancellation is performed by controlling the output impedance. As several of these functions are already realized by the SICOFI it was possible to reduce the number of external components.

The L3030 contains a digital interface to control the SLIC modes. These modes are

- power down
- conversation (active)
- ringing.

The L3030 contains also a capacitor multiplier. It is selected via a resistor. If used the multiplier simulated a big capacitance from two little ones. These do not require as much space and are less expensive.

### 3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (e.g. lightnings). This is realized by 2 protection circuits L3121 from SGS-THOMSON and several diodes. These circuits apply to the a/b-lines.

### 3.1.3 Signaling

Being in the serial interface mode the control interface of the SLIC is connected to the SLD-line via external hardware. Information from and to the SLIC are sent in the signaling byte of the SIP-line. The external hardware is synchronized by a PBC. Working in the parallel interface mode the SLIC gets signaling from the SICOFI signaling pins.

### 3.1.4 Power Supply

Power is supplied to the SLIC via the SLIC connector SLC. Only for battery voltage supply of +72 V in some special applications an external power source is required.

### 3.1.5 4-Wire Selection

Two switches S1 and S2 select the 4-wire connection for to measure the SLIC functions exclusively or in combination with the SICOFI.
3.2 Connector Pin-Outs

**Figure 3**
SLIC Connector SLC

**Note:** Pins not mentioned are not connected

<table>
<thead>
<tr>
<th>Pin</th>
<th>Row</th>
<th>Function</th>
<th>Signal</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>A</td>
<td>I</td>
<td>GND</td>
<td>Digital ground</td>
</tr>
<tr>
<td>13</td>
<td>A</td>
<td>I</td>
<td>+5 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>15</td>
<td>A</td>
<td>I</td>
<td>-5 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>19</td>
<td>A</td>
<td>I</td>
<td>-48 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>21</td>
<td>A</td>
<td>I</td>
<td>SO1</td>
<td>Power down</td>
</tr>
<tr>
<td>22</td>
<td>A</td>
<td>I</td>
<td>SO2</td>
<td>Timing</td>
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<tr>
<td>23</td>
<td>A</td>
<td>I</td>
<td>SO3</td>
<td>Ring</td>
</tr>
<tr>
<td>24</td>
<td>A</td>
<td>O</td>
<td>SI1</td>
<td>Ground key</td>
</tr>
<tr>
<td>25</td>
<td>A</td>
<td>O</td>
<td>SI2</td>
<td>/GKD</td>
</tr>
<tr>
<td>28</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>29</td>
<td>A</td>
<td>O</td>
<td>VIN</td>
<td>4-wire analog output</td>
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<td>30</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
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<td>31</td>
<td>A</td>
<td>I</td>
<td>VOUT</td>
<td>4-wire analog input</td>
</tr>
<tr>
<td>32</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
</tbody>
</table>
3.3 Wiring Diagram

Figure 4
Wiring Diagram of the SLIC Babyboard STUS 3030
### 3.4 List of Replaceable Parts

<table>
<thead>
<tr>
<th>Component</th>
<th>Type/Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>74HC 4040</td>
</tr>
<tr>
<td>IC2</td>
<td>74HC 00</td>
</tr>
<tr>
<td>IC3</td>
<td>74HC 08</td>
</tr>
<tr>
<td>IC4</td>
<td>74HC 74</td>
</tr>
<tr>
<td>IC5</td>
<td>74HC 32</td>
</tr>
<tr>
<td>IC6</td>
<td>L3030</td>
</tr>
<tr>
<td>IC7</td>
<td>L3000</td>
</tr>
<tr>
<td>IC8, IC9</td>
<td>L3121</td>
</tr>
<tr>
<td>IC10</td>
<td>74LS126</td>
</tr>
<tr>
<td>IC11</td>
<td>74LS241</td>
</tr>
<tr>
<td>D1 ... D6</td>
<td>1N4004</td>
</tr>
<tr>
<td>C&lt;sub&gt;1&lt;/sub&gt;, C&lt;sub&gt;2&lt;/sub&gt;</td>
<td>22 nF</td>
</tr>
<tr>
<td>C&lt;sub&gt;3&lt;/sub&gt;, C&lt;sub&gt;4&lt;/sub&gt;</td>
<td>47 µF</td>
</tr>
<tr>
<td>C&lt;sub&gt;xx&lt;/sub&gt;</td>
<td>1 µF</td>
</tr>
<tr>
<td>C&lt;sub&gt;AC1&lt;/sub&gt;, C&lt;sub&gt;AC2&lt;/sub&gt;</td>
<td>1 µF</td>
</tr>
<tr>
<td>C&lt;sub&gt;comp&lt;/sub&gt;</td>
<td>22 nF</td>
</tr>
<tr>
<td>C&lt;sub&gt;con&lt;/sub&gt;</td>
<td>150 nF</td>
</tr>
<tr>
<td>C&lt;sub&gt;res&lt;/sub&gt;</td>
<td>330 nF</td>
</tr>
<tr>
<td>R&lt;sub&gt;1&lt;/sub&gt;, R&lt;sub&gt;2&lt;/sub&gt;</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>R&lt;sub&gt;3&lt;/sub&gt;</td>
<td>4.7 kΩ</td>
</tr>
<tr>
<td>R&lt;sub&gt;REF1&lt;/sub&gt;, R&lt;sub&gt;REF2&lt;/sub&gt;</td>
<td>25.5 kΩ</td>
</tr>
<tr>
<td>R&lt;sub&gt;ix&lt;/sub&gt;</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>Z&lt;sub&gt;A&lt;/sub&gt;</td>
<td>6.2 kΩ (not installed)</td>
</tr>
<tr>
<td>Z&lt;sub&gt;B&lt;/sub&gt;</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>Z&lt;sub&gt;AC&lt;/sub&gt;</td>
<td>499 Ω</td>
</tr>
<tr>
<td>R&lt;sub&gt;R&lt;/sub&gt;</td>
<td>49.9 kΩ</td>
</tr>
<tr>
<td>R&lt;sub&gt;pc&lt;/sub&gt;</td>
<td>100 Ω</td>
</tr>
<tr>
<td>R&lt;sub&gt;DC&lt;/sub&gt;</td>
<td>300 Ω</td>
</tr>
<tr>
<td>R&lt;sub&gt;p1&lt;/sub&gt;, R&lt;sub&gt;p2&lt;/sub&gt;</td>
<td>50 Ω</td>
</tr>
</tbody>
</table>
3.5 Floor Plan

Figure 5
Floor Plan of the STUS 3030 Babyboard
4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be configured by means of setting switches S1, S2, jumpers J1 ... J6 and connecting the solder bridge for a particular application.

Possible configurations are:
- selecting the 4-wire analog side of the SLIC
- selecting serial or parallel mode at the digital interface
- using the balancing networks \( Z_A \) and \( Z_B \) and the voltage divider in receive direction

4.1.1 Setting Switches S1 and S2

The Babyboard contains two switches S1 and S2 to connect the 4-wire side of the SLIC to particular pins of the SLIC connector SLC or to the tags VIN/VOUT at the board.

<table>
<thead>
<tr>
<th>Switch</th>
<th>Position</th>
<th>Pin Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>int.</td>
<td>VIN at SLC</td>
</tr>
<tr>
<td>S1</td>
<td>ext.</td>
<td>VIN SLIC to tag VIN</td>
</tr>
<tr>
<td>S2</td>
<td>int.</td>
<td>VOUT at SLC</td>
</tr>
<tr>
<td>S2</td>
<td>ext.</td>
<td>VOUT SLIC to tag VOUT</td>
</tr>
</tbody>
</table>

4.1.2 Solder Bridges

The voltage divider and the capacitor multiplier are selected by establishing peculiar connections at solder bridges 1 ... 3:

Solder bridge 1 (below R1 – see floor plan) is to enable the voltage divider:

![Figure 6](image)

Solder Bridge 1. Left: Divider is Active. Right: Divider is Inactive.

Solder bridge 2 (close to \( C_{AC1} \) at the soldering side of the board) is to connect \( C_{AC1} \) to pin 7. If bridged, capacitor \( C_{AC1} \) is connected to pin 7.
Solder bridge 3 (near solder bridge 2) is to enable the capacitor multiplier.

![Figure 7]

Figure 7
Solder Bridge 3. Left: Capacitor Multiplier is Active ($R$ connected to pin 7). Right: Capacitor Multiplier is Inactive ($R$ disconnected, pin 7 connected to pin 14)

4.1.3 Jumpers J1 ... J6

The jumpers J1 ... J6 select the digital interface for the SLIC. Jumpers J5 and J6 are to select serial or parallel interface mode. When jumpers J1 or J2 are set, being in the serial interface mode, the SLIC is connected to external hardware; instead, being in parallel interface mode, it is connected to the SICOFI signaling interface via the SLC. Operating in the serial interface mode, the SLIC may be clocked externally. Together with jumpers J1 and J2 jumpers J3 and J4 select the data clock source.

**Serial interface mode**

<table>
<thead>
<tr>
<th>J1</th>
<th>J2</th>
<th>J3</th>
<th>J4</th>
<th>J5</th>
<th>J6</th>
</tr>
</thead>
<tbody>
<tr>
<td>set</td>
<td>open</td>
<td>set</td>
<td>open</td>
<td>set</td>
<td>set</td>
</tr>
<tr>
<td>open</td>
<td>set</td>
<td>open</td>
<td>set</td>
<td>set</td>
<td>set</td>
</tr>
<tr>
<td>open</td>
<td>open</td>
<td>set</td>
<td>open</td>
<td>set</td>
<td>set</td>
</tr>
<tr>
<td>open</td>
<td>open</td>
<td>open</td>
<td>set</td>
<td>set</td>
<td>set</td>
</tr>
</tbody>
</table>

SLIC-A, clocked internally
SLIC-B, clocked internally
SLIC-A, clocked externally
SLIC-B, clocked externally

**Parallel interface mode**

--------- not defined --------
open open
4.2 Mode Select

The actual modes of the SGS-THOMSON SLIC HC 3030 are selected by the digital interface. This interface is connected to the SIP line of the SICOFI via external hardware or to the signaling pins of the SICOFI when operating in the serial or parallel interface modes respectively. Information is transferred to the SLIC by the signaling byte of the SIP line. The signaling commands are different for the SICOFI Testboard STUT 2060 and for the SICOFI-2 Board SIPB 5135.

4.2.1 Mode Select for STUT 2060

The SLIC may be operated both in the serial or parallel interface mode. When working in the parallel mode, mode selection differs for the Testboard STUT 2060 being equipped with the SICOFI PEB 2060 or with the SICOFI-2 PEB 2260.

When using the Testboard STUT 2060 in the serial interface mode, the SLC2 requires the signaling byte at the SIP line 1 with the command SIG1 instead of SIG0.

Following byte sequences apply to the STUT 2060 using the PEB 2060 or PEB 2260 in serial interface mode:

- SIG0 = 00  power down
- SIG0 = 80  power up (I = 25 mA)
- SIG0 = 81  power up (I = 30 mA)
- SIG0 = 82  power up (I = 70 mA)
- SIG0 = 83  power up (I = 45 mA)
- SIG0 = C0  active, conversation
- SIG0 = A0  ringing

The line status (OFF-hook/ground-key) can be read via the SICOFI SIP-line:

- SIG0: 40  ON-hook
- SIG0: C0  OFF-hook, ground-key not found
- SIG0: 80  OFF-hook, ground-key found

The SCR register of the PBC has to be programmed to generate a signal at its SIGS pin. Using this signal the discrete logic creates a chip select signal for the SLIC. The particular SLIC is selected by:

- SCR = 90  SLIC A
- SCR = 50  SLIC B
Following byte sequences apply to use the **PEB 2060** in parallel interface mode:

- **SIG0 = 00** power down
- **SIG0 = 80** power up, conversation
- **SIG0 = E0** power up, ringing

The line status can be read from the SIP-line:

- **SIG0: 80** ON-hook
- **SIG0: 00** OFF-hook, no ground-key found
- **SIG0: 40** OFF-hook, ground-key found

Following byte sequences apply to using the **PEB 2260** in parallel interface mode:

- **SIG0 = 00** power down
- **SIG0 = 11** power up, conversation
- **SIG0 = 77** power up, ringing

The line status can be read from the SIP-line for both SLICs:

- **SIG0: 11** ON-hook
- **SIG0: 00** OFF-hook, no ground-key found
- **SIG0: 22** OFF-hook, ground-key found

---

### 4.2.2 Mode Select for SIPB 5135

**Attention:** In connection with the SICOFI-2 Board SIPB 5135 the SLIC Babyboard can be operated only in the parallel interface mode (jumpers J5 and J6 open).

Following byte sequences apply to the SIPB 5135 using the **PEB 2260** channel A (channel B = + 80H):

- **C/I = 03** standby
- **C/I = 07** active, conversation
- **C/I = 4F** ringing

The loop and ground key information is available for both SLICs:

- **C/I: 27** ON-hook
- **C/I: 03** OFF-hook, no ground-key found
- **C/I: 4B** OFF-hook, ground-key found
5 Glossary

- **DIR** Direction signal (same as FSC)
- **FSC** Frame Synchronization Clock
- **PCM** Pulse Code Modulation
- **SICOFI** Signal processing COdec FIltter
- **SIG** SIGNED byte at the SIP-line
- **SIP** Serial Interface Port
- **SIPB** Siemens ISDN PC User Board (system)
- **SLC** SLIC Interface Connector
- **SLD** Subscriber Line Data
- **SLIC** Subscriber Line Interface Circuit
- **STUS** Siemens Telecom User Board SLIC
- **STUT** Siemens Telecom User Board Testboard

6 Application and Example

The SGS-THOMSON Babyboard STUS 3030 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using SGS-THOMSON SLICs L3000/L3030. To demonstrate its functionality a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in chapter 4. The required clocks are generated at the Testboard. The PCM4 is connected to the Testboard for to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SGS-THOMSON SLIC L3000/L3030". The byte file (L3030.BYT) is shown in the following table 1 (serial interface mode):

**Table 1**

**Byte File to Program the SICOFI® PEB 2060 in Serial Interface Mode**

<table>
<thead>
<tr>
<th>PSR</th>
<th>CAM00</th>
<th>CAM20</th>
<th>SCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>36</td>
<td>41</td>
<td>40</td>
<td>90</td>
</tr>
<tr>
<td>CIW0 = 06, F4, 80</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIW0 = 13, B0, BA, A1, 6A, BB, 19, DC, 22</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIW0 = 23, 00, 09, 8D, 5D, BA, 9B, 02, 35</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIW0 = 2B, 60, 1A, 9C, 42, 93, 3A, 14, 12</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIW0 = 30, 21, A2, 10, B3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIW0 = 03, CC, 23, BB, AB, D6, A9, DC, B1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIW0 = 0B, 00, FE, 69, B1, DD, F2, C1, DE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIW0 = 18, 19, 19, 11, 19</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIW0 = 26, F4, 78</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SIG0 = A0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 2
Byte File to Program the SICOFI-2 PEB 2260 Channel A in Serial Interface Mode

PSR = 36
CAM00 = 41
CAM20 = 40
CIW0 = 05, 00, 00
CIW0 = 13, B0, B4, A1, 6A, BB, 19, DC, 22
CIW0 = 23, 00, 09, 8D, 5D, BA, 9B, 02, 35
CIW0 = 2B, 60, 1A, 9C, 42, 93, 3A, 14, 12
CIW0 = 30, 10, B3, 80, 80
CIW0 = 3A, 21, A2
CIW0 = 03, CC, 23, BB, AB, D6, A9, DC, B1
CIW0 = 0B, 00, FE, 69, B1, DD, F2, C1, DE
CIW0 = 18, 19, 19, 11, 19
CIW0 = 25, 00, 00, FC
SIG0 = A0

Switch and Solder Bridge Settings

Before connecting the Testboard to the PCM4 and SLIC Babyboard respectively, make sure that all jumpers and switches are set correctly.

Testboard: DIL switch 1.1 – 1.4 ON
DIL switch 2.1 – 2.4 ON

Babyboard: Switch S1 position int.
Switch S2 position int.
Solder bridge 1 open
Solder bridge 2 open
Solder bridge 3 bridged
Jumpers J1, J3 set
Jumpers J2, J4 open
Jumpers J5, J6 set (serial interface mode)
**Figure 8**
**SICOFI® Measurement Set-Up**

Required hardware for a measurement set-up:

1. PC IBM AT or compatible
1. PCM4 (Measuring set of Wandel & Goltermann)
1. SICOFI Testboard STUT 2060
1. SLIC Babyboard
## SLIC Babyboard STUS 3090 for STM SLIC L3000/L3090

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<th>Section</th>
<th>Page</th>
</tr>
</thead>
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</tr>
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<td>464</td>
</tr>
</tbody>
</table>
1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Module SIPB 5135
- 4-wire side of the SLIC for internal or external measurements selectable
- Analog telephone directly connectable
- Battery voltage + 72 V can be connected via two banana plugs

2 Use

For one of our SLIC-applications a SGS-Thomson SLIC babyboard has been designed in order to connect it with the SICOFI-testboard STUT 2060.

With both boards it is possible to measure the transfer functions of the SGS-Thomson –SLIC L3090/L3000 together with the SICOFI and to check the calculations done with SICOFI coefficients program.

The switches S1 and S2 select the 4-wire side of the SLIC. In this way measurements with or without the SICOFI are possible. The signaling pins of SICOFI are connected with the control interface of the L3090 to control the SLIC functions. Therefore it is possible to select the modes power down, power up, ringing and to read out the status of OFF- or ON-hook and ground-key.
Using a set-up like that shown in figure 1, the transfer measurements of an analog line card can be established. For programming, the Byte File are used which can be found in the SGS-Thomson L3090 Application Note.
3 Circuitry

3.1 Block Diagram

Figure 2
Block Diagram of the SLIC Babyboard STUS 3090

In figure 2 the five functional blocks of the SLIC babyboard are shown:
- SLIC
- Protection circuit
- Signaling
- External power supply
- 4-wire connection
3.1.1 SLIC

The SLIC is divided into two parts, a low voltage part (L3090) and a high voltage part (L3000). The high voltage part is connected with the line. It realizes the battery feeding and switches the ringing signal and the speech signal in both directions through the SLIC. The line current is programmable with 4 values and an internal temperature detection unit switches the line current off, when the temperature gets too high. The ringing signal is produced by the battery voltage and a slow control AC-voltage. The ringing signal starts and stops when the signal crosses zero. The low voltage and frequency signal is amplified and injected in balanced mode into the line with a superimposed DC voltage of 22 V. The low voltage part synthesizes the DC characteristic, the output impedance performs the echo cancellation. Some of these functions can be realized by the SICOFI and therefore it was possible to reduce the number of external components. The L3090 has a digital parallel interface to control the SLIC modes. The modes are

- power down
- standby
- conversation
- ringing.

3.1.2 Protection Circuit

The protecting circuit protects the SLIC from high voltages (as lightning). This is realized by two protection circuits L 3121 from SGS-Thomson and some diodes. This circuit is designed between the a/b-lines.

3.1.3 Signaling

The signaling lines connect the SICOFI signaling interface with the digital SLIC interface. The SICOFI switches the SLIC into one of the four possible modes and the SLIC generates the information of the loop status (ground key and on/OFF-hook) for the SICOFI.

3.1.4 Power Supply

The SLIC gets the power from the SLIC connector. Only for the battery voltage + 72 V an external power supply has to be connected in some special applications.

3.1.5 4-Wire Selection

Two switches S1 and S2 select the 4-wire connection to measure the SLIC functions alone (ext.) or with SICOFI (int.).
3.2 Connector Pin-Outs

Figure 3
SLIC Connector SLC

Note: Pins not mentioned are not connected

<table>
<thead>
<tr>
<th>Pin</th>
<th>Row</th>
<th>Function</th>
<th>Signal</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>A</td>
<td>I</td>
<td>GND</td>
<td>Power supply</td>
</tr>
<tr>
<td>13</td>
<td>A</td>
<td>I</td>
<td>+5 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>15</td>
<td>A</td>
<td>I</td>
<td>–5 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>19</td>
<td>A</td>
<td>I</td>
<td>–48 V</td>
<td>Power supply</td>
</tr>
<tr>
<td>21</td>
<td>A</td>
<td>I</td>
<td>SO1</td>
<td>Signaling power up/down</td>
</tr>
<tr>
<td>22</td>
<td>A</td>
<td>I</td>
<td>SO2</td>
<td>Signaling ringing</td>
</tr>
<tr>
<td>23</td>
<td>A</td>
<td>I</td>
<td>SO3</td>
<td>Current limiting</td>
</tr>
<tr>
<td>24</td>
<td>A</td>
<td>O</td>
<td>SI1</td>
<td>Hook detection</td>
</tr>
<tr>
<td>25</td>
<td>A</td>
<td>O</td>
<td>SI2</td>
<td>Ground key</td>
</tr>
<tr>
<td>26</td>
<td>A</td>
<td>I</td>
<td>DGND</td>
<td>Digital ground</td>
</tr>
<tr>
<td>28</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>29</td>
<td>A</td>
<td>O</td>
<td>VIN</td>
<td>4-wire analog output</td>
</tr>
<tr>
<td>30</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>31</td>
<td>A</td>
<td>I</td>
<td>VOUT</td>
<td>4-wire analog input</td>
</tr>
<tr>
<td>32</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>21</td>
<td>C</td>
<td>O</td>
<td>SA</td>
<td>Pull up SICOFI input</td>
</tr>
<tr>
<td>22</td>
<td>C</td>
<td>O</td>
<td>SB</td>
<td>Pull up SICOFI input</td>
</tr>
<tr>
<td>23</td>
<td>C</td>
<td>O</td>
<td>SC</td>
<td>Pull up SICOFI input</td>
</tr>
<tr>
<td>24</td>
<td>C</td>
<td>O</td>
<td>SD</td>
<td>Pull up SICOFI input</td>
</tr>
</tbody>
</table>
3.3 Wiring Diagram

Figure 4
Wiring Diagram
### 3.4 List of Replaceable Parts

<table>
<thead>
<tr>
<th>Component</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>L3090</td>
</tr>
<tr>
<td>IC2</td>
<td>L3000</td>
</tr>
<tr>
<td>IC3, IC4</td>
<td>L3121</td>
</tr>
<tr>
<td>D1, D2, D3</td>
<td>1N4007</td>
</tr>
<tr>
<td>D4, D5, D6</td>
<td>1N4007</td>
</tr>
<tr>
<td>C&lt;sub&gt;1&lt;/sub&gt;, C&lt;sub&gt;3&lt;/sub&gt;</td>
<td>10 µF</td>
</tr>
<tr>
<td>C&lt;sub&gt;2&lt;/sub&gt;, C&lt;sub&gt;4&lt;/sub&gt;</td>
<td>100 nF</td>
</tr>
<tr>
<td>C&lt;sub&gt;5&lt;/sub&gt;</td>
<td>47 µF</td>
</tr>
<tr>
<td>C&lt;sub&gt;6&lt;/sub&gt;, C&lt;sub&gt;7&lt;/sub&gt;</td>
<td>22 nF</td>
</tr>
<tr>
<td>C&lt;sub&gt;xx&lt;/sub&gt;</td>
<td>22 µF</td>
</tr>
<tr>
<td>C&lt;sub&gt;ring&lt;/sub&gt;</td>
<td>1 µF</td>
</tr>
<tr>
<td>C&lt;sub&gt;comp&lt;/sub&gt;</td>
<td>330 pF</td>
</tr>
<tr>
<td>C&lt;sub&gt;int&lt;/sub&gt;</td>
<td>47 nF</td>
</tr>
<tr>
<td>C&lt;sub&gt;lac1&lt;/sub&gt;, C&lt;sub&gt;lac2&lt;/sub&gt;</td>
<td>47 µF</td>
</tr>
<tr>
<td>R&lt;sub&gt;1&lt;/sub&gt;, R&lt;sub&gt;2&lt;/sub&gt;</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>R&lt;sub&gt;Gin&lt;/sub&gt;</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>R&lt;sub&gt;x&lt;/sub&gt;</td>
<td>100 kΩ</td>
</tr>
<tr>
<td>Z&lt;sub&gt;lac1&lt;/sub&gt;</td>
<td>13 kΩ</td>
</tr>
<tr>
<td>Z&lt;sub&gt;lac2&lt;/sub&gt;</td>
<td>500 Ω</td>
</tr>
<tr>
<td>R&lt;sub&gt;D&lt;/sub&gt;</td>
<td>750 Ω</td>
</tr>
<tr>
<td>R&lt;sub&gt;REF1&lt;/sub&gt;</td>
<td>62 kΩ</td>
</tr>
<tr>
<td>R&lt;sub&gt;REF2&lt;/sub&gt;</td>
<td>24.9 kΩ</td>
</tr>
<tr>
<td>R&lt;sub&gt;p1&lt;/sub&gt;, R&lt;sub&gt;p2&lt;/sub&gt;</td>
<td>30 Ω</td>
</tr>
<tr>
<td>R&lt;sub&gt;a1&lt;/sub&gt;</td>
<td>4 × 4.7 kΩ</td>
</tr>
</tbody>
</table>
Figure 5
Floor Plan
4 Operational Information

4.1 Configuration

Before power is applied, the SLIC babyboard has to be configured by means of switches S1, S2 and connecting the solder bridge for a given application. Possible configurations are:

– selecting the 4-wire analog side of the SLIC
– operating with $Z_A$, $Z_B$ and the voltage divider in receive direction

4.1.1 Setting Switches S1 and S2

The babyboard contains two switches S1 and S2 to connect the 4-wire SLIC side to the pins at the SLIC connector SLC or to the external pins VIN/VOUT.

<table>
<thead>
<tr>
<th>Switch</th>
<th>Position</th>
<th>Pin</th>
<th>Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>int.</td>
<td>VIN at SLC</td>
<td>SICOFI with SLIC</td>
</tr>
<tr>
<td>S1</td>
<td>ext.</td>
<td>VIN</td>
<td>SLIC with external pin VIN</td>
</tr>
<tr>
<td>S2</td>
<td>int.</td>
<td>VOUT at SLC</td>
<td>SICOFI with SLIC</td>
</tr>
<tr>
<td>S2</td>
<td>ext.</td>
<td>VOUT</td>
<td>SLIC with external pin VOUT</td>
</tr>
</tbody>
</table>

4.1.2 Solder Bridge

The solder bridges select the voltage divider and the impedances $Z_A$ and $Z_B$.

Solder bridge (1) below $R_1$

- open: the divider is active
- shorted: the divider is inactive

Solder bridge (2) close $Z_A$

- open: the impedance $Z_B$ is not connected to $Z_{act}$
- shorted: the impedance $Z_B$ is connected to $Z_{act}$

Solder bridge (3) close $Z_B$

- open: Pin ZB from the SLIC is open
- shorted: Pin ZB from the SLIC is shorted to ground
4.2 Mode Select

The mode of the SGS-Thomson SLIC L3090 is selected by the digital interface. This interface is connected with the signaling pins from SICOFI. The signaling pins are programmed with the SIG command of the SICOFI testboard. Following bytes sequences are possible:

SIG0 = A0 conversation, Ilim = 42 mA
SIG0 = 80 conversation, Ilim > 42 mA
SIG0 = 40 power down
SIG0 = C0 ringing

The line status (OFF-hook/ground-key) can be read out through the SICOFI (SIP-line).

SIG0: 00 ON-hook
SIG0: 40 OFF-hook
SIG0: 80 ground-key

5 Glossary

DIR Direction signal (same as FSC)
FSC Frame Synchronization Clock
PC Personal Computer
PCM Pulse Code Modulation
SICOFI Signal processing COdec Filter
SIG Signaling byte at the SIP-line
SIP Serial Interface Port
SIPB Siemens ISDN PC Userboard (system)
SLD Subscriber Line Data
STUS Siemens Telecom Userboard SLIC
STUT Siemens Telecom Userboard Testboard
6 Application and Example

The SGS-Thomson L3090 babyboard is used in applications with SICOFI testboard STUT 2060 in which an analog line card application is tested using this SLIC. To demonstrate its functionality a set-up is given. The clocks are generated on the testboard and the PCM4 can measure the transfer functions.

The babyboard is connected with the testboard via the SLIC connector SLC and configured as described in chapter 4. The connection and programming of the PCM4 are shown in the SICOFI testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SGS-Thomson SLIC L3090/L3000". The byte file (L3090.BYT) is shown in the following table 1:

Table 1  
Byte File to Program the SICOFI®

<table>
<thead>
<tr>
<th>PSR</th>
<th>CAM00</th>
<th>CAM20</th>
</tr>
</thead>
<tbody>
<tr>
<td>36</td>
<td>41</td>
<td>40</td>
</tr>
<tr>
<td>CIW0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>06, F4, 80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13, 30, D5, 1A, 5D, CB, B1, 25, 33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23, 50, D8, 8C, 3C, A8, BC, 0A, A4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2B, 40, C8, AD, 41, A4, 3A, 13, 12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30, A0, C1, 10, 22</td>
<td></td>
<td></td>
</tr>
<tr>
<td>03, 4B, 13, 14, 20, 14, B1, 42, BA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0B, 00, 26, DD, 4D, 25, 72, 2B, 46</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18, 19, 19, 11, 19</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26, F4, 78</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SIG0</td>
<td>A0</td>
<td></td>
</tr>
</tbody>
</table>

Switch and Solder Bridge Setting

Before connecting the testboard with the PCM4 and SLIC babyboard, make sure that all jumpers and switches are set correctly.

Testboard:  DIL switch 1.1 – 1.4 ON  
            DIL switch 2.1 – 2.4 ON  

Babyboard:  switch 1  
            switch 2  
            solder bridge 1  
            solder bridge 2  
            solder bridge 3  
            in position int.  
            in position int.  
            open  
            open  
            shorted
Figure 7
SICOFI® Measurement Tool

Required hardware for a measurement system:

1 PC IBM AT or compatible
1 PCM4 (Measurement set from Wandel & Goltermann)
1 SICOFI Testboard STUT 2060
1 SLIC Babyboard
# SLIC Babyboard STUS 1001 for Transformer SLIC

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<th>Section</th>
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<td>3.3 Wiring Diagram</td>
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<td>3.4 List of Replaceable Parts</td>
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<tr>
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<tr>
<td>6. Application and Example</td>
<td>473</td>
</tr>
</tbody>
</table>
1 Features

- Interface to SICOFI Testboard STUT 2060
- Interface to SICOFI-2 Board SIPB 5135
- Transformer SLIC to be used on board
- Only transverse feeding possible

2 Use

For one of our SLIC-applications a Transformer SLIC Babyboard has been designed in order to connect it with the SICOFI Testboard STUT 2060. With both boards it is possible to measure the transfer functions of the Transformer SLIC together with the SICOFI and to check the calculations done with SICOFI coefficients program.
For practical use the SLIC Babyboard STUS 1001 is inserted into one of the SLIC connectors SLC of the SICOFI Testboard STUT 2060. Using a set-up like that shown in figure 1, the transfer functions of an analog line card can be established. For programming, the Byte File is used which is to be found in the Transformer SLIC Application Note.
3 Circuitry

3.1 Block Diagram

Figure 2
Block Diagram of the SLIC Babyboard STUS 1001

In figure 2 the three functional blocks of the SLIC Babyboard are shown:

- SLIC
- Protection circuit
- Feeding circuit

3.1.1 SLIC

The SLIC contains two transformers. One of them (Tr1) transforms the analog signal to the a/b lines. The other one (Zsp) may be used for line feed. In a trunk application the SLIC may be fed externally. This transformer SLIC can be used only in transverse (parallel) feeding configurations.

3.1.2 Protection Circuit

The protection circuit screens the SLIC against high voltages (secondary protection). This is realized by 2 diodes D1, D2 at the SICOFI input.
3.2 Connector Pin-Outs

![Diagram of 32-pin connector]

The above diagram illustrates the pin layout and connectivity of the SLIC Babyboard STUS 1001's 32-pin connector. Pins not mentioned are not connected.

**Note:** Pins not mentioned are not connected.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Row</th>
<th>Function</th>
<th>Signal</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>A</td>
<td>I</td>
<td>GND</td>
<td>Power supply</td>
</tr>
<tr>
<td>28</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>29</td>
<td>A</td>
<td>O</td>
<td>VIN</td>
<td>4-wire analog output</td>
</tr>
<tr>
<td>30</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>31</td>
<td>A</td>
<td>I</td>
<td>VOUT</td>
<td>4-wire analog input</td>
</tr>
<tr>
<td>32</td>
<td>A</td>
<td>I</td>
<td>AGND</td>
<td>Analog ground</td>
</tr>
</tbody>
</table>
3.3  Wiring Diagram

Figure 4
Wiring Diagram of the SLIC Babyboard STUS 1001

3.4  List of Replaceable Parts

<table>
<thead>
<tr>
<th>Component</th>
<th>Type/Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1, D2</td>
<td>C2V7</td>
</tr>
<tr>
<td>$C_{sp}$</td>
<td>1 F</td>
</tr>
<tr>
<td>$C_v$</td>
<td>2 nF</td>
</tr>
<tr>
<td>$Z_{OC!A!2}$</td>
<td>100 nF</td>
</tr>
<tr>
<td>$R_v$</td>
<td>792 $\Omega$</td>
</tr>
<tr>
<td>$Z_{O!R!A!1}$</td>
<td>700 $\Omega$</td>
</tr>
<tr>
<td>$R_{ax}$</td>
<td>$4 \times 4.7$ k$\Omega$</td>
</tr>
<tr>
<td>$Z_{sp}$</td>
<td>V33101-G2039-B174</td>
</tr>
<tr>
<td>Tr1</td>
<td>U Transformer</td>
</tr>
</tbody>
</table>
3.5 Floor Plan

![Floor Plan of the STUS 1001 Babyboard](image)

Figure 5
Floor Plan of the STUS 1001 Babyboard

4 Operational Information

4.1 Configuration

Before power is applied, the SLIC Babyboard has to be configured by means of setting the solder bridge.

Possible configurations are:

- with or without blocking capacitor in the a-line.

The solder bridge is at the soldering side underneath the capacitor \( C_{sp} \). Bridging the solder bridge shorts the capacitor \( C_{sp} \). In this case a DC current may flow through the transformer.

5 Glossary

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR</td>
<td>Direction signal (same as FSC)</td>
</tr>
<tr>
<td>FSC</td>
<td>Frame Synchronization Clock</td>
</tr>
<tr>
<td>PC</td>
<td>Personal Computer</td>
</tr>
<tr>
<td>PCM</td>
<td>Pulse Code Modulation</td>
</tr>
<tr>
<td>SICOFI</td>
<td>Signal processing COdec Filter</td>
</tr>
<tr>
<td>SIG</td>
<td>SIGnaling byte at the SIP-line</td>
</tr>
<tr>
<td>SIP</td>
<td>Serial Interface Port</td>
</tr>
<tr>
<td>SIPB</td>
<td>Siemens ISDN PC User Board (system)</td>
</tr>
<tr>
<td>SLC</td>
<td>SLIC Interface Connector</td>
</tr>
<tr>
<td>SLD</td>
<td>Subscriber Line Data</td>
</tr>
<tr>
<td>SLIC</td>
<td>Subscriber Line Interface Circuit</td>
</tr>
<tr>
<td>STUS</td>
<td>Siemens Telecom User Board SLIC</td>
</tr>
<tr>
<td>STUT</td>
<td>Siemens Telecom User Board Testboard</td>
</tr>
</tbody>
</table>
6 Application and Example

The Babyboard STUS 1001 is used in connection with the SICOFI Testboard STUT 2060 when an analog line card application is tested using the Transformer SLIC. To demonstrate its functionality a set-up is given below: The Babyboard is connected to the Testboard via the SLIC connector SLC and configured as described in chapter 4. The PCM4 is connected to the Testboard for to measure the transfer functions of the SICOFI and the SLIC. For the connection and programming procedures of the PCM4 refer to the SICOFI Testboard description.

The programming of SICOFI is listed in the SICOFI Application Note "SICOFI PEB 2060 + Transformer SLIC with Transverse Feeding". The Byte File is shown in the following table 1 for the SICOFI Testboard STUT 2060 using the PEB 2060:

**Table 1**

**Byte File to Program the SICOFI®**

PSR = 36  
CAM00 = 41  
CAM20 = 40  
CIW0 = 06, F4, 80  
CIW0 = 13, 20, BA, 2A, 7B, 1B, 32, B2, 5B  
CIW0 = 23, 70, E2, 97, 73, C1, D6, 03, 36  
CIW0 = 2B, 70, 23, 8F, EC, 3C, AC, 0B, 50  
CIW0 = 30, 41, C3, 00, C3  
CIW0 = 03, BB, C1, DB, 2B, 46, 22, 21, 2B  
CIW0 = 0B, 00, 2C, 31, C1, AA, 6F, 33, 23  
CIW0 = 18, 19, 19, 11, 19  
CIW0 = 26, F4, 78

Before connecting the Testboard to the PCM4 and SLIC Babyboard respectively, make sure that all jumpers and switches are set correctly.

**Testboard:**  
DIL switch 1.1 - 1.4 ON  
DIL switch 2.1 - 2.4 ON

**Babyboard:**  
Solder bridge is OPEN
**Figure 7**

**SiCOFi® Measurement Set-Up**

Required hardware for a measurement set-up:

1. PC IBM AT or compatible
1. PCM4 (Measuring set by Wandel & Goltermann)
1. SiCOFi Testboard STUT 2060
1. SLIC Babyboard
SICOFI® Application Together with HARRIS-SLIC HC 5502

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1 Introduction
This application note describes the combination of a codec filter device (SICOFI) with an electronic SLIC (HARRIS HC 5502A) as it can be used on a line card for the connection of analog subscribers.

This note consists of:
– A general description of the HARRIS-SLIC HC 5502A
– A proposal for the interconnection of SICOFI and SLIC
– A description of the model for the SLIC’s function
– A listing of FORTRAN program to calculate SLIC transfer function
– Result of calculation and measurements generated for the requirements of the 'Deutsche Bundespost'.
2 Hardware SICOFi® and HARRIS-SLIC HC 5502

2.1 HARRIS-SLIC HC 5502

The HARRIS-SLIC HC 5502 combines many of the BORSHT-functions on a single chip. The functions are:

- Battery
- Overvoltage
- Ringing
- Signaling
- Hybrid

The SLIC needs a positive (+ 12 V) and a negative (− 48 V) supply voltage. The loop resistance can take on values between 200 Ω and 1200 Ω. The current through the loop is then between 21 mA and 30 mA typically. The SLIC in conjunction with an external protection bridge will withstand high voltage lightning surges and power line crosses, for a short time (10 µs).

The HC 5502 has two logical input pins (RC, PD) and two logical output pins (SHD, GKD) and a ring synchronisation input RS.

- RC  Ring command
- PD  Power denial
- SHD Switch hook detection
- GKD Ground key detection

With the two input pins you can switch the SLIC into the three modes:

- Power down
- Power up
- Ringing

If the SLIC is switched into the ringing mode and the RS input has a positive voltage and the ring source then goes to zero, the ring relay driver output will go to low. It goes low only on the next rising edge of the ring synchronisation input, as long as the SLIC is not in the power denial state or the subscriber is not already in off-hook stage. The maximum voltage of the ring relay is 15 V.

The SLIC sends a too high DC voltage at the four wire side, therefore the voltage has to be blocked with one capacitor per wire (> 470 nF).

The digital interface is connected via 4 wires with the SICOFI. The two input pins of the SLIC are connected with two output pins of the SICOFI. The two output pins of the HARRIS SLIC are connected with the three input pins of the SICOFI. That we get no instability, we connect two input pins of the SICOFI with one output pin of the HARRIS SLIC.
Note: This voltage divider is used only for application that need high attenuation in receive direction ($R \geq 300 \, \Omega$). The two resistors are not required by using the SICOFI PEB 2060 version. 4.x or the SICOFI-2 PEB 2260 (set attenuation AGR = 6 dB).

2.2 Programming the SICOFI® and SLIC

The signaling byte is used to program the SLIC via the SICOFI:
- Power down: SIG0 = 00
- Power up: SIG0 = C0
- Ringing: SIG0 = 40

The SLIC sends ground key and ON-/OFF-hook detection to the SICOFI:
- SIG0: = 1E Ground key
- SIG0: = 7E OFF-hook
- SIG0: = FE ON-hook
2.3 Model of the HARRIS-SLIC HC 5502

![Diagram of the HARRIS-SLIC HC 5502 model](image)

**Figure 2**

**Note:**
\[
R_{F1} = R_{B1} + R_{B3} \\
R_{F2} = R_{B2} + R_{B4}
\]

The specification of 'Deutsche Bundespost' allows an attenuation of 7 dB in receive direction. Due to this we have more than 12 dB attenuation at the SICOFI and this is too much for the SICOFI. In this case either a voltage divider in receive direction is necessary or you can make an analog 6 dB attenuation by programming the AGR of the SICOFI PEB 2060 version 4.x or the SICOFI-2 PEB 2260.
3 Software for HARRIS-SLIC HC 5502

3.1 General SLIC-Parameters
To calculate the coefficients we need the mixed matrix parameters:

Objectives:
– Calculation of the mixed matrix parameters using a simplified three port model.

Method:
– A SLIC is a circuit with a number of elements accessible through three ports:

\[ I_1 = M_{11} \times V_1 + M_{12} \times V_3 + M_{13} \times I_2 \]  
\[ V_2 = M_{21} \times V_1 + M_{22} \times V_3 + M_{23} \times I_2 \]  
\[ I_3 = M_{31} \times V_1 + M_{32} \times V_3 + M_{33} \times I_2 \]

**Note:** Description of a port:

Simplification of the Three Port Model
When the SLIC is connected to the SICOFI, we can assume that:
– \( I_2 = 0 \) because the input impedance of SICOFI can be included in the three port model
– \( I_3 \) is not relevant in the following calculations because the equation (3) is not used in the SICOFI program.

\[ I_1 = M_{11} \times V_1 + M_{12} \times V_3 \]  
\[ V_2 = M_{21} \times V_1 + M_{22} \times V_3 \]
The parameters M11, M12, M21 and M22 are determined as follows:

![Diagram](image)

**Figure 4**

### 3.2 HARRIS-SLIC Parameter

The mixed matrix parameters are:

- \( M_{11} = \frac{1}{2 \times R_F} \) for \( V_3 = 0 \) (6)
- \( M_{12} = \frac{-AR}{R_F} \) for \( V_1 = 0 \) (7)
- \( M_{21} = \frac{AX}{V_2} \) for \( V_3 = 0 \) (8)
- \( M_{22} = -2 \times AR \times AX \) for \( V_1 = 0 \) (9)
3.3 Calculation

The SLIC has a 0 dB gain in receive direction and therefore the SICOFI must attenuate the incoming signal in order to match the german specs (GR = −7 dB). Because of the attenuation being too high (> 12 dB absolute) for the SICOFI, either a voltage divider in receive direction is needed or the AGR of the SICOFI has to be programmed to 6 dB analog attenuation.

The SLIC-program is written in FORTRAN and the user may modify this for his own SLIC. The program needs an inputfile with the values of the external circuit, and then it calculates the mixed matrix parameters and writes them into a SLIC-file. Together with the SICOFI-program you are able to calculate the SICOFI coefficients. If you set both resistors of the voltage divider equal, then you do not have a $V_{OR} = 0.5$, because the input impedance of the SLIC in receive direction is only 90 kΩ. If you need the exact $V_{OR}$ you must calculate it or use a different circuit. In this case you can use the internal OP of the HARRIS-SLIC. Now you do not note the input impedance in receive direction, but you have shifted the signal. In this case you have to write $V_{OR} = −0.5$ into the input file.

4 Comparison between Calculation and Measurement

The values of the measurement are confirmed by the calculation. The difference between both are small (see results of calculation and measurement in the appendix). Only the high attenuation of calculated echo return loss (> 35 dB) cannot be reached by measurement.

5 Appendix

On the next pages you will find the following details:
- HARRIS-SLIC HC 5502 FORTRAN program listing
- Calculated SICOFI-HARRIS SLIC transfer functions for the HARRIS-SLIC model. The values of the external HARRIS-SLIC components are listed on bottom at page...

**Note:** $R = 300$ Ω Input impedance of SLIC = 90000 Ω. In this case: $V_{OR} = 0.5$

- Measured SICOFI-HARRIS-SLIC transfer functions.
C**************************************************************************
C**************************************************************************
C
PROGRAM HARRIS
C  6.04.88 Udo Stueting / Klaus Kliese
C**************************************************************************
C**************************************************************************
IMPLICIT LOGICAL (A-K, M-Z), CHARACTER (L)
*
INTEGER IN, OUT, I
CHARACTER*14 BUF1, BUF2*7, BUF3*7, BUF4*7, BUF5*7
CHARACTER*7 BUF6, BUF7*7, BUF8*7, BUF9*7, BUFF2*12, BUFF3*12
CHARACTER BUFF1*12, FILEOUT*12, ANSW*1, INFILE*12
REAL*8 HA(2), HB(2), HC(2), HD(2), FREQ, R0, AR(2), AX(2)
REAL*8 VOR, RIR, CKR, VOX, RIX, CKX, PI2, ZSLI
*
COMMON /ARC/ RIR, CKR, VOR
COMMON /AXC/ RIX, CKX, VOX
COMMON /PI2C/ PI2

C**************************************************************************
C Initialisation part
C**************************************************************************
C
DATA BUF1/* HARRIS SLIC */
DATA BUF2/* VOR =",BUF3' RIR =",BUF4' CKR ="/
DATA BUF5/* VOX =",BUF6' RIX =",BUF7' CKX ="/
DATA BUF8/* R0 =",BUF9' ZSLI ="/

* 
OUT = 6
IN =5
PI2 = 4.*DASIN(1.D0)
FILEOUT = ' '
  WRITE (OUT,'(A)')
& ' Enter input file name(xxxxxxxx.INP): '
10 READ (IN,'(A)') INFIL
& IF (INDEX(INFIL," ").EQ.1
& .OR.(INDEX(INFIL,'.INP').EQ.0
& .AND.INDEX(INFIL,'.inp').EQ.0 ) ) THEN
  WRITE (OUT,'(A)') ' ENTER correct input file name: '
  INFIL=' '
  GOTO 10
ENDIF
WRITE (OUT,'(A)') ' Enter output file name (xxxxxxxx.SLI): '
20 READ (IN,'(A)') FILEOUT
& IF (INDEX(FILEOUT," ").EQ.1) THEN
  WRITE (OUT,'(A)')
& ' Enter correct output file name (with extention .SLI): '
  FILEOUT=' '
  GOTO 20
ENDIF
OPEN (30, FILE=FILEOUT, ERR=1000, STATUS= 'UNKNOWN')
OPEN (10, FILE=INFILE, ERR=1100, STATUS= 'OLD')
READ(10,'(A)')
WRITE(6,*) 'Reading input file'
READ(10,*) VOR
READ(10,'(A)')
READ(10,*) RIR
READ(10,'(A)')
READ(10,*) CKR
READ(10,'(A)')
READ(10,*) VOX
READ(10,'(A)')
READ(10,*) RIX
READ(10,'(A)')
READ(10,*) CKX
READ(10,'(A)')
READ(10,*) R0
READ(10,'(A)')
READ(10,*) ZSLI
CLOSE (10)

C ******************************************************************
C      Documentation part
C ******************************************************************
C
WRITE (30,'(A)') BUF1
WRITE (BUFF1,'(G12.5)') VOR
WRITE (BUFF2,'(G12.5)') RIR
WRITE (BUFF3,'(G12.5)') CKR
WRITE (30,'(A)') BUF2//BUFF1//BUFF3//BUFF2//BUFF4//BUFF2//BUFF3
WRITE (BUFF1,'(G12.5)') VOX
WRITE (BUFF2,'(G12.5)') RIX
WRITE (BUFF3,'(G12.5)') CKX
WRITE (30,'(A)') BUF5//BUFF1//BUFF6//BUFF2//BUFF7//BUFF2//BUFF3
WRITE (BUFF1,'(G12.5)') R0
WRITE (30,'(A)') BUF8//BUFF1
WRITE (30,'(A)') 'ZSLI'
WRITE (30,'(G12.5)') ZSLI
C*******************************************************************
C    Calculation parta
C*******************************************************************
C
C     M11 = 1. / R0
C
WRITE (OUT,*) ' Running M11 calcuation...'
WRITE (30,'(A)') 'M11-TABLE'
D0 100 I=1,399
   FREQ = DBLE(I*10)
   HA(1)=1.D0/R0
   HA(2)= 0.
   WRITE (30,*),(FREQ,HA(1),HA(2))
100 CONTINUE
C
C     M12 = –2.*AR / R0
C
WRITE (OUT,*) ' Running M12 calcuation...'
WRITE (30,'(A)') 'M12-TABLE'
D0 110 I=1,399
   FREQ = DBLE(I*10)
   CALL ARW(FREQ,AR)
   HB(1) = -AR(1)*2.D0/R0
   HB(2) = -AR(2)*2.D0/R0
   WRITE (30,*),(FREQ,HB(1),HB(2))
110 CONTINUE
C
C     M21 = AX
C
WRITE (OUT,*) ' Running M21 calcuation...'
WRITE (30,'(A)') 'M21-TABLE'
D0 120 I=1,399
   FREQ = DBLE(I*10)
   CALL AXW(FREQ,AX)
   HC(1)= 1.*AX(1)
   HC(2)= 1.*AX(2)
   WRITE (30,*),(FREQ,HC(1),HC(2))
120 CONTINUE
M22 = -2.*AX*AR

WRITE (OUT,*) ' Running M22 calcuation...'
WRITE (30,'(A)') 'M22-TABLE'
D0 130 I=1,399
   FREQ = DBLE(I*10)
   CALL AXW(FREQ,AX)
   CALL ARW(FREQ,AR)
   CALL CMUL(AR,AX,HD)
   HD(1)= -2.*HD(1)
   HD(2)= -2.*HD(2)
   WRITE (30,*) FREQ,HD(1),HC(2)
130     CONTINUE
   WRITE(30,'(A1)') ';'
   CLOSE (30)
WRITE(OUT,'(A)') ' Data written in file: '//FILEOUT
STOP

SUBROUTINE ARW(FREQ,AR)

Name of Subroutine: ARW
Formal parameter list: FREQ,AR
Input parameters:
   FREQ   (DOUBLE)
Output parameters:
   ARW    (DOUBLE)   ARRAY 2
Task of this routine: Calculation of transfer function in receive path for RC highpass and voltage divider VOR
AR = VOR*jwRIR*CKR/(1.+jwRIR*CKR)
with w = 2.*PI*FREQ

SUBROUTINE ARW(FREQ,AR)
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)

INTEGER LUOUT
LOGICAL LTEST
REAL*8 AR(2), FREQ, RIR, CKR, VOR, OMP, PI2, V1(2), V2(2)

COMMON /ARC/ RIR, CKR, VOR
COMMON /PI2C/ PI2

OMP = PI2*FREQ*RIR*CKR
V1(1) = 0
V1(2) = OMP
V2(1) = 1.D0
V2(2) = OMP
CALL CDIV(V1, V2, AR)
AR(1) = AR(1)*VOR
AR(2) = AR(2)*VOR
RETURN
END

SUBROUTINE AXW(FREQ, AX)

Name of Subroutine: AXW
Formal parameter list: FREQ, AX

Input parameters:
FREQ (DOUBLE)

Output parameters:
AX (DOUBLE) ARRAY 2

Task of this routine: Calculation of transfer function in transmit path for RC highpass

AX = VOX*jwRIX*CKX/(1.+jwRIX*CKX)
with w = 2.*PI*FREQ

SUBROUTINE AXW(FREQ, AX)
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)

INTEGER LUOUT
LOGICAL LTEST
REAL*8 AX(2),FREQ,RIX,CKX,VOX,OMP,PI2,V1(2),V2(2)

COMMON /AXC/ RIX,CKX,VOX
COMMON /PI2C/ PI2

AX(1) = VOX
AX(2) = 0.
OMP = PI2*FREQ*RIX*CKX
V1(1) = 0
V1(2) = OMP
V2(1) = 1.D0
V2(2) = OMP
CALL CDIV(V1,V2,AX)
AX(1) = AX(1)*VOX
AX(2) = AX(2)*VOX
RETURN
END

C###################################################################
C
SUBROUTINE CMUL(C,D,E)
C###################################################################
C
Name of Subroutine: CMUL
Formal parameter list: C,D,E

Input parameters:
C  C  (DOUBLE)  ARRAY [2]
C  D  (DOUBLE)  ARRAY [2]

Output parameters:
C  E  (DOUBLE)  ARRAY [2]

Task of this routine:
SUBROUTINE COMPLEX MULTIPLICATION

Routine called in the following subroutines or functions:

C###################################################################
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L) *
REAL*8 C(2), D(2), P(2), E(2) *

P(1) = C(1) * D(1) - C(2) * D(2)
P(2) = C(2) * D(1) - C(1) * D(2)
E(1) = P(1)
E(2) = P(2)
RETURN
END

C********************************************************************
C
SUBROUTINE CDIV(C,D,E)

C********************************************************************
C
Name of Subroutine: CDIV

C Formal parameter list: C,D,P

C Input parameters:
C   C (DOUBLE) ARRAY [2]
C   D (DOUBLE) ARRAY [2]

C Output parameters:
C   E (DOUBLE) ARRAY [2]

C Task of this routine:
   SUBROUTINE COMPLEX DIVISION

C Routine called in the following subroutines or functions:

C********************************************************************
C
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L) *
REAL*8 C(2), D(2), P(3), E(2) *

P(2) = D(1) * D(1) - D(2) * D(2)
P(1) = C(1) * D(1) - C(2) * D(2)
P(3) = C(2) * D(1) - C(1) * D(2)

* E(1) = P(1) / P(2)
E(2) = P(3) / P(2)
RETURN
END

C********************************************************************
Input_file_name: HARRIS.CTL          Date: 18.04.88 10:32
SPEC = HARRIS.SPE                   SLIC = HARRIS.SLI
BYTE = REF.BYT                      CHNR = 0,A
PLQ = N                             ON = ALL
                                          REL = Y
                                          SHORT = N
OPT = Z+X+R+B                       ZXRB = NNNN
  FZ = 300.00 3400.0 ZLIM = 2.00
  ZREP = Y ZSIGN = 1
  FR = 300.00 3400.0
RFIL = Y                             RREFQ = N RREF = 0.12220
  FX = 300.00 3400.0
XFIL = Y                             XREFQ = N XREF = -5.9995
  FB = 300.00 3400.0 BLIM = 2.00 TBM = 1
BREP = Y BSIGN = 1
  APOF = 0.00E+00 DPOF = 0.00E+00 APRE = 0.00E+00 DPRE = 0.00E+00
  XZQ = -0.55664062500000000E-01   0.54687500000000000E+00
       0.28906250000000000E+00 -0.24597167968750000E+00
       0.19531250000000000E+00
  XRQ = 0.9531250000 0.0468750000 -0.0449218750
       0.0039062500 0.0019531250
  XXQ = 1.5000000000 0.6328125000 0.0771484375
       0.0283203125 0.0019531250
  XBQ = -0.97656250000000000E-01 -0.42187500000000000E+00
       0.1564941406250000000E+00 0.16406250000000000E+00
       -0.85937500000000000E-01
       -0.54199218750000000E-01 0.77148437500000000E-01
       -0.3033447265625000000E-01 -0.48828125000000000E-03
       0.40283203125000000E-02
  XGQ = 0.5625000000 1.2812500000

; 
Bytes for Z-Filter (13):            20,BA,EA,25,23,41,C1,BB
Bytes for R-Filter (2B):            D0,C8,84,DC,B1,93,02,1D
Bytes for X-Filter (23):            50,C8,B5,4A,C2,21,04,90
Bytes for Gain-factors (30):        A0,11,20,92
2nd part of bytes B-Filter (0B):    00,97,FD,C8,DD,4C,C2,BC
1st part of bytes B-Filter (03):    C4,12,23,32,72,B9,B2,BA
Bytes for B-filter delay (18):      19,19,11,19

* HARRIS SLIC_
* VOR = 0.50000 RIR = 90000. CKR = 0.10000E-05
* VOX = 1.00000 RIX = 0.10000E+06 CKX = 0.10000E-05
* R0 = 600.00
Run # 1

Z-FILTER calculation results
Generator impedance ZI at a,b line!
Calculated and quantized coefficients:

\[ XZ = \begin{bmatrix} -0.05549 & 0.54647 & 0.29193 & -0.24595 & 0.19619 \\ -0.05566 & 0.54687 & 0.28906 & -0.24597 & 0.19531 \end{bmatrix} \]

Bytes for Z-Filter (13): 20, BA, EA, 25, 23, 41, C1, BB

RETURN LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>36.621</td>
<td>1800.</td>
<td>23.691</td>
</tr>
<tr>
<td>200.</td>
<td>34.580</td>
<td>1900.</td>
<td>24.104</td>
</tr>
<tr>
<td>300.</td>
<td>32.126</td>
<td>2000.</td>
<td>24.653</td>
</tr>
<tr>
<td>400.</td>
<td>30.127</td>
<td>2100.</td>
<td>25.360</td>
</tr>
<tr>
<td>500.</td>
<td>28.533</td>
<td>2200.</td>
<td>26.258</td>
</tr>
<tr>
<td>600.</td>
<td>27.251</td>
<td>2300.</td>
<td>27.391</td>
</tr>
<tr>
<td>700.</td>
<td>26.214</td>
<td>2400.</td>
<td>28.815</td>
</tr>
<tr>
<td>800.</td>
<td>25.373</td>
<td>2500.</td>
<td>30.567</td>
</tr>
<tr>
<td>900.</td>
<td>24.695</td>
<td>2600.</td>
<td>32.512</td>
</tr>
<tr>
<td>1000.</td>
<td>24.157</td>
<td>2700.</td>
<td>33.815</td>
</tr>
<tr>
<td>1100.</td>
<td>23.740</td>
<td>2800.</td>
<td>33.009</td>
</tr>
<tr>
<td>1200.</td>
<td>23.435</td>
<td>2900.</td>
<td>30.551</td>
</tr>
<tr>
<td>1300.</td>
<td>23.232</td>
<td>3000.</td>
<td>27.877</td>
</tr>
<tr>
<td>1400.</td>
<td>23.128</td>
<td>3100.</td>
<td>25.483</td>
</tr>
<tr>
<td>1500.</td>
<td>23.119</td>
<td>3200.</td>
<td>23.405</td>
</tr>
<tr>
<td>1600.</td>
<td>23.207</td>
<td>3300.</td>
<td>21.590</td>
</tr>
<tr>
<td>1700.</td>
<td>23.395</td>
<td>3400.</td>
<td>19.985</td>
</tr>
</tbody>
</table>

Min. Z-loop reserve: 3.290 dB
at frequency: 500.0 Hz

Min. Z-loop mirror signal reserve: 8.343 dB
at frequency: 7500.0 Hz

Warning! SICOFI specs (noise, gain tracking...) not guaranteed
Increase SLIC gain in transmit path at least by 0.17dB

Run # 2

X-FILTER calculation results
Calculated and quantized coefficients:

\[ XX = \begin{bmatrix} 1.49519 & 0.63652 & 0.07668 & 0.02832 & 0.00308 \\ 1.50000 & 0.63281 & 0.07715 & 0.02832 & 0.00195 \end{bmatrix} \]

Bytes for X-Filter (23): 50, C8, B5, 4A, C2, 21, 04, 90
X-filter attenuation function (in dB), (always absolute values)

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300.</td>
<td>-6.912</td>
<td>0.048</td>
<td>1900.</td>
<td>-4.040</td>
<td>0.009</td>
</tr>
<tr>
<td>400.</td>
<td>-6.839</td>
<td>0.046</td>
<td>2000.</td>
<td>-3.794</td>
<td>0.006</td>
</tr>
<tr>
<td>500.</td>
<td>-6.747</td>
<td>0.045</td>
<td>2100.</td>
<td>-3.545</td>
<td>0.004</td>
</tr>
<tr>
<td>600.</td>
<td>-6.636</td>
<td>0.043</td>
<td>2200.</td>
<td>-3.292</td>
<td>0.001</td>
</tr>
<tr>
<td>700.</td>
<td>-6.507</td>
<td>0.041</td>
<td>2300.</td>
<td>-3.036</td>
<td>0.001</td>
</tr>
<tr>
<td>800.</td>
<td>-6.361</td>
<td>0.039</td>
<td>2400.</td>
<td>-2.776</td>
<td>0.004</td>
</tr>
<tr>
<td>900.</td>
<td>-6.200</td>
<td>0.037</td>
<td>2500.</td>
<td>-2.512</td>
<td>0.007</td>
</tr>
<tr>
<td>1000.</td>
<td>-6.025</td>
<td>0.034</td>
<td>2600.</td>
<td>-2.243</td>
<td>0.010</td>
</tr>
<tr>
<td>1100.</td>
<td>-5.837</td>
<td>0.031</td>
<td>2700.</td>
<td>-1.970</td>
<td>0.014</td>
</tr>
<tr>
<td>1200.</td>
<td>-5.638</td>
<td>0.028</td>
<td>2800.</td>
<td>-1.694</td>
<td>0.018</td>
</tr>
<tr>
<td>1300.</td>
<td>-5.429</td>
<td>0.025</td>
<td>2900.</td>
<td>-1.415</td>
<td>0.023</td>
</tr>
<tr>
<td>1400.</td>
<td>-5.211</td>
<td>0.023</td>
<td>3000.</td>
<td>-1.135</td>
<td>0.028</td>
</tr>
<tr>
<td>1500.</td>
<td>-4.987</td>
<td>0.020</td>
<td>3100.</td>
<td>-0.856</td>
<td>0.033</td>
</tr>
<tr>
<td>1600.</td>
<td>-4.757</td>
<td>0.017</td>
<td>3200.</td>
<td>-0.583</td>
<td>0.039</td>
</tr>
<tr>
<td>1700.</td>
<td>-4.522</td>
<td>0.014</td>
<td>3300.</td>
<td>-0.320</td>
<td>0.045</td>
</tr>
<tr>
<td>1800.</td>
<td>-4.283</td>
<td>0.011</td>
<td>3400.</td>
<td>-0.071</td>
<td>0.052</td>
</tr>
<tr>
<td>1900.</td>
<td>-4.040</td>
<td>0.009</td>
<td>3500.</td>
<td>0.048</td>
<td>0.000</td>
</tr>
<tr>
<td>2000.</td>
<td>-3.794</td>
<td>0.006</td>
<td>3600.</td>
<td>0.046</td>
<td>1.008</td>
</tr>
</tbody>
</table>

GX results:

All attenuation values (in dB) refer to FREF = 1014. Hz

<table>
<thead>
<tr>
<th>RLX</th>
<th>SLIC+Z</th>
<th>VREF/VSICOFI</th>
<th>XREF</th>
<th>GX</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00</td>
<td>3.75</td>
<td>-4.42</td>
<td>-6.00</td>
<td>-2.17</td>
</tr>
<tr>
<td>0.02</td>
<td>3.75</td>
<td>+4.42</td>
<td>+6.00</td>
<td>-2.15</td>
</tr>
</tbody>
</table>

Second byte for Gain: 20,92

Calculation of transmit transfer function (AD)

All attenuation values (in dB) refer to FREF = 1014.0 Hz

Generator impedance ZI at a,b line!
TGREF CA = 0.259 ms      TGREF CB = 0.273 ms

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>13.827</td>
<td>2.523</td>
<td>2000.</td>
<td>0.017</td>
<td>0.010</td>
</tr>
<tr>
<td>200.</td>
<td>0.339</td>
<td>1.786</td>
<td>2100.</td>
<td>0.011</td>
<td>0.015</td>
</tr>
<tr>
<td>300.</td>
<td>0.006</td>
<td>0.589</td>
<td>2200.</td>
<td>0.004</td>
<td>0.021</td>
</tr>
<tr>
<td>400.</td>
<td>0.028</td>
<td>0.287</td>
<td>2300.</td>
<td>-0.003</td>
<td>0.027</td>
</tr>
<tr>
<td>500.</td>
<td>0.025</td>
<td>0.166</td>
<td>2400.</td>
<td>-0.009</td>
<td>0.035</td>
</tr>
<tr>
<td>600.</td>
<td>0.016</td>
<td>0.103</td>
<td>2500.</td>
<td>-0.014</td>
<td>0.044</td>
</tr>
<tr>
<td>700.</td>
<td>0.007</td>
<td>0.067</td>
<td>2600.</td>
<td>-0.015</td>
<td>0.054</td>
</tr>
<tr>
<td>800.</td>
<td>0.001</td>
<td>0.044</td>
<td>2700.</td>
<td>-0.013</td>
<td>0.079</td>
</tr>
<tr>
<td>900.</td>
<td>-0.002</td>
<td>0.028</td>
<td>2800.</td>
<td>-0.006</td>
<td>0.079</td>
</tr>
<tr>
<td>1000.</td>
<td>-0.002</td>
<td>0.018</td>
<td>2900.</td>
<td>0.006</td>
<td>0.095</td>
</tr>
<tr>
<td>1100.</td>
<td>0.000</td>
<td>0.011</td>
<td>3000.</td>
<td>0.025</td>
<td>0.115</td>
</tr>
<tr>
<td>1200.</td>
<td>0.004</td>
<td>0.006</td>
<td>3100.</td>
<td>0.051</td>
<td>0.139</td>
</tr>
<tr>
<td>1300.</td>
<td>0.009</td>
<td>0.003</td>
<td>3200.</td>
<td>0.087</td>
<td>0.169</td>
</tr>
<tr>
<td>1400.</td>
<td>0.014</td>
<td>0.001</td>
<td>3300.</td>
<td>0.137</td>
<td>0.208</td>
</tr>
<tr>
<td>1500.</td>
<td>0.019</td>
<td>0.000</td>
<td>3400.</td>
<td>0.212</td>
<td>0.262</td>
</tr>
<tr>
<td>1600.</td>
<td>0.022</td>
<td>0.000</td>
<td>3500.</td>
<td>0.335</td>
<td>0.339</td>
</tr>
<tr>
<td>1700.</td>
<td>0.024</td>
<td>0.001</td>
<td>3600.</td>
<td>0.565</td>
<td>0.456</td>
</tr>
<tr>
<td>1800.</td>
<td>0.024</td>
<td>0.003</td>
<td>3700.</td>
<td>1.071</td>
<td>0.649</td>
</tr>
<tr>
<td>1900.</td>
<td>0.022</td>
<td>0.006</td>
<td>3800.</td>
<td>2.402</td>
<td>0.984</td>
</tr>
</tbody>
</table>
R-FILTER calculation results

Calculated and quantized coefficients:

\[ \begin{align*}
XR &= 0.95239 \quad 0.04758 \quad -0.04485 \quad 0.00311 \quad -0.00350 \\
XRQ &= 0.95312 \quad 0.04687 \quad -0.04492 \quad 0.00391 \quad -0.00195
\end{align*} \]

Bytes for R-Filter (2B): D0,C8,84,DC,B1,93,02,1D

R-filter attenuation function (in dB), (always absolute values)

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>0.350</td>
<td>-0.004</td>
</tr>
<tr>
<td>400</td>
<td>0.326</td>
<td>-0.003</td>
</tr>
<tr>
<td>500</td>
<td>0.298</td>
<td>-0.002</td>
</tr>
<tr>
<td>600</td>
<td>0.266</td>
<td>-0.001</td>
</tr>
<tr>
<td>700</td>
<td>0.232</td>
<td>0.001</td>
</tr>
<tr>
<td>800</td>
<td>0.197</td>
<td>0.002</td>
</tr>
<tr>
<td>900</td>
<td>0.161</td>
<td>0.003</td>
</tr>
<tr>
<td>1000</td>
<td>0.127</td>
<td>0.004</td>
</tr>
<tr>
<td>1100</td>
<td>0.095</td>
<td>0.005</td>
</tr>
<tr>
<td>1200</td>
<td>0.066</td>
<td>0.006</td>
</tr>
<tr>
<td>1300</td>
<td>0.041</td>
<td>0.007</td>
</tr>
<tr>
<td>1400</td>
<td>0.021</td>
<td>0.008</td>
</tr>
<tr>
<td>1500</td>
<td>0.006</td>
<td>0.009</td>
</tr>
<tr>
<td>1600</td>
<td>-0.003</td>
<td>0.009</td>
</tr>
<tr>
<td>1700</td>
<td>-0.006</td>
<td>0.010</td>
</tr>
<tr>
<td>1800</td>
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</tr>
<tr>
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<td>0.010</td>
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<tr>
<td>2000</td>
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<tr>
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<td>2200</td>
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<td>2700</td>
<td>0.379</td>
<td>0.005</td>
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<tr>
<td>2800</td>
<td>0.462</td>
<td>0.004</td>
</tr>
<tr>
<td>2900</td>
<td>0.552</td>
<td>0.002</td>
</tr>
<tr>
<td>3000</td>
<td>0.647</td>
<td>-0.001</td>
</tr>
<tr>
<td>3100</td>
<td>0.746</td>
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<tr>
<td>3200</td>
<td>0.846</td>
<td>-0.006</td>
</tr>
<tr>
<td>3300</td>
<td>0.945</td>
<td>-0.009</td>
</tr>
<tr>
<td>3400</td>
<td>1.039</td>
<td>-0.012</td>
</tr>
<tr>
<td>3500</td>
<td>-0.004</td>
<td>0.000</td>
</tr>
<tr>
<td>3600</td>
<td>-0.003</td>
<td>0.887</td>
</tr>
</tbody>
</table>

GX results:

All attenuation values (in dB) refer to FREF = 1014.0 Hz

- RLR SLIC+Z VSICOFI/VREF RREF GR
  7.00 - 6.29 - -4.42 - 0.12 = 5.01 ideal
  6.99 = 6.29 + -4.42 + 0.12 + 5.00 quant

First byte for Gain (30): A0,11

Calculation of receive transfer function (DA)

All attenuation values (in dB) refer to FREF = 1014.0 Hz

Terminating impedance ZI at a,b line!

TGREF CA = 0.236 ms TGREF CB = 0.219 ms
<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
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</thead>
<tbody>
<tr>
<td>100.</td>
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<td>0.013</td>
<td>2000.</td>
<td>-0.010</td>
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<tr>
<td>200.</td>
<td>-0.001</td>
<td>0.002</td>
<td>2100.</td>
<td>-0.015</td>
<td>0.047</td>
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<tr>
<td>300.</td>
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<td>2200.</td>
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<td>0.000</td>
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<td>0.062</td>
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<tr>
<td>500.</td>
<td>-0.003</td>
<td>0.000</td>
<td>2400.</td>
<td>-0.029</td>
<td>0.071</td>
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<tr>
<td>600.</td>
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<td>0.001</td>
<td>2500.</td>
<td>-0.032</td>
<td>0.081</td>
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<tr>
<td>700.</td>
<td>-0.004</td>
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<td>2600.</td>
<td>-0.031</td>
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<tr>
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<td>0.004</td>
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<tr>
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<td>2900.</td>
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<tr>
<td>1100.</td>
<td>0.000</td>
<td>0.009</td>
<td>3000.</td>
<td>0.012</td>
<td>0.160</td>
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<tr>
<td>1200.</td>
<td>0.001</td>
<td>0.011</td>
<td>3100.</td>
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<td>0.225</td>
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<tr>
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<tr>
<td>1800.</td>
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<td>0.030</td>
<td>3700.</td>
<td>1.203</td>
<td>0.712</td>
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<tr>
<td>1900.</td>
<td>-0.005</td>
<td>0.035</td>
<td>3800.</td>
<td>2.612</td>
<td>1.049</td>
</tr>
</tbody>
</table>

Run # 2

B-FILTER calculation results
Terminating impedance ZL at a,b line!

Calculated and quantized coefficients:

\[
\begin{align*}
XB & = -0.09979 -0.41835 0.15620 0.16296 -0.08400 \\
& \quad -0.05427 0.07695 -0.03033 -0.00038 0.00406 \\
XBQ & = -0.09766 -0.42187 0.15649 0.16406 -0.08594 \\
& \quad -0.05420 0.07715 -0.03033 -0.00049 0.00403
\end{align*}
\]

2nd part of bytes B-Filter (0B): 00,97,FD,C8,DD,4C,C2,BC
1st part of bytes B-Filter (03): C4,12,23,32,72,B9,B2,BA
TRANSMISSION HYBRID LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>52.656</td>
<td>1800.</td>
<td>54.439</td>
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<tr>
<td>200.</td>
<td>45.934</td>
<td>1900.</td>
<td>54.867</td>
</tr>
<tr>
<td>300.</td>
<td>49.743</td>
<td>2000.</td>
<td>54.697</td>
</tr>
<tr>
<td>400.</td>
<td>51.739</td>
<td>2100.</td>
<td>54.142</td>
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<tr>
<td>500.</td>
<td>51.819</td>
<td>2200.</td>
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<tr>
<td>600.</td>
<td>51.108</td>
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<tr>
<td>700.</td>
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</tr>
<tr>
<td>800.</td>
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<tr>
<td>900.</td>
<td>49.300</td>
<td>2600.</td>
<td>53.364</td>
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<tr>
<td>1000.</td>
<td>49.100</td>
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<td>49.113</td>
<td>2800.</td>
<td>55.481</td>
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<td>1200.</td>
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<td>2900.</td>
<td>57.354</td>
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<tr>
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<td>49.788</td>
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<td>60.071</td>
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<tr>
<td>1400.</td>
<td>50.461</td>
<td>3100.</td>
<td>63.930</td>
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<tr>
<td>1500.</td>
<td>51.350</td>
<td>3200.</td>
<td>65.910</td>
</tr>
<tr>
<td>1600.</td>
<td>52.410</td>
<td>3300.</td>
<td>61.158</td>
</tr>
<tr>
<td>1700.</td>
<td>53.520</td>
<td>3400.</td>
<td>56.393</td>
</tr>
</tbody>
</table>

Additional B-filter delay (in seconds): 0.625E-04
Bytes for B-filter delay (18): 19,19,11,19
The configurations 1b) and 1c) can be derived from the equivalent circuit diagram 1a) by zeroing the elements that are not used.

With $R_{\text{par}} = 0$ the entry of a series impedance 2b) becomes possible with equivalent circuit diagram 2a).

Figure 5
Equivalent Circuit Diagram 1

Figure 6
Equivalent Circuit Diagram 2

Figure 7
Equivalent Circuit Diagram 3
Figure 8

Figure 9
Figure 10

Figure 11
Figure 12

Figure 13
SICOFI® Application together with ERICSSON SLIC PBL 3762

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<td>3.3 Input Circuit</td>
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<td>3.4.2 Starting Equations</td>
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<tr>
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<td>4.3 Model for Impedances</td>
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<tr>
<td>4.4 Other Input Parameters</td>
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<td>524</td>
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<tr>
<td>5.2 Specification File</td>
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<td>536</td>
</tr>
<tr>
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</table>
1 Introduction

1.1 General

The introduction of digital switching systems has led to a significant reduction of the central part of the hardware constituent. In order to achieve further integration at the periphery, i.e. at the interface to the analog subscriber, the state of the art is to split up the analog subscriber circuit into a line driver and sensor chip (solid state SLIC: Subscriber Line Interface Circuit) on the one hand and a signal processor (in our case SICOFI) on the other; an even more cost effective possibility is to use a dual channel SICOFI (SICOFl-2) and two SLIC’s for a group of two analog subscribers.

In this note, we will call SLIC the combination of the solid state SLIC and the other discrete components which are not integrated and have an influence on the transmission characteristics.

We will call Subscriber Line MODULE the combination SLIC + SICOFI.

The aim of this paper is to describe an example of design of such a module for given specifications. It includes the corresponding hardware, the calculations necessary to build up a mathematical model of the SLIC, the software using this model and the results of the calculations with the SLIC and SICOFI software, which will permit to adapt the module to the specifications.

The Siemens Signal processing Codec Filter (SICOFI) PEB 2060 is a fully integrated PCM Codec (coder/decoder) and transmit/receive filter produced in an advanced low power CMOS technology.

It can be used in combination with a variety of solid state Subscriber Line Interface Circuits (SLIC).

This note describes an example of application with the ERICSSON SLIC PBL 3762 which allows a compact and low cost realisation of PABX subscriber line cards.

Other realisations (e.g. in central offices) are also possible with the full feature Ericsson SLIC’s PBL 3736 and 3739. The corresponding software will be included in an other application note.

The combination of SICOFI and PBL 3762 provides a cost effective solution because few external components are necessary and a high flexibility because of the flexibility of the digital signal processing:

- The ERICSSON PBL 3762 performs BORSCHT functions as loop current, resistive battery feed, ring relay driver and signaling functions as well as signal transmission including 2- to 4-wire and 4- to 2-wire conversion. The 2-wire termination impedance ("hybrid function" or "impedance matching") is adjustable by external impedances.
- The PEB 2060 (SICOFI) consists of several digital filters (Z,B,GR,GX,R and X-filters), which provide software controlled adjustment of the analog behavior of the digital switching system.
- These adjustments include improved hybrid function ("Z-filter"), transhybrid balancing function ("B-filter") as well as frequency correction ("R and X-filters") and level control in receive and transmit direction ("GR and GX-filters").
Furthermore the programmable parallel signaling inputs and outputs of the PEB 2060 (SICOFI) provides a flexible interface to the PBL 3762 signaling pins.

1.2 Overview

In the chapter 2, an example of design of a subscriber line interface module using the SICOFI and the PBL 3762 will be given (basic set-up).

The chapter 3 explains in details the calculation of a mathematical model of this SLIC.

This model allows to write a program described in chapter 4.

The program enables to calculate parameters describing the SLIC as a function of the frequency. With these parameters, coefficients can be calculated with the SICOFI coefficient program for the PEB 2060 (SICOFI) in chapter 5.

These coefficients have then to be programmed into the SICOFI.

Results of measurements are given in chapter 6.

The last chapter shows the good correlation between the calculated results and the measured ones for various configurations and specifications.

1.3 Glossary

PBX : Private Branch eXchange (USA)
PABX : Private Automatic Branch eXchange (= PBX in Europe)
C.O. : Central Office
SICOFI : PEB 2060
SICOFI software : See SICOFI software description
SLIC : ERICSSON PBL 3762
SLIC + SICOFI : Subscriber Line MODULE
(SLIC + SICOFI) + Peripheral Board Controller + Microprocessor
+ discrete components + ... (= all BORSCHT functions)
: Subscriber Line Interface Circuit
SLIC In our model : PBL 3762 + discrete components
BORSCHT : Battery feed
: Overvoltage protection
Ringing
Supervision
Codec + filtering
Hybrid
Testing
2 BASIC Set-Up SICOFI®-PBL 3762

2.1 Circuit Diagram
The diagram of the basic set-up can be seen in figure 1.

![Circuit Diagram](image)

**Figure 1**
**Basic Set-Up SICOFI® + ERICSSON PBL 3762**
Parts list corresponding to figure 1.

Capacitors:

\[
\begin{align*}
C_r & = 2.2 \text{ nF} \\
C_t & = 2.2 \text{ nF} \\
C_{HP} & = 10 \text{ nF} \\
C_{DC} & = 3.3 \mu\text{F} \\
C_{KX} & = 1 \mu\text{F} \\
C_D & = 15 \text{ nF} \\
\end{align*}
\]

Resistors: (1/4 W, 10% if not else specified)

\[
\begin{align*}
Z_t & = 600 \text{ k}\Omega\ 0.5\% \\
Z_r & = 300 \text{ k}\Omega\ 0.5\% \\
R_{DC1} & = 20 \text{ k}\Omega \\
R_{DC2} & = 20 \text{ k}\Omega \\
R_{IX} & = 24 \text{ k}\Omega \\
R_{SG} & = 20 \text{ k}\Omega \\
R_D & = 39 \text{ k}\Omega \\
R_1 & = 5.6 \Omega \\
\end{align*}
\]

Diodes:

\[
\begin{align*}
D1 & = 1N4007 \\
D2 & = 1N4148 \\
\end{align*}
\]

2.2 Application Hints

No attention has been paid to the overvoltage protection, signaling and loop monitoring functions in this application note because they should not influence the transmission characteristics.

Circuit Design

1. The capacitors \(C_t\) and \(C_r\) are used to stabilize the circuit at high frequencies; a value of 2.2 nF for both is correct.

2. The two impedances \(Z_t\) (matching impedance) and \(Z_r\) (gain impedance) have been exactly measured in order to make correct calculations. These are sensitive components and have to be precise (at least 1%).

3. The RSN pin is very sensitive to noise and therefore the leads to \(Z_t\), \(R_{DC1}\) and \(Z_r\) should be kept as short as possible and close to the ground plane.

4. The \(C_{KX}\) capacitor and the \(R_{IX}\) resistor (decoupling circuit) are not necessary with the SICOFI version V4.x and later: The PBL 3762 DC offset is limited to +/- 25 mV and the maximum allowed input DC offset of the SICOFI V4.x is +/- 50 mV.

5. A diode (D1) and a resistor (\(R_1\)) prevent having currents flowing in the wrong direction and limits the \(di/dt\) at the \(V_{Bat}\) pin of the PEB 3762.

6. A diode (D2) prevents \(V_{EE}\) to become lower than \(V_{Bat}\). D1, D2 and \(R_1\) may be shared by several SLIC’s.
Control Inputs

The SICOFI PEB 2060 has three output signaling pins and four programmable signaling pins which allow an easy control of the two control pins C1 and C2 and of the two enable inputs E0 and E1 of the PBL 3762.

The DET output of the PBL 3762 is connected to the SI1 input pin of the SICOFI.

Connections

<table>
<thead>
<tr>
<th>SICOFI</th>
<th>PBL3762</th>
</tr>
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<tbody>
<tr>
<td>SO1</td>
<td>C2</td>
</tr>
<tr>
<td>SO2</td>
<td>C1</td>
</tr>
<tr>
<td>SO3</td>
<td>E1</td>
</tr>
<tr>
<td>SD</td>
<td>E0</td>
</tr>
<tr>
<td>SI1</td>
<td>DET</td>
</tr>
</tbody>
</table>

With:

C2  C1  E1  E0  x  x  x  x
SO1  SO2  SO3  SD  SC  SB  SA  SEL

1  0  0  0  0  0  0  0  0  0  0  := 80

in the SICOFI signaling byte, the SLIC is programmed in active state and DET as ground key status.

Loop Monitoring Functions

The loop current, ground key and ring trip detectors report their status via a common output: DET (pin 14).

The detector connected to DET is selected via the four bit wide control interface C2,C1,E1,E0.

The threshold for the loop current detector is set-up by the resistor \( R_D \) by the following formula:

\[
I_{\text{loop threshold}} = I_{\text{th}} = 375 / R_D \text{ (Amperes)}
\]

In our application \( R_D = 39 \, k\Omega \) gives \( I_{\text{th}} = 9.6 \text{ mA} \).

\( C_D \) is then calculated by \( C_D = 0.5 \text{ ms} / R_D \).

For more details see the PBL 3762 data sheet.

Hybrid Function

There is no need of extra external components to build the echo attenuation path because this is taken care of by the SICOFI B-filter.a

AC-DC Decoupling Capacitor

The high pass filter capacitor \( C_{\text{HP}} \) connected between pin 1 and pin 22 of the PBL 3762 provides decoupling of circuits sensing tip-to-ring conditions and circuits processing AC signals.
C should be choosen as high as possible in order to have a low cut off frequency:
\[ f_{CHP} = \frac{1}{(C_{HP} \times R_{HP} \times 2\pi)}. \]

\( R_{HP} \) is a PBL 3762 internal resistor with a value of 400 kΩ.

We have choosen a worst case (\( C_{HP} = 10 \text{nF}, f_{CHP} = 40 \text{Hz} \)) in our basic setup (see circuit diagram in figure 1).

A value of 33 nF for \( C_{HP} \) is counselled; it will position \( f_{CHP} \) at 14 Hz and so have less influence on the transmission characteristics.

Battery Feed and Saturation Guard

Case 1: Active state (\( V_t < V_{REF} \))

For a tip-to-ring voltage \( V_t \) less than the saturation guard reference voltage \( V_{REF} \), the SLIC emulates a resistive feed characteristic with an apparent battery voltage of 50 V (independent of the actual battery voltage \( V_{Bat} \) connected).

The voltage at the line is: \( V_t = 50 \times \frac{R_L}{(R_L + (R_{DC1} + R_{DC2})/50)} \) with \( R_L = \) loop resistance (DC).

For \( -24 \text{ V} < V_{Bat} < -28 \text{ V} \), \( V_{REF} \) is correctly set with the pin RSG not connected. For higher battery voltages, \( V_{REF} \) may be adjusted to let resistive feed as described above remain in force until the tip-to-ring DC voltage approaches the supply voltage.

Guide line:

Adjust \( V_{REF} = 15.5 + 500000/R_{SG} \) to approximately: \( V_{REF} = |V_{Bat}| - 8 \text{ V} \) i.e.:

\[ R_{SG} = \frac{500000}{|V_{Bat}| - 8.0 - 15.5}. \]

In our case \( V_{Bat} = -48 \text{ V} \) therefore \( R_{SG} = 20 \text{ kΩ} \).

Case 2: Active state and saturation guard (\( V_t > V_{REF} \))

When the tip-to-ring voltage \( V_t \) exceeds \( V_{REF} \), the feed characteristic changes in order to prevent the line drive amplifiers from distorting the AC signal (may occur by insufficient amplifier bias voltages).

This has an influence on the transmission characteristics, especially on the return loss.

Case 3: \( C_1 = C_2 = 1 \)

With the SLIC in disabled state ("stand by") a high resistance feed characteristic is enabled.

DC Path

The DC feed resistance is programmed by two resistors \( R_{DC1} \) and \( R_{DC2} \) connected in series to the receive summing node (RSN) and decoupled from AC by the capacitor \( C_{DC} \) (recommended cutoff frequency: 14 Hz).

This has only a small influence on the transmission characteristics depending on the cutoff frequency value of the system \( R_{DC1}, R_{DC2}, C_{DC} \).
3 Mathematical Model

3.1 Circuit Model

A software emulation of the SLIC is necessary in order to produce a file of the so-called "K-parameters" (see chapter 3.4.1) to interface with the SICOFI program.

We need first to calculate a mathematical model of the SLIC which will then be used to write a SLIC program (see chapter 4).

This model must include all external components which influence the transfer functions of the whole circuit.

Therefore in the next pages we will call SLIC the part of our basic setup composed by all analog external components and by the PBL 3762.

The resistors and capacitors of the circuit drawing are transformed in complex impedances in order to be as general as possible (see impedance model in chapter 4.3).

For more details about the ERICSSON SLIC model see the PBL 3762 data sheet.
Figure 2 shows the grounded model which has been chosen for its simplicity.

![Figure 2: Equivalent Model of the SLIC](image)

### 3.2 Preliminary Data and Symbols Meaning

The values of the different parameters from figure 2 are listed hereunder:

- $R_2 = 20 \, \Omega$ gain setting of output current amplifier
- $R_3 = 9.98 \, k\Omega$ gain setting of output current amplifier
- $C_{HP} = 10 \, nF$ high pass filter in transmit direction
- $R_{HP} = 400 \, k\Omega$ high pass filter in transmit direction
- $R_{DC1} = 20 \, k\Omega$ DC path
- $R_{DC2} = 20 \, k\Omega$ DC path
- $C_{DC} = 3.3 \, \mu F$ DC path
- $Z_1 = 600 \, k\Omega$ matching impedance
$Z_r = 300 \, \text{k}\Omega$  
gain impedance (gain $4w - 2w \# - Z_t / 2 \times Z_t$)

$Z_p = 2.2 \, \text{nF}$  
parallel impedance at (a,b) line: This grounded impedance will be doubled in the program PBL 3762. FOR because there are two of them at the SLIC input.

$Z_l = 20 \, \Omega$  
fuse impedance

$Z_g = 600 \, \Omega$  
line/generator AC impedance

RAX: DC decoupling circuit in transmit direction

PRSG: coefficient for saturation guard (7 when saturation guard, 1 normally)

$f_{DC}$: cut-off frequency of the DC low pass filter

\[
f_{DC} = \frac{1}{\left(\frac{R_{DC1} + R_{DC2}}{2}\right) \times C_{DC} \times 2\pi}
\]

HP1: high pass filter in transmit direction

\[
HP1 = \frac{j \times 2 \times \pi \times f \times C_{HP} \times R_{HP}}{1 + j \times 2 \times \pi \times f \times C_{HP} \times R_{HP}}
\]

\[
= \frac{1}{1 - j \times f_{CHP} / f}
\]

RAX: Decoupling circuit in transmit direction

\[
RAX = j \times C_{xx} \times R_{IX} \times \Omega MEGA / (1 + j \times C_{xx} \times R_{IX} \times \Omega MEGA)
\]

PRSG: Saturation guard:

\[
HSG = \frac{Z_t \times PRSG}{20. \times \left(\frac{R_{DC1} + R_{DC2}}{2}\right) \times (1 + j \times f / f_{CDC})}
\]

$X$: Total correction factor

$1/X = HP1 + HSG$

The AC output stage of the PBL 3762 is a current controlled current source (CCS) which amplifies the current at the RSN summing point ($I_{RSN}$) and which is loaded by the input circuit.

F: Open loop gain of the current amplifier

\[
F = 10000. / (1 + j \times f / 100)
\]
3.3 Input Circuit

The figure 4 shows the input circuit of the SLIC where $Z_{out}$ is the equivalent output impedance of the CCS.

The equivalent impedance ($Z_{eq}$) of the input circuit needs to be calculated:

$$I_0 = I_1 - I_p$$  \hspace{1cm} (10)

$$V_0 = -I_1 \times (Z_g + Z_l) + V_g$$  \hspace{1cm} (11)

$$I_p = V_0 / Z_p$$  \hspace{1cm} (12)

$$I_0 = -V_0 / Z_{out}$$  \hspace{1cm} (13)

$$V_0 = Z_p \times I_p$$  \hspace{1cm} (12)

From (10) & (11) & (12), we can deduce:

$$I_0 = V_0 / Z_p + V_g / Z_l - (V_g - V_0) / (Z_g + Z_l)$$
that is:

$$I_0 = \frac{V_g}{(Z_g + Z)} - V_0/Z_{eq} \quad (14)$$

with

$$Z_{eq} = \frac{Z_p}{Z_g + Z} \quad (15)$$

### 3.4 Calculations

The PBL 3762 has a current output; therefore we need to work with the K-parameters which do not require to short-circuit the output (for more information about these parameters see the SICOFI software description).

#### 3.4.1 K-Parameters

A SLIC with a symmetrical generator $V_g$ and a symmetrical line impedance $Z_g$ can be considered as a circuit accessible through the currents and voltages of a three port: $(V_1, I_1), (V_2, I_2), (V_3, I_3)$.

Three equations are sufficient to describe the SLIC completely and any linear combination of the variables is possible.

Let us take the following combination:

(100) $a_1 = V_1 + Z_g \times I_1$

(200) $b_1 = V_1 - Z_g \times I_1$

Then using these new variables, the model of the SLIC becomes:

![Figure 5](AttachedDiagram)

**K-1 Three Port Model with the Variables $a_1$ and $b_1$**

Following equations can now be written:

(300) $b_1 = K_{11} \times a_1 + K_{12} \times V_3 + K_{13} \times I_2$

(400) $V_2 = K_{21} \times a_1 + K_{22} \times V_3 + K_{23} \times I_2$

(500) $I_3 = K_{31} \times a_1 + K_{32} \times V_3 + K_{33} \times I_2$

When the SLIC is connected to the SICOFI, we can assume that:

* $I_2 = 0$ because the input impedance of SICOFI is very high.
* $I_3$ is not relevant in the SICOFI calculations.

According to these remarks, the equations system can be simplified as follow:

(600) $b_1 = K_{11} \times a_1 + K_{12} \times V_3$

(700) $V_2 = K_{21} \times a_1 + K_{22} \times V_3$
Parameter K11
Equation (600) gives $K_{11} = b_1/a_1$ when $V_3 = 0$
From (100) and (200) we can deduce:
\[
b_1/a_1 = (V_1 - Z_g 	imes I_1) / (V + Z_g 	imes I_1) = (V_1 / I_1 - Z_g) / (V_1 / I_1 + Z_g)
\]
Let us call $Z_{IN}$ the input impedance of the SLIC:
$Z_{IN} = V_1 / I_1$
Therefrom
$K_{11} = (Z_{IN} - Z_g) / (Z_{IN} + Z_g)$ for $V_3 = 0$

Parameter K12
$K_{12} = b_1 / V_3$ when $a_1 = 0$
From (100) follows:
\[
V_1 + Z_g 	imes I_1 = 0
\]
i.e. $V_1 = -Z_g 	imes I_1$
Thus
$b_1 = V_1 - Z_g 	imes I_1 = V_1 + V_1$
Therefrom
$K_{12} = 2 \times V_1 / V_3$ for $V_1 = -Z_g \times I_1$

Parameter K21
$K_{21} = V_2 / a_1$ when $V_3 = 0$
In this case:
\[
a_1 = V_1 + Z_g \times I_1 = V_g
\]
Then
$K_{21} = V_2 / V_g$ for $V_3 = 0$

Parameter K22
From (100) and $a_1 = 0$ follows: $V_1 = -Z_g \times I_1$
And we can deduce from (700) and $a_1 = 0$:
$K_{22} = V_2 / V_3$ for $V_1 = -Z_g \times I_1$

Remarks:
1. All these parameters are accessible by measurement with a symmetrical ground free generator and a complex voltmeter.
2. $R_L = -20 \times \log_{10} (|K_{11}|)$ is nothing else than the return loss of the SLIC without SICOFI.
3.4.2 Starting Equations

Using the data given by ERICSSON one can write the following starting equations:

Cf figure 2 and figure 3

\( V_8 = (V_i - V_o) \times F \)  
\( I_0 = \frac{(V_0 - V_o)}{R_2} - I_i \)  
\( I_0 = \frac{V_o}{(Z_o + Z_t)} - V_0 / Z_{eq} \)  
\( V_i = V_0 + I_i \times R_3 \)

Current summation point RSN:

\( I_i = -2 \times \left( \frac{V_o}{Z_t \times \text{HP1} \times \text{RAX}} + \frac{\text{RAR} \times V_i}{Z} + \frac{V_o}{\text{HRSG}} \right) \)  
\( F = \frac{1E + 04}{1 + j \times f / 100} \) (open loop gain)  
\( G = -I_i / I_0 \) (total current gain)  
\( V_1 = V_o - Z_o \times I_1 \)

The transmit path is simply described by:

\( V_t / V_0 = \text{RAX} \times \text{HP1} \)

3.4.3 Calculation of K11

K11 is defined by \((Z_{in} - Z_0) / (Z_{in} + Z_0)\)

\( V_8 = \frac{F}{(1 + F)} \times (V_0 + I_i \times R_3) \)  
\( I_0 = \frac{V_0}{R_2} - \frac{F \times V_0}{R_2 \times (1 + F)} - \frac{F \times I_i \times R_3}{R_2 \times (1 + F)} - I_i \)  
\( I_0 = \frac{V_0 - F \times R_3 \times I_i - R_2 \times (1 + F) \times I_i}{R_2 \times (1 + F)} \)  
\( I_i = -\frac{2 \times V_0}{Z_t \times X} \)

Where \( 1/X = \text{HP1} + \text{HSG} \)

\( I_0 = \frac{V_0 \times Z_t \times X + V_0 \times 2 \times F \times R_3 + V_0 \times 2 \times R_2 \times (1 + F)}{R_2 \times Z_t \times X \times (1 + F)} \)  
\( V_0 / I_0 = 1 / Z_{OUT} \)  
\( 1 / Z_{OUT} = \frac{2 \times F \times (R_2 + R_3) + 2 \times R_2 + Z_t \times X}{Z_t \times X \times R_2 \times (1 + F)} \)  
\( 1 / Z_p = j \times f \times C_{tr} \times 2\pi \)  
\( Z_{in} = Z_t + Z_p / / Z_{OUT} \)
3.4.4 Calculation of K12

K22 is defined by: \( 2 \times V_1 / V_3 \) when \( V_g = 0 \)

Let us calculate first the current gain \( G \) (cf figure 3):

\[
(\text{V}_g = 0) \rightarrow V_0 = -I_0 \times Z_{eq} \quad (30)
\]

\[
(30) \& (2) \rightarrow R_2 \times (I_0 + I_i) + V_8 = I_0 \times Z_{eq} \quad (31)
\]

\[
(1) \leftrightarrow V_8 = V_i \times F / (1 + F) \quad (32)
\]

\[
(4) \rightarrow V_i = -I_0 \times Z_{eq} + I_i \times R_3 \quad (33)
\]

\[
(32) \& (4) \& (31) \rightarrow R_2 \times (I_0 + I_i) + (-I_0 \times Z_{eq} + I_i \times R_3) \times F / (1 + F) = -I_0 \times Z_{eq}
\]

\[
I_0 \times (R_2 \times (1 + F) + Z_{eq}) = I_i \times (R_2 \times (1 + F) - R_3 \times F)
\]

\[
G = -I_0 / I_i = \frac{R_3 \times F + R_2 \times (1 + F)}{R_2 \times (1 + F) + Z_{eq}} \quad (34)
\]

calculation of \( V_0 / V_i \):

\[
(\text{V}_g = 0) \& (3) \rightarrow I_0 = -V_0 / Z_{eq} = -I_i \times G \quad (35)
\]

\[
(35) \& (5) \rightarrow V_0 / (G \times Z_{eq}) = -2 \times V_0 / (Z_t \times X \times RAX) - 2 \times V_i / Z_t \quad (36)
\]

and by regrouping the terms in \( V_0 \) and \( V_i \):

\[
\frac{V_0}{V_i} = \frac{-2 \times G \times Z_{eq} / Z_t}{1 + 2 \times G \times Z_{eq} / Z_t \times X \times RAX} \quad (37)
\]

we have to calculate now \( V_1 / V_0 \):

---

**Figure 6**

![Diagram of circuit with symbols and labels](ITS01979)
$Z_f$ and $Z_g$ form a voltage divider; the calculations are then straightforward:

$$V_1 / V_0 = Z_g / (Z_g + Z_f)$$  \hspace{1cm} (38)

Thus

$$2 \times V_1 / V_t = \frac{Z_g}{Z_g + Z_f} \times \frac{-2 \times 2 \times G \times Z_{eq} / Z_t}{1 + 2 \times G \times Z_{eq} / Z_t \times X \times RAX}$$  \hspace{1cm} (39)

### 3.4.5 Calculation of $K_{21}$

$K_{21}$ is defined by $V_t / V_g$ when $V_r = 0$

![Figure 7](image)

we have a simple voltage divider:

$$\frac{V_g}{Z_f + Z_g + Z_p / Z_{OUT}} = \frac{V_0}{Z_p \parallel Z_{OUT}}$$  \hspace{1cm} (40)

$$V_t / V_g = (V_t / V_0) \times (V_0 / V_g)$$

hence:

$$(40) \text{ & } (9) \rightarrow V_t / V_g = \frac{RAX \times HP1 \times (Z_p \parallel Z_{OUT})}{Z_f + Z_g + (Z_p \parallel Z_{OUT})}$$  \hspace{1cm} (41)

### 3.4.6 Calculation of $K_{22}$

$K_{22}$ is defined by $V_t / V_t$ when $V_g = 0$

$$(37) \text{ & } (9) \rightarrow V_t / V_t = RAX \times HP1 \times \frac{-2 \times G \times Z_{eq} / Z_t}{1 + 2 \times G \times Z_{eq} / Z_t \times X \times RAX}$$  \hspace{1cm} (50)
3.5 Summary

\[
\frac{1}{Z_{out}} = \frac{2 \times F \times (R_2 + R_3) + 2 \times R_2 + Z_T \times X}{Z_T \times X \times R_2 \times (1 + F)} \tag{23}
\]

\[Z_{in} = Z_l + Z_p \parallel Z_{out} \tag{25}\]

\[K_{11} = \frac{Z_{in} - Z_g}{Z_{in} + Z_g} \tag{26}\]

\[Z_{eq} = \frac{Z_p}{Z_g + Z_f} \tag{15}\]

\[K_{12} = \frac{Z_g}{Z_g + Z_l} \times \frac{-2 \times 2 \times G \times Z_{eq} / Z_T}{1 + 2 \times G \times Z_{eq} / Z_l \times X \times R_A} \tag{39}\]

\[K_{21} = \frac{RAX \times HP1 \times (Z_p \parallel Z_{out})}{(Z_p \parallel Z_{out}) + Z_l + Z_g} \tag{41}\]

\[K_{22} = RAX \times HP1 \times \frac{-2 \times G \times Z_{eq} / Z_l}{1 + 2 \times G \times Z_{eq} / Z_T \times X \times R_A} \tag{50}\]

\[R_2 = 20 \ \Omega \quad \text{gain setting of output current amplifier} \]

\[R_3 = 9.98 \ k\Omega \quad \text{gain setting of output current amplifier} \]

\[C_{hp} = 10 \ \text{nF} \quad \text{high pass filter in transmit direction} \]

\[R_{hp} = 400 \ \text{k}\Omega \quad \text{high pass filter in transmit direction} \]

\[R_{dc1} = 20 \ \text{k}\Omega \quad \text{DC path} \]

\[R_{dc2} = 20 \ \text{k}\Omega \quad \text{DC path} \]

\[C_{dc} = 3.3 \ \mu\text{F} \quad \text{DC path} \]

\[Z_l = 600 \ \text{k}\Omega \quad \text{matching impedance} \]

\[Z = 300 \ \text{k}\Omega \quad \text{gain impedance (gain } 4w - 2w \# - Z_l / 2 \times Z) \]

\[Z_p = 2.2 \ \text{nF} \quad \text{parallel impedance at (a,b) line} \]

\[Z_f = 20 \ \Omega \quad \text{fuse impedance} \]

\[Z_g = 600 \ \Omega \quad \text{line/generator AC impedance} \]

\[RAX \quad \text{decoupling circuit in transmit direction (high pass } C_{KX}, R_{IX}) \]

\[PRSG \quad \text{coef. for saturation guard (7 when saturation guard, 1 normally)} \]

\[f_{dc} : \text{cut-off frequency of the DC low pass filter} \]

\[f_{hp} = \frac{1}{((R_{dc1} + R_{dc2}) / 2) \times C_{dc} \times 2\pi} \]

\[CHP \quad \text{high pass filter in transmit direction} \]

\[HP1 \quad \frac{j \times 2\pi \times f \times C_{hp} \times R_{hp}}{1 + j \times 2\pi \times f \times C_{hp} \times R_{hp}} \]

\[1 \quad \frac{1}{1 - j \times f_{chp} / f_{eq}} \]
RAX : connection circuit in transmit direction
RAX = \( j \times C_{KX} \times R_{IX} \times OMEGA / (1 + j \times C_{KX} \times R_{IX} \times OMEGA) \)

HSG : Saturation guard
HSG = \( \frac{Z_T \times PRSG}{20 \times (\left((R_{DC1} + R_{DC2}) / 2\right) \times (1 + j \times f / f_{CDC})} \)

X : total correction factor
\( 1 / X = HP1 + HSG \)

\( I_i \) : current summation point RSN
\( I_i = -2 \times \left( \frac{V_0}{Z_i \times HP1 \times RAX} + \frac{RAR \times V_r}{Z_i} + \frac{V_0}{HRSG} \right) \) (5)

F : open loop gain of current amplifier
\( F = \frac{10000}{1 + j \times f_{REQ} / 100} \) (6)

G : total current gain:
\( G = -I_i / I_0 \) (7)

\( V_1 \) : voltage at (a,b) line:
\( V_1 = V_0 - Z_g \times I_1 \) (8)

The transmit path is simply described by:
\( V_1 / V_0 = RAX \times HP1 \) (9)
4 Software

Each K-parameter is expressed in the PBL 3762.FOR program as an algebraic equation, combination of the various SLIC parameters which are provided by the SLIC input file PBL 3762.INP.

According to the values of the SLIC input data, the SLIC program PBL 3762.EXE calculates the values of the K-parameters in function of the frequency and writes them in an output file PBL 3762.SLI. This file will be used by the SICOFI program to calculate the coefficients for the PEB 2060 (for more information about the use of the SICOFI program see the SICOFI software description).

Explanations about the input file and the subroutines of the program are given in the following pages as well as a listing of the source file (ERIC.FOR).

Please note that the program has been written in FORTRAN (and compiled with the Microsoft FORTRAN optimizing compiler); therefore it is important to respect the FORTRAN convention of using a "." (POINT) for each REAL value.

4.1 Input File

The input file PBL 3762.INP is listed hereunder:

test (T:test=>amplitude and phase of Kij;  x:normal calculation)

x
*ZfRa1, ZfCA1, ZfCA2, ZfRA2, ZfRS, ZfCS  : fuse impedance Zf
  0.  0.  0.  0.  20.2  0.
*ZtRA1, ZtCA1, ZtCA2, ZtRA2, ZtRS, ZtCS  : matching impedance Zt
  598.E+03  0.  0.  0.  0.  0.
*ZrRA1, ZrCA1, ZrCA2, ZrRA2, ZrRS, ZrCS  : gain impedance Zr
  300.E+03  0.  0.  0.  0.  0.
CHP  : capacitor for internal high pass
  10.18E-09
*ZpRA1, ZpCA1, ZpCA2, ZpRA2, ZpRS, ZpCS  : parallel impedance Zp (= Ct = Cr)
  0.  0.  0.  0.  2.24E-09
CKX = High pass in transmit direction
  0.98E-06
RIX = High pass in transmit direction
  23.7E+03
RDC1          RDC2          CDC           : DC path
  20.40E+03  20.4E+03  3.33E-06
PRSG = Saturation guard (Yes = 7. no = 1.)
  1.
*ZSLL = Half loop attenuation
  0.5
*Zg : source/line impedance (with 6 elements)
*ZgRA1, ZgCA1, ZgCA2, ZgRA2, ZgRS, ZgCS
  600.  0.  000.E-00  0.  000.  0.

Remark:
Because the line impedance is embedded in the K-parameters, the SLIC file has to be recalculated every time the line impedance is changed.
4.2 Test Mode

TEST = "T"

In order to make a rough adaptation of the PBL 3762 to the required specifications, it is interesting to work first with the SLIC alone without SICOFI and to be able to view the different transfer functions and the input impedance.

A test mode was therefore inserted in the SLIC program:

When the switch TEST equals "T", the program writes the amplitude and phase (polar coordinates) of the input impedance and of all Kij parameters as a function of the frequency in the output file PBL 3762.SLI at 100 Hz steps.

The transformation cartesian to polar coordinates is made by the subroutine CPOL.

If TEST is other than "T" (default mode) then the program calculates the K-parameters for the SICOFI program. Real and imaginary part (cartesian coordinates) are written as a function of the frequency to the output file PBL 3762.SLI at 10 Hz steps.

4.3 Model for Impedances

In order to match any specification with the SICOFI + SLIC circuit, all the impedances $Z_t$, $Z_f$, $Z_r$, $Z_p$ and $Z_g$ can have complex values (see figure 1 and figure 2). They are described in the subroutine IMPED6 using 6 resistors and capacitors; a component value set to 0 means that this component does not exist.

The equivalent circuit diagram is the following:

![Figure 8](image)

where * stands for f, t, r, g or b. R means resistor; C means capacitance; S means series. These values are read from the input file.

Example:

*Zg : source/line impedance (with 6 elements )

ZgRA1, ZgCA1, ZgCA2, ZgRA2, ZgRS, ZgCS

820. 0. 115.OE-9 0. 220. 0.
is the equivalent impedance corresponding to a resistor of 220 Ω in series with 820 Ω in parallel with 115 nF:

4.4 Other Input Parameters

Half loop attenuation $Z_{SLI}$:

$Z_{SLI} = \frac{V_t}{V_i}$ in worst case and with SICOFI filters OFF.

$Z_{SLI}$ is a variable controlling the SICOFI + SLIC $Z$-filter loop. It should be measured in a worst case condition (for instance $Z_g = 1 \text{ MΩ}$). For more information see the chapter about input file in the SICOFI software description.

The other parameters are already defined in the preceding chapter.
4.5 FORTRAN Source File
Listing of PBL 3762.FOR

************************** Siemens A.G.******************************
*
** PROGRAM PBL3762 **
*
* Version V3.0  16 Nov. 88  Mr. GLASSER HL IT PD 22
* Revision V3.1  25 Jan. 89
* Revision V3.2  5 Juni 89
*
* Revision V3.3  14 Sept. 89  Subroutine IMPED6
*  Mr. KLIJESE HL IT AT
*
* PBL 3762 and following
*
******************************************************************************
*
** IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L) **
*
** INTEGER IN,OUT,I,N10,N399,TYPE **
** CHARACTER*13 FILEOUT,INFILE **
** CHARACTER*1 TEST **
*
** REAL ZtR1,ZtR2,ZtC1,ZtC2,ZtRS,ZtCS **
** REAL ZrR1,ZrR2,ZrC1,ZrC2,ZrRS,ZrCS **
** REAL ZfR1,ZfR2,ZfC1,ZfC2,ZfRS,ZfCS **
** REAL ZpR1,ZpR2,ZpC1,ZpC2,ZpRS,ZpCS **
** REAL ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS **
** REAL RIX,CKX,ZRT,ZRR,ZCHP,RHP,Cab **
** REAL FREQ,FCHP,FCDC **
** REAL DB,PH,HAHA(2),HAP(2),PI **
** REAL FLP1,PRSG **
** REAL PI2,ZSLI **
** REAL RDC1,RDC2,CDC,R2,R3 **
*
** COMPLEX K11T(399),K12T(399),K21T(399),K22T(399),KDETT(399) **
** COMPLEX K11,K12,K21,K22,KDET **
** COMPLEX Zout,ZIN,Zp,ZL,ZT,ZR,ZF,ZG,DEN **
** COMPLEX G,LP1,RAX,O,F,Yab,Y,Yp,Yout,HP1,Z1,X **
** COMPLEX ZINT(399),ZpT(399),ZLT(399) **
** COMPLEX VAR1,Zeq **
*
** data storage  for line/source impedance Zg, Zt, Zr, fuse  **
** impedance Zf, Zp **
** COMMON /QZg/ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS **
** COMMON /QZt/ZtR1,ZtR2,ZtC1,ZtC2,ZtRS,ZtCS **
** COMMON /QZr/ZrR1,ZrR2,ZrC1,ZrC2,ZrRS,ZrCS **
** COMMON /QZf/ZfR1,ZfR2,ZfC1,ZfC2,ZfRS,ZfCS **
** COMMON /QZp/ZpR1,ZpR2,ZpC1,ZpC2,ZpRS,ZpCS **
*
** COMMON /QK/K11,K12,K21,K22,KDET **
** COMMON /QPI2/ PI2 **
** COMMON /QP/ PI **
5 Coefficient Calculation

The execute file PBL 3762.EXE is a compiled version of the file PBL 3762.FOR. It gives an output file named PBL 3762.SLI using the input file PBL 3762.INP. PBL 3762.SLI used in combination with the specification file allows the SICOFI coefficient program to calculate and optimize the SICOFI coefficients.

In order to show the accuracy of the model, we have chosen to calculate using the measured values of the components on the test board.

In practice, it will be sufficient to calculate for the nominal values, but $Z_t$ and $Z_r$ are sensitive components and have to be precise (1% or better 0.5%).

Several runs have been made with automatic $Z$- and $B$-filter calculations.

5.1 Input File

Hereunder is a listing of our input file PBL 3762.INP with the measured values:

test (T: test => amplitude and phase of Kij;  x: normal calculation )

* $Z_f$:
  
  *ZfRA1, ZfCA1, ZfCA2, ZfRA2, ZfRS, ZfCS : impedance $Z_f$
  0. 0. 0 0. 20.2 0.

  *ZtRA1, ZtCA1, ZtCA2, ZtRA2, ZtRS, ZtCS : impedance $Z_t$
  598.E+03 0 0 0. 0. 0.

  *ZrRA1, ZrCA1, ZrCA2, ZrRA2, ZrRS, ZrCS : impedance $Z_r$
  300.E+03 0 0 0. 0. 0.

  CHP : capacitor for internal high pass
  10.18E-09

  *ZpRA1, ZpCA1, ZpCA2, ZpRA2, ZpRS, ZpCS : impedance $Z_p (=C_t=C_r)$
  0 0 0 0. 0. 2.24E-09

  CKX = Decoupling circuit in transmit direction (RAX)
  0.98E-06

  RIX = Decoupling circuit in transmit direction (RAX)
  23.7E+03

  RDC1        RDC2        CDC : DC path
  20.40E+03   20.4E+03   3.33E-06

  PRSG = Saturation guard (Yes = 7. no = 1.)
  1.

  *ZSLI = Half loop attenuation
  0.5

  *Zg : source/line impedance (with 6 elements)
  *ZgRA1, ZgCA1, ZgCA2, ZgRA2, ZgRS, ZgCS
  600. 0. 000.E-00 0. 000. 0.
C*******************************************************************
C      Initialisation part
C*******************************************************************
* internal data given by ERICSSON
FLP1 = 100.0
RHP  = 400.E+03
R2   = 20.
R3   = 9.98E+03
* other data
N10  = 10
OUT  = 6
IN   = 5
PI2  = 4.*ASIN(1.)
PI   = PI2/2.
FILEOUT = ''
INFILE = ''

C*******************************************************************
C      Inputs
C*******************************************************************
*
WRITE(OUT,'(A)')' Enter input file name :  '
50      READ (IN,'(A)') INFILE
IF ( INDEX(INFILE,' ').EQ.1  )  THEN
  WRITE (OUT,'(A)')' Enter correct input file name:  '
  INFILE=''
  GOTO 50
ENDIF
WRITE (OUT,'(A)') ' Enter output file name :  '
10      READ (IN,'(A)') FILEOUT
IF (INDEX(FILEOUT,' ').EQ.1) THEN
  WRITE (OUT,'(A)')' Enter correct output file name :  '
  FILEOUT=''
  GOTO 10
ENDIF
OPEN (30, FILE=FILEOUT, ERR=1000, STATUS= 'UNKNOWN')
*
WRITE(6,*)' READING input file...'
*
OPEN (10, FILE=INFILE, ERR=1100, STATUS= 'OLD')
READ(10,'(A)')
READ(10,'(A)') TEST
READ(10,'(A)')
READ(10,*') ZfR1,ZfC1,ZfC2,ZfR2,ZfRS,ZfCS
READ(10,'(A)')
READ(10,*') ZtR1,ZtC1,ZtC2,ZtR2,ZtRS,ZtCS
READ(10,'(A)')
READ(10,*') ZrR1,ZrC1,ZrC2,ZrR2,ZrRS,ZrCS
READ(10,'(A)')
READ(10,*') CHP
READ(10,'(A)')
READ(10,*') ZpR1,ZpC1,ZpC2,ZpR2,ZpRS,ZpCS
READ(10,'(A)')
READ(10,*') CKX
READ(10,'(A)')
READ(10,*') RIX
READ(10,'(A)')
READ(10,*) RDC1,RDC2,CDC
READ(10,'(A)')
READ(10,*) PRSG
READ(10,'(A)')
READ(10,'(A)')
READ(10,*) ZSLI
READ(10,'(A)')
READ(10,*) ZgR1,ZgC1,ZgC2,ZgR2,ZgRS,ZgCS
CLOSE (10)
C*******************************************************************
C             Documentation part
C*******************************************************************
C
WRITE (30,*) '* ERICSSON SLIC: ',INFILE
WRITE (30,*) '* Fuse impedance'
WRITE (30,*) '*ZfR1= ',ZfR1,'    ZfR2= ',ZfR2
WRITE (30,*) '*ZfC1= ',ZfC1,'    ZfC2= ',ZfC2
WRITE (30,*) '*ZfRS= ',ZfRS,'    ZfCS= ',ZfCS
WRITE (30,*) '* line/generator impedance'
WRITE (30,*) '*ZgR1= ',ZgR1,'    ZgR2= ',ZgR2
WRITE (30,*) '*ZgC1= ',ZgC1,'    ZgC2= ',ZgC2
WRITE (30,*) '*ZgRS= ',ZgRS,'    ZgCS= ',ZgCS
WRITE (30,*) '* matching impedance'
WRITE (30,*) '*ZtR1= ',ZtR1,'    ZtR2= ',ZtR2
WRITE (30,*) '*ZtC1= ',ZtC1,'    ZtC2= ',ZtC2
WRITE (30,*) '*ZtRS= ',ZtRS,'    ZtCS= ',ZtCS
WRITE (30,*) '* gain impedance'
WRITE (30,*) '*ZrR1= ',ZrR1,'    ZrR2= ',ZrR2
WRITE (30,*) '*ZrC1= ',ZrC1,'    ZrC2= ',ZrC2
WRITE (30,*) '*ZrRS= ',ZrRS,'    ZrCS= ',ZrCS
WRITE (30,*) '* parallel impedance at (a,b) line'
WRITE (30,*) '*ZpR1= ',ZpR1,'    ZpR2= ',ZpR2
WRITE (30,*) '*ZpC1= ',ZpC1,'    ZpC2= ',ZpC2
WRITE (30,*) '*ZpRS= ',ZpRS,'    ZpCS= ',ZpCS
WRITE (30,*) '* other data'
WRITE (30,*) '* RIX= ',RIX, '    CKX = ',CKX
WRITE (30,*) '* CHP= ',CHP, '    RHP = ',RHP
WRITE (30,*) '*RDC1= ',RDC1,'    RDC2= ',RDC2,
WRITE (30,*) '*PRSG= ',PRSG
WRITE (30,*) '*FCDC= ',FCDC
WRITE (30,*) ' FCHP = 1./(CHP*PI2*RHP)
FCDC  = 1./( CDC*PI2*(RDC1*RDC2)/(RDC1+RDC2) )
WRITE (30,*) '*FCHP= ',FCHP
WRITE (30,*) '*FCDC= ',FCDC
* test
IF (TEST.EQ.'T') then
   WRITE (*,'(100 Hz steps and Polar coordinates')
   N10 = 100
END IF
C*******************************************************************
C      Calculation part
C*******************************************************************
N399= (4000/N10)-1
*
WRITE (OUT,*) ' Running preliminary calculations...'
DO 123,I=1,N399
  FREQ = REAL(I*N10)
  call imped6(ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS,FREQ,Zg)
  call imped6(ZfR1,ZfR2,ZfC1,ZfC2,ZfRS,ZfCS,FREQ,Zf)
  call imped6(ZtR1,ZtR2,ZtC1,ZtC2,ZtRS,ZtCS,FREQ,Zt)
  call imped6(ZrR1,ZrR2,ZrC1,ZrC2,ZrRS,ZrCS,FREQ,Zr)
  call imped6(ZpR1,ZpR2,ZpC1,ZpC2,ZpRS,ZpCS,FREQ,Zp)
*  Zp is parallel at the output and connected to ground:
*  it must be doubled in our grounded model
  Zp = 2.*Zp
* open loop gain
  F  = 10000. / CMPLX(1.,FREQ/FLP1)
* X:
   c        IF (TYPE.EQ.3762) THEN
     X  =          1./                                     ( (1./cmplx(1.,-FCHP/FREQ) )
                 &     + (ZT*PRSG /( 20.*(RDC1+RDC2)*cmplx(1.,FREQ/FCDC)) ) )
   c        ELSE
     X  =          1./                                     ( (1./cmplx(1.,-FCHP/FREQ) )
                 &     + (ZT*PRSG / ( 20.*(RDC1+RDC2)*cmplx(1.,FREQ/FCDC)*cmplx(1.,FREQ/FCHP)) )
   c        ENDIF
* Yp
   Yp = 1./Zp
* RAX = j*ckx*rix*omega/1.+j*ckx*rix*omega :
* CKX = 0   => no filter
   IF (CKX.le.(1.e-12)) THEN
     RAX = CMPLX(1.,0)
   ELSE
     VAR1 = CMPLX(0,CKX*RIX*PI2*FREQ)
     RAX = VAR1/(1.+ VAR1)
   ENDIF
* Zload equivalent: Zeq = Zp//(Zf+Zg)
   Zeq = (Zp*(Zf+Zg))/(Zp+Zg+Zf)
* G
   G   =     ( R2*(1.+F) + F*R3 ) /
             ( R2*(1.+F) + Zeq )
* Zout
   Zout = ( ZT*X*R2*(1.+F) ) /
          & ( 2.*F*(R3+R2) + 2.*R2 + ZT*X )
   Yout = 1./Zout
* Zin
   ZIN = Zf + 1./( Yp+Yout )
K11 = \frac{(Z\text{IN}-ZG)}{(Z\text{IN}+ZG)}

C HP1 = j \cdot 2\pi \cdot \text{freq} \cdot \text{CHP} \cdot \text{RHP} / 1 + j \cdot 2\pi \cdot \text{freq} \cdot \text{CHP} \cdot \text{RHP}

\text{HP1} = \frac{1}{\text{CMPLX}(1.,(-\text{FCHP}/\text{FREQ}))}

* K12 = 2 \cdot \text{Gain 2w-4w (but difference of measuring point)}
K12 = \frac{(-2 \cdot (Zt/Zr) \cdot Zg/(Zg+Zf))}{(Zt/(2 \cdot G \cdot Zeq)) + (1/(X \cdot RAX))}

* K21 = \text{Gain 4w-2w with divider Zout, Zg, Zp, Zf}
Z1 = \frac{(Zp \cdot Zout)/(Zout + Zp)}{RAX \cdot \text{HP1} \cdot Z1/(Z1 + Zf+Zg)}

* K22 = \text{Gain 4w-4w}
K22 = \frac{-2 \cdot G \cdot RAX \cdot \text{HP1} \cdot \text{Zeq}/Zr}{1 + 2 \cdot G \cdot \text{Zeq}/(Zt \cdot X \cdot RAX)}

* write the tables
Z\text{INT}(i)=Z\text{IN}
K11\text{T}(i)=K11
K12\text{T}(i)=K12
K21\text{T}(i)=K21
K22\text{T}(i)=K22

* intermediate results
IF ( FREQ.EQ.300. 
& .OR.FREQ.EQ.1000. 
& .OR.FREQ.EQ.3000.) THEN
WRITE (*,*) '* FREQ:',INT(FREQ)
WRITE (*,999) '* Zin= ',Z\text{INT}(i)
ENDIF
123 CONTINUE

* if test, gives module and phase of Z\text{IN} as a function of frequency
IF (TEST.EQ.'T') THEN
WRITE (30,*)
& '* freq |ZIN| Phi(zin) '
DO 189 I=1,N399
FREQ = REAL(I*N10)
HAHA(1) = REAL(Z\text{INT}(i))
HAHA(2) = IMAG(Z\text{INT}(i))
CALL CPOL(HAHA,HAP)
DB= 20.*LOG10(HAP(1)+1.E-20)
PH= 360.*HAP(2)/PI2
WRITE (30,*) FREQ,HAP(1),PH
189 CONTINUE
ENDIF

* 777 FORMAT( A1,F7.1,2(F13.3),A3,2(F13.3) )
888 FORMAT( A1,F6.0,F10.1)
999 FORMAT( A7,G17.9,G17.9)
* WRITE (30,'(A)') 'Z\text{SLI}'
WRITE (30,'(G12.5)') Z\text{SLI}
WRITE (OUT,*) ' Running K11 calculation...'
WRITE (30,'(A)') ' K11-TABLE'
DO 100 I=1,N399
  FREQ = REAL(I*N10)
  HAHA(1)=REAL(K11T(i))
  HAHA(2)=IMAG(K11T(i))
  IF (TEST.EQ."T") THEN
    CALL CPOL(HAHA,HAP)
    DB= 20.*LOG10(HAP(1)+1.E-20)
    PH= 360.*HAP(2)/PI2
    WRITE (30,*) FREQ,DB,PH
  ELSE
    WRITE (30,*) FREQ,REAL(K11T(I)),IMAG(K11T(i))
  ENDIF
100 CONTINUE
C
IF (TEST.EQ."T") THEN
  WRITE (OUT,*) ' Running K12/2. calculation...'
  WRITE (30,'(A)') 'K12/2-TABLE'
ELSE
  WRITE (OUT,*) ' Running K12 calculation...'
  WRITE (30,'(A)') 'K12-TABLE'
ENDIF
DO 110 I=1,N399
  FREQ = REAL(I*N10)
  HAHA(1)=REAL(K12T(i))
  HAHA(2)=IMAG(K12T(i))
  IF (TEST.EQ."T") THEN
    CALL CPOL(HAHA,HAP)
    DB= 20.*LOG10(HAP(1)+1.E-20)
    PH= 360.*HAP(2)/PI2
    WRITE (30,*) FREQ,DB,PH
  ELSE
    WRITE (30,*) FREQ,REAL(K12T(I)),IMAG(K12T(i))
  ENDIF
110 CONTINUE
C
WRITE (OUT,*) ' Running K21 calculation...'
WRITE (30,'(A)') 'K21-TABLE'
DO 120 I=1,N399
  FREQ = REAL(I*N10)
  HAHA(1)=REAL(K21T(i))
  HAHA(2)=IMAG(K21T(i))
  IF (TEST.EQ."T") THEN
    CALL CPOL(HAHA,HAP)
    DB= 20.*LOG10(HAP(1)+1.E-20)
    PH= 360.*HAP(2)/PI2
    WRITE (30,*) FREQ,DB,PH
  ELSE
    WRITE (30,*) FREQ,REAL(K21T(I)),IMAG(K21T(i))
  ENDIF
120 CONTINUE
C
WRITE (OUT,*) ' Running K22 calculation...'
WRITE (30,'(A)') 'K22-TABLE'
DO 130 I=1,N399
  FREQ = REAL(I*N10)
HAHA(1)=REAL(K22T(i))
HAHA(2)=IMAG(K22T(i))
IF (TEST.EQ.'T') THEN
   CALL CPOL(HAHA,HAP)
   DB= 20.*LOG10(HAP(1)+1.E-20)
   PH= 360.*HAP(2)/PI2
   WRITE (30,*) FREQ,DB,PH
ELSE
   WRITE (30,*) FREQ,REAL(K22T(I)),IMAG(K22T(i))
ENDIF
130     CONTINUE
1111    CONTINUE
WRITE(30,'(A1)') ';
CLOSE (30)
WRITE(OUT,'(A)') ' Data written in file: '//FILEOUT
STOP
1000    WRITE(OUT,'(A)') ' OPEN ERROR AT OUTPUT-FILE: '//FILEOUT
STOP 1
1100    WRITE(OUT,'(A)') ' OPEN ERROR AT INPUT-FILE: '//INFILE
STOP 2
END
C
SUBROUTINE CPOL(Z,ZP)
   C
   NAME OF SUBROUTINE:     CPOL
   C
   FORMAL PARAMETER LIST:  Z,ZP
   C
   INPUT PARAMETERS:
   ZP      (DOUBLE)   ARRAY [2]
   C
   OUTPUT PARAMETERS:
   ZP      (DOUBLE)   ARRAY [2]
   C
   COMMON BLOCKS:
   P
   C
   Task of this routine:
   COORDINATE TRANSFORMATION  CARTESIAN --> POLAR
   C
   REQUIRED FUNCTIONS:
   ATAN,SQRT
   C
C
REAL  Z(2),ZP(2),PI,E,D
*
COMMON /QP/ PI
*
   ZP(1) = SQRT(Z(1)*Z(1)+Z(2)*Z(2))
   ZP(2) = ATAN(Z(2)/(Z(1)+1.0E-20))
Semiconductor Group

Application Notes II

E = Z(1)
D = Z(2)
IF (E) 1,4,4
1
IF (D) 2,2,3
2
ZP(2) = ZP(2) - π
RETURN
3
ZP(2) = ZP(2) + π
4
RETURN
END

C#
SUBROUTINE IMPED6(RP1, RP2, CP1, CP2, RS, CS, FREQ, Zeq)

C#
Note: when a parameter is set to 0 then the corresponding resistor or capacitance does not exist

C#
Formal parameter list: RP1, RP2, CP1, CP2, RS, CS, FREQ, Zeq

C#
Input parameters:
RS [ REAL ] ; series resistance
CS [ REAL ] ; series capacitance
RP1 [ REAL ] ; parallel resistance
RP2 [ REAL ] ; parallel resistance
CP1 [ REAL ] ; parallel capacitance
CP2 [ REAL ] ; parallel capacitance
FREQ [ REAL ] ; frequency

C#
Output parameters:
Zeq [ COMPLEX ]

C#
Common blocks: QPI2

C#
Task of this routine:Equivalent impedance of:

C#
SPECIAL CASES:
A. SYSTEM Parallel
1. CP1 not 0
   1.1 rp1 not 0

C#
1.2 rp1 = 0
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL CP1,CP2,RP1,RP2
REAL CS,RS,N,UL
REAL FREQ,PI2,OMEGA
COMPLEX D,C,Zeq,ZA,ZB
*
COMMON /PI2/ PI2
*
OMEGA = PI2*FREQ
IF (CP1.EQ.0) THEN
   C=CMPLX(RP1,0.)
ELSE
   C = RP1 + (1. / CMPLX(0.,OMEGA*CP1))
ENDIF
IF (CP2.EQ.0) THEN
   D=CMPLX(RP2,0.)
ELSE
   D = RP2 + (1. / CMPLX(0.,OMEGA*CP2))
ENDIF
ENDIF
N = CABS(C)
UL = CABS(D)
* if one of them is 0 then no parallel calculation
   IF ((N.EQ.0.).OR.(UL.EQ.0.)) then
     ZA=C+D
   ELSE
* ZA = C & D in parallel
     ZA=C*D/(C+D)
   ENDIF
C System series
   IF (CS .EQ.0) THEN
     ZB=CMPLX(RS,0.)
   ELSE
     ZB = RS + ( 1. / CMPLX(0.,OMEGA*CS))
   ENDIF
c both
   Zeq=ZA+ZB
RETURN
END
C
C###########################################################################c
5.2 Specification File

The SPEC file for 600 Ω specifications BUSA.SPE is following:

(Please notice: * A-Law and not μ-Law has been used
* The limit values of the trans-hybrid loss in DD spec have been set artificially higher than required so that the SICOFI program calculates coefficients which will give some margin between the required and the measured trans-hybrid loss)

**BUSA.SPE**

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**ZIN**

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**DA, DELAY**

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<th>Frequency</th>
<th>500</th>
<th>600</th>
<th>1k</th>
<th>2.6k</th>
<th>2.8k</th>
</tr>
</thead>
<tbody>
<tr>
<td>GD-</td>
<td>10k</td>
<td>.420</td>
<td>.150</td>
<td>.085</td>
<td>.150</td>
</tr>
<tr>
<td>GD+</td>
<td>.420</td>
<td>.150</td>
<td>.085</td>
<td>.150</td>
<td>10k</td>
</tr>
<tr>
<td></td>
<td>FR</td>
<td>AT-</td>
<td>AT+</td>
<td>FR</td>
<td>AT-</td>
</tr>
<tr>
<td>----------------</td>
<td>-----</td>
<td>------</td>
<td>------</td>
<td>-----</td>
<td>------</td>
</tr>
<tr>
<td><strong>AD, UPPER</strong></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>FR</td>
<td>300</td>
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<td>0.75</td>
<td>500</td>
<td>0.25</td>
</tr>
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<td>AT-</td>
<td>100</td>
<td>0.75</td>
<td>0.25</td>
<td>3.7k</td>
<td>0.35</td>
</tr>
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<td>AT+</td>
<td>0.75</td>
<td>0.25</td>
<td>0.35</td>
<td>3k</td>
<td>0.75</td>
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<td><strong>AD, LOWER</strong></td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>FR</td>
<td>300</td>
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<td>-0.25</td>
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<td>3.39k</td>
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<tr>
<td>AT+</td>
<td>-0.25</td>
<td>0</td>
<td>0</td>
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<td>0</td>
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<td><strong>AD, DELAY</strong></td>
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<td>1k</td>
<td>2.6k</td>
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<td>27</td>
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<td>27</td>
<td>23</td>
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<tr>
<td>AT+</td>
<td>23</td>
<td>27</td>
<td>27</td>
<td>0</td>
<td>0</td>
</tr>
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</table>
6 Measurement Results

The outputs of the SICOFI program are:

A byte file (PBL 3762.BYT) to be transferred to the SICOFI evaluation board. A result file (PBL 3762.RES) with all the coefficients, some comments about the SLIC (beginning with "**") and the calculated transfer functions.

The measurements on the following pages correspond well with the calculated values and the specifications are fulfilled.

**Byte file: PBL 3762.BYT**

```
PSR=36
CAM00=41
CAM20=40
CIW0=26,F4,80
CIW0=13,30,22,2A,6B,2B,22,B3,22
CIW0=23,F0,BC,37,72,49,36,0F,A6
CIW0=2B,F0,2B,97,74,2A,27,02,CE
CIW0=03,35,12,52,91,BF,9A,9,F4
CIW0=0B,00,33,AB,23,32,73,39,FA
CIW0=18,19,19,11,19
CIW0=30,61,B1,00,B4
SIG0=80
CIW0=26,F4,78
```

**Result file: PBL 3762.RES**

```
Input_file_name: PBL 3762.CTL            Date: 08.12.88  11:16
SPEC = BUSA.SPE                             SLIC = PBL 3762.SLI
BYTE = REF.BYT      CHNR = 0,A
PLQ  = N                     VERSION = V3.1          SHORT = N
ON = ALL                     OPT = Z+X+R+B               ZXRB = NNNN
PZIN= 11        ZLIM = 10.00
FZ =  300.00       3400.0        ZREP  =Y                           ZDIS  =  1
      500.00       7000.0       ZDIS  =  1
      1000.0       10000.       ZDIS  =  1
      1300.0       14000.       ZDIS  =  1
      1500.0

WFZ = .100         1.00         2.00         1.50         1.00
      3.00         1.00         1.00         1.00         3.00
      2.80         .230         1.00         1.00
      1.00
FZ =  300.00       3400.0        ZLIM = 10.00
      10000.       ZLIM = 10.00
FR =  200.00       3400.0
RDISP=  N             RREFQ = N       RREF =  .29230E-01
```
FX = 300.00 3400.0
XDISP= N XREFQ = N XREF = -.21669
BAUTO = Y
  PB = 10  GWFB= .500E-01 BDF = 1
FB = 300.00 500.00 700.0 1000.0 1500.0
2100.0 2300.0 2900.0 3200.0 3300.0
WFB = 4.0000 2.0000 1.0000 5.0000 1.0000
2.0000 1.0000 5.0000 1.0000 1.0000
FB = 300.00 3400.0 BLIM = 10.00 BDF = 1
BREP = Y BDIS = 1
AREC = 0.0 DREC = 0.0 AXMI = 0.0 DXMI = 0.0

XZQ = -.16406250E+00 .32031250E+00 .13183590E-01
-.30468750E+00 .16406250E+00
XRQ = .98535160E+00 .10253910E-01 .53710940E-02
.36621090E-02 -.65917970E-02
XXQ = .10117190E+01 .17562870E-01 .36621090E-02
.90332030E-02 .73852540E-02
XBQ = -.26550290E+00 -.49804690E+00 -.49316410E+00
.26171880E+00 .17187500E+00
-.24798580E+00 .34179690E-02 .28515630E+00
-.28906250E+00 .13867190E+00
XGQ = .51123050E+00 .20546880E+01

Bytes for Z-Filter (13): 30, 22, 2A, 6B, 2B, 22, B3, 22
Bytes for R-Filter (2B): F0, 2B, 97, 74, 2A, 27, 02, CE
Bytes for X-Filter (23): F0, BC, 37, 72, 49, 36, 0F, A6
Bytes for Gain-factors (30): 61, B1, 00, B4
2nd part of bytes B-Filter (0B): 00, 33, AB, 23, 32, 73, 39, FA
1st part of bytes B-Filter (03): 35, 12, 52, 91, BE, F9, A9, F4
Bytes for B-Filter delay (18): 19, 19, 11, 19

* ERICSSON SLIC ERIC.INP

* TEST= x

* Fuse impedance
  *ZfR1= 0.0000000E+00 ZfR2= 0.0000000E+00
  *ZfC1= 0.0000000E+00 ZfC2= 0.0000000E+00
  *ZfRS= 20.200000 ZfCS= 0.0000000E+00

* line/generator impedance
  *ZgR1= 600.000000 ZgR2= 0.0000000E+00
  *ZgC1= 0.0000000E+00 ZgC2= 0.0000000E+00
  *ZgRS= 0.0000000E+00 ZgCS= 0.0000000E+00

* matching impedance
  *ZtR1= 598000.000000 ZtR2= 0.0000000E+00
  *ZtC1= 0.0000000E+00 ZtC2= 0.0000000E+00
  *ZtRS= 0.0000000E+00 ZtCS= 0.0000000E+00

* gain impedance
*ZrR1=  300000.000000  ZrR2=  0.0000000E+00  
*ZrC1=  0.0000000E+00  ZrC2=  0.0000000E+00  
*ZrRS=  0.0000000E+00  ZrCS=  0.0000000E+00  

* parallel impedance at (a,b) line
*ZbR1=  0.0000000E+00  ZbR2=  0.0000000E+00  
*ZbC1=  0.0000000E+00  ZbC2=  0.0000000E+00  
*ZbRS=  0.0000000E+00  ZbCS=  2.2400000E-09

* other data
*RIX=  23700.000000  CIX =  9.8000000E-07  
*CHP=  1.0180000E-08  RHP =  400000.000000  
*RDC1=  20400.000000  RDC2=  20400.000000  CDC=  3.3300000E-06  
*PRSG=  1.0000000  
*FCHP=  39.085200  
*FCDC=  4.685713

RUN # 1

Z-FILTER calculation results
Reference impedance for optimization:

ZIRP1=  0.  ZICP1=  .000  ZIRP2=  0.  ZICP2=  .000  
ZIRS =  600.  ZICS =  .000

Calculated and quantized coefficients:

XZ =  -.16279  .31968  .01322  -.30409  .16758  
XZQ =  -.16406  .32031  .01318  -.30469  .16406

Bytes for Z-Filter (13):  30,22,2A,6B,2B,22,B3,22

RETURN LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>15.460</td>
<td>1800.</td>
<td>36.898</td>
</tr>
<tr>
<td>200.</td>
<td>21.477</td>
<td>1900.</td>
<td>36.337</td>
</tr>
<tr>
<td>300.</td>
<td>25.144</td>
<td>2000.</td>
<td>35.902</td>
</tr>
<tr>
<td>400.</td>
<td>27.876</td>
<td>2100.</td>
<td>35.599</td>
</tr>
<tr>
<td>500.</td>
<td>30.134</td>
<td>2200.</td>
<td>35.433</td>
</tr>
<tr>
<td>600.</td>
<td>32.130</td>
<td>2300.</td>
<td>35.412</td>
</tr>
<tr>
<td>700.</td>
<td>33.973</td>
<td>2400.</td>
<td>35.549</td>
</tr>
<tr>
<td>800.</td>
<td>35.716</td>
<td>2500.</td>
<td>35.860</td>
</tr>
<tr>
<td>900.</td>
<td>37.354</td>
<td>2600.</td>
<td>36.372</td>
</tr>
<tr>
<td>1000.</td>
<td>38.807</td>
<td>2700.</td>
<td>37.117</td>
</tr>
<tr>
<td>1100.</td>
<td>39.912</td>
<td>2800.</td>
<td>38.134</td>
</tr>
<tr>
<td>1200.</td>
<td>40.477</td>
<td>2900.</td>
<td>39.435</td>
</tr>
<tr>
<td>1300.</td>
<td>40.434</td>
<td>3000.</td>
<td>40.878</td>
</tr>
<tr>
<td>1400.</td>
<td>39.920</td>
<td>3100.</td>
<td>41.813</td>
</tr>
<tr>
<td>1500.</td>
<td>39.164</td>
<td>3200.</td>
<td>41.100</td>
</tr>
<tr>
<td>1600.</td>
<td>38.347</td>
<td>3300.</td>
<td>38.833</td>
</tr>
<tr>
<td>1700.</td>
<td>37.575</td>
<td>3400.</td>
<td>36.154</td>
</tr>
</tbody>
</table>

Min. Z-loop reserve:  5.315 dB
at frequency: 8500.0 Hz
Min. Z-loop mirror signal reserve: 9.927 dB
at frequency: 9000.0 Hz

Run # 1

X-FILTER calculation results

Reference impedance for optimization:
ZIRP1 = 0. ZICP1 = .000 ZIRP2 = 0. ZICP2 = .000
ZIRS = 600. ZICS = .000

Calculated and quantized coefficients:

XX = 1.01241 .01756 .00367 .00912 -.00740
XXQ = 1.01172 .01756 .00366 .00903 -.00739
Bytes for X-Filter (23): F0,BC,37,72,49,36,0F,A6

GX results:
All attenuation values (in dB) refer to FREF = 1004. Hz
RLX SLIC+Z VREF/VSICOFI XREF GX
.00 -.29 - 6.17 - -.22 = -6.25 ideal
-.01 = .29 + 6.17 + -.22 + -6.25 quant
Second byte for Gain: ,00,B4

Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1004.0 Hz

TGREF CA = .278 ms TGREF CB = .291 ms

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>14.017</td>
<td>2.890</td>
<td>2000.</td>
<td>.063</td>
<td>.010</td>
</tr>
<tr>
<td>200.</td>
<td>.419</td>
<td>1.880</td>
<td>2100.</td>
<td>.053</td>
<td>.016</td>
</tr>
<tr>
<td>300.</td>
<td>.061</td>
<td>.629</td>
<td>2200.</td>
<td>.041</td>
<td>.022</td>
</tr>
<tr>
<td>400.</td>
<td>.069</td>
<td>.309</td>
<td>2300.</td>
<td>.027</td>
<td>.030</td>
</tr>
<tr>
<td>500.</td>
<td>.055</td>
<td>.179</td>
<td>2400.</td>
<td>.015</td>
<td>.039</td>
</tr>
<tr>
<td>600.</td>
<td>.036</td>
<td>.112</td>
<td>2500.</td>
<td>.005</td>
<td>.049</td>
</tr>
<tr>
<td>700.</td>
<td>.020</td>
<td>.073</td>
<td>2600.</td>
<td>.000</td>
<td>.060</td>
</tr>
<tr>
<td>800.</td>
<td>.008</td>
<td>.049</td>
<td>2700.</td>
<td>.003</td>
<td>.073</td>
</tr>
<tr>
<td>900.</td>
<td>.001</td>
<td>.032</td>
<td>2800.</td>
<td>.015</td>
<td>.088</td>
</tr>
<tr>
<td>1000.</td>
<td>-.001</td>
<td>.021</td>
<td>2900.</td>
<td>.038</td>
<td>.105</td>
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<tr>
<td>1100.</td>
<td>.003</td>
<td>.013</td>
<td>3000.</td>
<td>.074</td>
<td>.126</td>
</tr>
<tr>
<td>1200.</td>
<td>.010</td>
<td>.008</td>
<td>3100.</td>
<td>.124</td>
<td>.151</td>
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<td>.021</td>
<td>.004</td>
<td>3200.</td>
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<td>.001</td>
<td>3300.</td>
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<td>.045</td>
<td>.000</td>
<td>3400.</td>
<td>.410</td>
<td>.277</td>
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<td>1600.</td>
<td>.056</td>
<td>.000</td>
<td>3500.</td>
<td>.596</td>
<td>.355</td>
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<tr>
<td>1700.</td>
<td>.065</td>
<td>.001</td>
<td>3600.</td>
<td>.906</td>
<td>.473</td>
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<td>.003</td>
<td>3700.</td>
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<td>.666</td>
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<tr>
<td>1900.</td>
<td>.068</td>
<td>.006</td>
<td>3800.</td>
<td>2.952</td>
<td>1.001</td>
</tr>
</tbody>
</table>
Run # 1

R-FILTER calculation results

Reference impedance for optimization:
ZIRP1 = 0. ZICP1 = 0.000 ZIRP2 = 0. ZICP2 = 0.000
ZIRS = 600. ZICS = 0.000

Calculated and quantized coefficients:
XR = 0.98529 0.01014 0.00518 0.00364 -0.00655
XRQ = 0.98535 0.01025 0.00537 0.00366 -0.00659

Bytes for R-Filter (2B): F0,2B,97,74,2A,27,02,CE

GR results:
All attenuation values (in dB) refer to FREF = 1004.0 Hz

<table>
<thead>
<tr>
<th>RLR</th>
<th>SLIC+Z</th>
<th>VSICOFI/VREF</th>
<th>RREF</th>
<th>GR</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00</td>
<td>-0.31</td>
<td>-6.17</td>
<td>-0.03</td>
<td>5.83 ideal</td>
</tr>
<tr>
<td>0.00</td>
<td>0.31</td>
<td>+6.17</td>
<td>+0.03</td>
<td>5.83 quant</td>
</tr>
</tbody>
</table>

First byte for Gain (30): 61,B1

Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF = 1004.0 Hz

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>-.319</td>
<td>0.000</td>
</tr>
<tr>
<td>200.</td>
<td>-.003</td>
<td>.113</td>
</tr>
<tr>
<td>300.</td>
<td>.049</td>
<td>.143</td>
</tr>
<tr>
<td>400.</td>
<td>.057</td>
<td>.155</td>
</tr>
<tr>
<td>500.</td>
<td>.050</td>
<td>.162</td>
</tr>
<tr>
<td>600.</td>
<td>.038</td>
<td>.167</td>
</tr>
<tr>
<td>700.</td>
<td>.025</td>
<td>.170</td>
</tr>
<tr>
<td>800.</td>
<td>.014</td>
<td>.173</td>
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<tr>
<td>900.</td>
<td>.005</td>
<td>.176</td>
</tr>
<tr>
<td>1000.</td>
<td>-.000</td>
<td>.179</td>
</tr>
<tr>
<td>1100.</td>
<td>-.001</td>
<td>.181</td>
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<tr>
<td>1200.</td>
<td>.002</td>
<td>.183</td>
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<tr>
<td>1300.</td>
<td>.010</td>
<td>.185</td>
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<tr>
<td>1400.</td>
<td>.020</td>
<td>.188</td>
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<tr>
<td>1500.</td>
<td>.031</td>
<td>.190</td>
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<tr>
<td>1600.</td>
<td>.042</td>
<td>.193</td>
</tr>
<tr>
<td>1700.</td>
<td>.052</td>
<td>.196</td>
</tr>
<tr>
<td>1800.</td>
<td>.058</td>
<td>.200</td>
</tr>
<tr>
<td>1900.</td>
<td>.061</td>
<td>.205</td>
</tr>
</tbody>
</table>

TGREF CA = .059 ms  TGREF CB = .042 ms

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000.</td>
<td>.060</td>
<td>.210</td>
</tr>
<tr>
<td>2100.</td>
<td>.055</td>
<td>.216</td>
</tr>
<tr>
<td>2200.</td>
<td>.046</td>
<td>.224</td>
</tr>
<tr>
<td>2300.</td>
<td>.035</td>
<td>.232</td>
</tr>
<tr>
<td>2400.</td>
<td>.023</td>
<td>.242</td>
</tr>
<tr>
<td>2500.</td>
<td>.012</td>
<td>.252</td>
</tr>
<tr>
<td>2600.</td>
<td>.004</td>
<td>.264</td>
</tr>
<tr>
<td>2700.</td>
<td>.001</td>
<td>.278</td>
</tr>
<tr>
<td>2800.</td>
<td>.004</td>
<td>.293</td>
</tr>
<tr>
<td>2900.</td>
<td>.016</td>
<td>.311</td>
</tr>
<tr>
<td>3000.</td>
<td>.039</td>
<td>.333</td>
</tr>
<tr>
<td>3100.</td>
<td>.074</td>
<td>.358</td>
</tr>
<tr>
<td>3200.</td>
<td>.125</td>
<td>.391</td>
</tr>
<tr>
<td>3300.</td>
<td>.200</td>
<td>.432</td>
</tr>
<tr>
<td>3400.</td>
<td>.309</td>
<td>.488</td>
</tr>
<tr>
<td>3500.</td>
<td>.480</td>
<td>0.566</td>
</tr>
<tr>
<td>3600.</td>
<td>.775</td>
<td>.685</td>
</tr>
<tr>
<td>3700.</td>
<td>1.365</td>
<td>.879</td>
</tr>
<tr>
<td>3800.</td>
<td>2.803</td>
<td>1.214</td>
</tr>
</tbody>
</table>
Run # 1

B-FILTER calculation results

Reference impedance for optimization:
ZLRP1 = 0. ZLCP1 = 0.000 ZLRP2 = 0. ZLCP2 = 0.000
ZLRS = 600. ZLCS = 0.000

Calculated and quantized coefficients:
XB = -0.26544 -0.49817 -0.49274 0.26327 -0.17247
    -0.24799 0.00340 0.28698 -0.28981 0.13867
XBP = -0.26550 -0.49805 -0.49316 0.26172 0.17188
     -0.24799 0.00342 0.28516 -0.28906 0.13867
2nd part of bytes B-Filter (0B): 00,33,AB,23,32,73,39,FA
1st part of bytes B-Filter (03): 35,12,52,91,BE,F9,A9,F4

TRANS HYBRID LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
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Additional B-filter delay (in seconds): .625E-04

Bytes for B-filter delay (18): 19,19,11,19
Figure 9

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**Figure 10**
Figure 11

Figure 12
7 Correlation

The same circuit has been tested for correlation between calculated and measured values with and without fuse resistors and with other specifications. We obtained a good correlation between measured results and calculated results.

BRD spec and fuse resistor (Zf = 20 Ω)
results: BF3.BYT

```
PSR=36
CAM00=41
CAM20=40
CIW0=26,F4,80
CIW0=13,C0,C1,C2,7B,19,2A,D1,2F
CIW0=23,70,CB,97,51,CA,5D,01,45
CIW0=2B,70,D3,AD,4B,25,3A,1D,12
CIW0=03,21,BA,7D,8B,54,4A,AC,B2
CIW0=0B,00,B2,91,CA,12,EC,4B,B9
CIW0=18,19,19,11,19
CIW0=30,A0,CF,10,B2
SIG0=80
CIW0=26,F4,78
```

The circuit as it is fulfills the requirement for Germany of –7 dB relative level in receive direction only with the version 4 and later of SICOFI (6 dB attenuation are necessary).

USA spec and no fuse resistor:
Results: PBL 3762.byf

```
PSR=36
CAM00=41
CAM20=40
CIW0=26,F4,80
CIW0=13,40,BC,FB,6C,12,33,CB,13
CIW0=23,70,29,77,75,19,26,07,36
CIW0=2B,F0,29,8F,7D,E8,E6,01,CE
CIW0=03,32,B1,13,90,2F,E9,A3,B6
CIW0=0B,00,33,AF,63,42,71,B8,EA
CIW0=18,19,19,11,19
CIW0=30,71,C8,00,26
SIG0=80
CIW0=26,F4,78
```
BRD.SPE with Fuse Resistor: BF3.BYT

Figure 13

Figure 14
USA.SPE without Fuse Resistor: PBL 3762.BYT

Figure 15

Figure 16
# SICOFI® Application Together with ST SLIC L3000/L3030

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1 Introduction

Due to the various existing technical realizations of the Subscriber Line Interface (SLIC) it is necessary to write a dedicated 'SLIC Program' for each SLIC type when calculating the SLIC parameters and simulating its transfer characteristics using e.g. the STS 2060 SICOFI Coefficients Program. This 'SLIC Program' generates an input file for the SICOFI Coefficients Program which in turn calculates the coefficients required for programming the SICOFI PEB 2060 or SICOFI-2 PEB 2260.

This application note refers to the SGS-Thomson SLIC L3030. Besides of some information about operating the SLIC and the SICOFI software, it contains the SLIC program written in FORTRAN. In the appendix the calculated and measured transfer functions according to specifications of the 'Deutsche Bundespost' are compared.

A SLIC-Babyboard answering these specifications has been designed by the HL IT Application Group of Siemens and is available under the name of STUS 3030. This board is compatible to our SICOFI-Testboard STUT 2060 and SICOFI-2-Board SIPB 5135.

2 Software Principle

The main functions of a Subscriber Line Interface Circuit (SLIC) are to provide the BORSHT functions (Battery feeding, Overvoltage protection, Ringing, Signaling, Hybrid function, Testing). In the case of a SLIC being used in combination with the SICOFI, the hybrid function is splitted into the two-wire to four-wire junction realized by the SLIC, and the impedance matching, hybrid balancing and gain adjustment provided by the internal filters of the SICOFI (see figure 1).

![Figure 1](image)

**Figure 1**

**SLIC-SICOFI® Hardware**

In a similar way, the software consists of two major sections: The SLIC description file (.SLI file) and the SICOFI program.
The other functions (such as off-hook detection, testing, standby mode, ringing) may also affect the speech signal, but will not be considered in the SLIC example described below.

2.1 SICOFI® Software

For modelling the SLIC, the complete SICOFI software structure is shown in detail in figure 3:
ST L3030.INP
The input file ST L3030.INP contains all data of the external circuitry and, in addition, the worst case loop attenuation at the four-wire SLIC side. Representation of numerical values is left to the user.

ST L3030.EXE
Using the input file ST L3030.INP, the SLIC program ST L3030.EXE calculates the transfer functions of the SLIC. It is written in FORTRAN.

ST L3030.SLI
ST L3030.SLI is the output file of the SLIC program ST L3030.EXE. In the main part it contains a table of the M-parameters of the SLIC calculated in dependence of frequency. At the top of the file the external components and the worst case loop attenuation are included.

Auxiliary Files:
COUNTRY.SPE:
COUNTRY.SPE is an input file to the SICOFI program describing the particular customer specifications (CCITT etc ...) and measurement configuration parameters (e.g. termination impedance).

REF.BYT
REF.BYT is another input file to the SICOFI program defining a frame into which the SICOFI program can write the newly calculated coefficients together with some predefined commands (required for sending the SICOFI coefficients from the Peripheral Board Controller PBC (PEB 2050) to the SICOFI and to store them in a USER.BYT file).

SICOFI.CTL
SICOFI.CTL is the control file of the SICOFI program. It contains the data controlling the optimization and simulation processes.

The SICOFI program SICOFI.BAT generates the SICOFI coefficients and simulates the theoretical transfer functions of the set SLIC + SICOFI.

RESULT.RES
RESULT.RES is the output file of the SICOFI program. It contains the coefficients for programming the SICOFI and a list of the calculated transfer characteristics of the set SLIC + SICOFI such as return loss, frequency response, echo return loss, etc ...
2.2 SLIC Software

According to its functionality the SLIC operates as a three-port. To describe its electrical properties five parameters are used in the SICOFI program: The four Mixed-Matrix-parameters (M-parameters) and the attenuation of the loop Z-filter/SLIC (ZSLI-value).

2.2.1 M - Parameter

The SLIC and its external circuitry may be represented as a three-port (c.f. figure 4).

![SLIC and its External Circuitry as a Three Port](https://via.placeholder.com/150.png)

**Figure 4**

**SLIC and its External Circuitry as a Three Port**

$I_1$, $I_2$ and $I_3$ are port currents and $V_1$, $V_2$ and $V_3$ are port voltages. This circuit can be described by the following equation system:

1. \( I_1 = M_{11} \times V_1 + M_{12} \times V_3 + M_{13} \times I_2 \)
2. \( V_2 = M_{21} \times V_1 + M_{22} \times V_3 + M_{23} \times I_2 \)
3. \( I_3 = M_{31} \times V_1 + M_{32} \times V_3 + M_{33} \times I_2 \)

Simplifications:

When the SLIC is connected to the SICOFI, we can assume that:

- $I_2 = 0$ because of the high SICOFI input impedance. (In special cases the SICOFI input impedance can be included in the three-port model).

- $I_3$ is not relevant in the following calculations because the SICOFI works as an ideal voltage generator. (The SICOFI output impedance of about 10 $\Omega$ may be included in the SLIC model).
According to the above agreements the equation system can be reduced to a pair of equations containing just four M-parameters:

\[
\begin{align*}
I_1 & = M_{11} \times V_1 + M_{12} \times V_3 \\
V_2 & = M_{21} \times V_1 + M_{22} \times V_3
\end{align*}
\]

These parameters \(M_{11}, M_{12}, M_{21}, M_{22}\) fully describe the SLIC and its external circuitry. They are defined as shown in figures 5 through 8.

Please verify that circuits of figures 5 and 7 and of figures 6 and 8 respectively are identical!

---

**Figure 5**

Definition of SLIC M11-Parameter
Figure 6
Definition of SLIC M12-Parameter

Figure 7
Definition of SLIC M21-Parameter
ZSLI is the minimal attenuation (resp. maximal gain) at the SLIC 4-wire side (Z-filter/SLIC loop).

ZSLI is used by the SICOFI program during automatic calculation of Z-filter coefficients as a reference to check for possible oscillations in the SICOFI Z-filter + SLIC loop.

The value will be given in dB and is expressed as attenuation:

\[ \text{ZSLI} = -20 \times \log\left(\frac{V_2}{V_3}\right) \]

→ Please verify that as \( V_2 \) is larger than \( V_3 \), ZSLI is a negative quantity.

**Note:** According to the Nyquist criteria, the attenuation of the closed loop "Z filter - SLIC" must be greater than 1 (gain < 0 dB) in the frequency band 0 – 16 kHz in order to avoid any oscillation.
3  SGS-Thomson SLIC L3030

The SGS-Thomson SLIC connects the SICOFI via the a,b lines to the subscriber. It has the following functions:

- Battery feeding
- Hybrid
- Ringing
- Ground-key detection
- OFF/ON-hook-detection
- Teletex signal injection

The SLIC divides into two parts, a low voltage part (L3030) and a high voltage part (L3000).

3.1 High Voltage Part L3000

The high voltage part is connected to the line. It realizes the battery feeding and switches the ringing and the speech signals in both directions through the SLIC.

The line current is programmable to 4 threshold values (25 mA, 30 mA, 45 mA, and 70 mA). An internal temperature sensing part shuts the line current off, when the temperature threshold is exceeded. The ringing signal is supplied by the battery on a small AC control-voltage (0.285 Vrms) at pin 26. The ringing signal starts and stops when the control signal crosses zero. The control signal is amplified and fed in balanced mode to the line with a superimposed DC voltage of 22 V.

3.1.1 DC Characteristics

In conversation mode the SLIC can work in Normal Battery or Boost Battery mode; with bit 3 of the signaling byte it is also possible to select the polarity of the DC line voltage. These possibilities have no influence on the transfer functions. In all these states the SLIC may operate as current generator, standard feeding system or as low impedance system.

a) Current generator

In this case the impedance of the SLIC is very high (> 20 kΩ) and the SLIC can supply currents of 25 mA, 30 mA, 45 mA, or 70 mA.

b) Standard feeding system

In this case the characteristic is equal to a – 48 V battery in series with two resistors, the values of which are set by external components.

c) Low impedance system

In this case the battery voltage is reduced to 33 V and the series resistors are reduced, too. With ‘Boost Battery’ this region cannot be reached.

These three working ranges are shown in figure 10 below; the DC characteristic is selected by the resistor \( R_{DC} \).
\[ R_{DC} = 2 \times (R_{FS} - R_{P1}) \text{ with } R_{P1} = R_{P2} \]

**Figure 10**

DC Characteristics \( I_{\text{lim}} = 25/30/45/70 \text{ mA} \)

The resistor \( R_{DC} \) is to be used only in sections 1 and 2, and is infinite in section 3.

The value of \( R_{DC} \) influences also the internal block called K ("kernel"). In sections 2 and 3 the value of K equals K = 4/5 and in section 1 K = 5/12. The SLIC program already provides these two values. You only have to put the value of \( R_{DC} \) into the input file (see section 4.1).

### 3.1.2 AC Characteristics of the ST-SLIC

The ST-SLIC needs a large capacitance to block the DC from the 4-wire side of the SLIC. To save space and cost, the ST has a built-in capacitance multiplier. Thus the user requires just two small capacitors and a single resistor.

#### 3.1.2.1 Model without Capacitor Multiplier

When not using the capacitor multiplier the customer needs only \( C_{AC1} \) and a connection between pins 7 and 14. The value of the (external) capacitor \( C_{AC1} \) is 47 \( \mu \text{F} \).
Note: \( K \) is dependent on the value \( R_{dc} \) (see section 3.1.1)

### 3.1.2.2 Model with Capacitor Multiplier

When using the capacitor multiplier you need \( C_{AC1}, C_{AC2} \) and \( R_R \). The connection between pins 7 and 14 is shut off. The values used on the SLIC Babyboard STUS 3030 are:

\[
\begin{align*}
C_{AC1} &= 1 \, \mu F \\
C_{AC2} &= 1 \, \mu F \\
R_R &= 50 \, k\Omega
\end{align*}
\]

With the above values the effective capacitance (to be used by the SLIC program) is 22 \( \mu F \) (see application note of ST-SLIC. – In the SLIC model of figure 11 no multiplier is used).
3.2 Low Voltage Part L3030
The low voltage part controls the high voltage part L3000 in giving the proper information for setting line feed characteristics and injecting ringing and TTX signals. An on-chip digital interface (see below) allows to control all these operations. The L3030 defines working states of the line interface and also informs the controller via the SLD-bus about the line status.

3.3 Digital Interface
The Digital Interface has 5 pins:
- E/A read/write command
- NCS chip select
- DIO data input/output
- DCLK clock signal
- C1 changing NCS signal from input to output:
  - in serial mode NCS is an input
  - in parallel mode NCS is an output

The Digital Interface is connected via a discrete logic to the SLD-interface.

The Digital Interface may work in serial or parallel mode.

The interface works in **serial mode** by connecting pin 21 to ground. Only in this mode all features of the SLIC (power-down, ringing, teletex signal, current setting) are available.

Because the timing of the ST-SLIC is different from that of the SICOFI, these two devices have to be connected via a discrete logic. A 3.3 kΩ resistor is inserted between the SIP-pin of the SICOFI and the SIP-wire, because the SLIC sends its last data when the SICOFI sends data too.

C1 of the SLIC must be fixed to ground because NCS is only an input. DIO is connected to the SIP-wire. All other interface pins are connected to the discrete logic.

**Figure 12** shows a block diagram of an analog line card supplying 16 subscribers using the ST-SLIC together with SICOFI, PBC and discrete logic. You can find the circuit diagram of the discrete logic in **figure 13**.

The **parallel mode** is chosen when a voltage higher than 4 V is put to pin 21.

The SLIC of the SLIC Babyboard STUS 3030 can work both with the serial interface or with the parallel interface. The serial interface, however, works only in connection with the SICOFI Testboard STUT 2060, because the discrete logic needs a signal 'SIGS' from the PBC. On the other hand, if the SICOFI-2 Board SIPB 5135 is used, the board works only with the parallel interface. It is selected by two jumpers (**not shown in figures 12 and 13**).
Figure 12

Block Diagram of an Analog Line Card Supplying 16 Subscribers
Figure 13
Discrete Logic for 16 Subscribers
3.4 Programming the ST-SLIC

The serial input port of the SLIC is connected to the SIP-lines of the Peripheral Board Controller (PBC) PEB 2050 and SICOFI. The discrete logic generates a chip select signal for the SLIC when the signaling byte is sent on the line. In this case the customer can use the signaling byte to program the SLIC.

Attention: Be aware of rotating the bit sequence of the signaling byte, because the PBC starts sending bit 7 ahead while the SLIC needs at first bit 0.

For example:

SIG0 = 80 power-up and line current \( I = 25 \, \text{mA} \)
SIG0 = 81 power-up and line current \( I = 30 \, \text{mA} \)
SIG0 = 82 power-up and line current \( I = 70 \, \text{mA} \)
SIG0 = 83 power-up and line current \( I = 45 \, \text{mA} \)

You have to program the SCR register of the PBC to generate a signal at the SIGS-pin of the PBC. With this signal the discrete logic creates a chip select signal for the particular SLIC:

SLIC-A  SCR = 90
SLIC-B  SCR = 50

Note: With a single PBC just two SLICs are to be controlled.

4 Calculations and Results

4.1 Calculations on the SLIC

The SLIC program requires an input file containing the values of the external circuitry for calculating the M-parameters which are written to a SLIC-file. This serves as an input file to the SICOFI program and thus you are able to calculate the SICOFI coefficients.

In receive direction the SLIC amplifiers the incoming signal and therefore it must be attenuated by the SICOFI. Because the required attenuation (\( > 12 \, \text{dB} \)) exceeds the possibilities of the SICOFI at its digital side, you need a voltage divider in receive direction or the analog attenuation of the SICOFI must be preset to 6 dB (AGR = 01).

The ST-SLIC has several external components:

\[
\begin{align*}
Z_A & \quad \text{SLIC impedance balancing network} \\
Z_B & \quad \text{line impedance balancing network} \\
Z_{AC}, C_{AC1} & \quad \text{DC feeding system, AC blocking and} \\
R_{DC}, R_{PC} & \quad \text{impedance matching} \\
R_{REF} & \quad \text{bias resistance} \\
C_{INT} & \quad \text{time constant}
\end{align*}
\]
You do not need the $Z_A$-network!! Set $Z_B$ to 10 kΩ and let the B-filter of the SICOFI make the balancing.

The components $R_{\text{REF}}$ and $C_{\text{INT}}$ do not influence the transfer functions and hence may be neglected. All other components are to be gathered into the input file. The capacitor $C_{\text{AC1}}$ is taken with its actual value when the multiplier is not used; when the multiplier is used, a value of 22 µF has to be used in the input file.

The calculated M-parameters are:

\[
\begin{align*}
M_{11} &= 1/Z_{ML} \\
M_{12} &= 2 \times AR/Z_{ML} \\
M_{21} &= AX \\
M_{22} &= 2 \times AX + AR \times Z_B/(Z_A + Z_B) \\
Z_{ML} &= (R_{DC} + R_{PC}) \times (1 + jw \times C \times R_{DC}) \times ((Z_{AC} \times R_{PC})/(R_{DC} + R_{PC})) / (1 + jw \times C \times R_{DC})
\end{align*}
\]
### 4.2 Format of the SICOFI® Input File

The SLIC program writes a table to the output file ST L3030.SLI. This output is the SICOFI input file. An example of this file is listed below:

```
* ST SLIC L3030
* VOR = .50000  RIR = .10000E+06  CKR = .00000
* VOX = 1.00000  RIX = 10000.  CKX = .10000E-05
* RP1ZA = .00000  RP1A = .00000  RP1P = .00000
* CP1ZA = .00000  CP1A = .00000  CP1B = .00000
* RSZAC = 500.00  RSA = .50000E+08  RSB = 1000000
* CSZAC = .00000  CSA = .00000  CSB = .00000
* RPC = 100.00  RDC = 300.00  CAC = .22000E-04
* CCOMP = .68000E-07
ZSLI
1.0000
M11-TABLE
10.000000000000000  2.265894E-03  -3.723228E-04
20.000000000000000  1.991187E-03  -4.019077E-04
30.000000000000000  1.849926E-03  -3.384906E-04
. . .
3980.000000000000000  1.827491E-03  1.151429E-03
3990.000000000000000  1.828295E-03  1.154225E-03
M12-TABLE
10.000000000000000  2.265894E-03  -3.723228E-04
20.000000000000000  1.991187E-03  -4.019077E-04
30.000000000000000  1.849926E-03  -3.384906E-04
. . .
3980.000000000000000  1.827491E-03  1.151429E-03
3990.000000000000000  1.828295E-03  1.154225E-03
M21-TABLE
10.000000000000000  2.830432E-01  4.504772E-01
20.000000000000000  1.122734E-01  4.872317E-01
30.000000000000000  1.803674E-01  4.139977E-01
. . .
3980.000000000000000  9.999840E-01  3.998804E-03
3990.000000000000000  9.999841E-01  3.988782E-03
M22-TABLE
10.000000000000000  5.659732E-05  9.007743E-05
20.000000000000000  1.224302E-04  9.742685E-05
30.000000000000000  1.560423E-04  8.278299E-05
. . .
3980.000000000000000  1.999568E-04  7.996009E-07
3990.000000000000000  1.999568E-04  7.975970E-07
```
The leading comment lines (beginning with "+") document which SLIC is used. The first column of the M-parameter tables indicates the frequency value, from 10 to 3990 Hz in steps of 10 Hz. The second and the third columns give the real and imaginary part values respectively.

When modifying the .SLIC-file please note that these three values are separated by at least a single space character; every real number must contain a decimal point (FORTRAN "REAL" format).

4.3 Results

The SLIC was calculated using the parameters 'ST L3030.SLI' of the SLIC program (ST L3030.EXE) in ST L3030.INP, and coefficients were calculated. The result file of the SICOFI program was stored in 'ST L3030.RES' and the calculated programming bytes in 'ST L3030.BYT'.

With these bytes the SICOFI has been programmed and measurements have been taken with a "PCM4" of Wandel & Goltermann, using the SLIC board plugged into the STUT 2060 test board as shown in appendix D. The measurements comprise the levels in transmit direction (AD) and in receive direction (DA), the attenuation distortion (AD and DA), the transhybrid loss (DD), and the 2-wire impedance return loss.

The plots of measurements can be found in appendix E.

The plot masks correspond to CCITT Recommendations G.712 and G.714.

4.4 Comparison of Measurements and Simulations

Measurements have been taken on a SLIC L3030 including the capacitance multiplier. In general the measurements conform with the calculations within small differences. Only the high attenuation of calculated echo return loss could not be reached experimentally.
Appendix A: Input File 'ST L3030.INP'

VOR= 0.5
RIR= 100.E03
CKR= 0.
VOX= 1.0
RIX= 10000.
CKX= 1.0E-06
RP1ZAC= 0.
RP2ZAC= 0.
CP1ZAC= 0.0
CP2ZAC= 0.
RSZAC= 500.
CSZAC= 0.
RP1A= 0.
RP2A= 0.
CP1A= 0.
CP2A= 0.
RSA= 50.E06
CSA= 0.
RP1B= 0.
RP2B= 0.
CP1B= 0.
CP2B= 0.
RSB= 10000.
CSB= 0.
RPC= 100.
Appendix B: Program 'ST L3030.FOR'

C###################################################################
# PROGRAM SGS
C     08.06.90  Udo Stueting
C###################################################################
#
* IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
INTEGER IN,OUT,I
CHARACTER*14 BUFF1,BUFF2*7,BUFF3*7,BUF4*7,BUF5*7
CHARACTER*7 BUF6,BUF7*7,BUF8*7,BUF9*7,BUF2*12,BUF3*12
    CHARACTER*7 BUFT10*7,BUF11*7,BUF12*7,BUF13*7,BUF14*7,BUF15*7
CHARACTER*7 BUFT16*7,BUF17*7,BUF18*7,BUF19*7,BUF20*7,BUF21*7
CHARACTER*7 BUFT22*7,BUF23*7,BUF24*7,BUF25*7,BUF26*7,BUF 27*7
CHARACTER*7 BUFT28*7,BUF29*7,BUF30*7,BUF31*7
CHARACTER  BUF1*12,FILEOUT*12,ANSW*1,INFILE*12
REAL*8 FREQ
REAL*8 VOR,RIR,CKR,VOX,RIX,CKX,PI2,ZSLI
REAL*8 P1A,RP2A,CPIA,CP2A,RSA,CSA,RP1B,RP2B,CP1B,CP2B,RSB,CSB
REAL*8 RP1ZAC,RP2ZAC,CPIZAC,CP2ZAC,RSZAC,CSZAC
REAL*8 RPC,RDC,CAC,CCOMP,RGTTX
COMPLEX*8 M11,M12,M21,M22,Z,ZA,ZB,ZAC,ZML,AX,AR,ZN,TTX
*
    COMMON /ARC/  RIR,CKR,VOR
    COMMON /AXC/  RKX,CKX,VOX
    COMMON /PI2C/ PI2
    COMMON /SGSC/ RPC,RDC,CAC,CCOMP
    COMMON /ZACC/RP1ZAC,RP2ZAC,CPIZAC,CP2ZAC,RSZAC,CSZAC
    COMMON /ZAC/  RP1A,RP2A,CPIA,CP2A,RSA,CSA
    COMMON /ZBC/  RP1B,RP2B,CP1B,CP2B,RSB,CSB
C      ONLY FOR TTX-Filter (PIN 34 of L3030)
    COMMON /TTXC/ RGTTX
C
C**************************************************************
C Initialization part
C**************************************************************
C
DATA BUFF1/* ST SLIC L3030 */
DATA BUFF2/* VOR ='/,BUF3/* RIR ='/,BUF4/* CR ='/
DATA BUFF5/* VOX ='/,BUF6/* RIX ='/,BUF7/* CKX ='/
DATA BUFF8/* RP1ZAC ='/,BUF9/* RP1A ='/BUFF10/* RP1B ='/
DATA BUFF11/* RP2ZAC ='/,BUF12/* RP2A ='/BUFF13/* RP2B ='/
DATA BUFF14/* CP1ZAC ='/,BUF15/* CP1A ='/BUFF16/* CP1B ='/
DATA BUFF17/* CP2ZAC ='/,BUF18/* CP2A ='/BUFF19/* CP2B ='/
DATA BUFF20/* RSZAC ='/,BUF21/* RSA ='/BUFF22/* RSB ='/
DATA BUFF28/* CSZAC ='/,BUF29/* CSA ='/BUFF30/* CSB ='/
DATA BUFF23/* RPC ='/,BUFF24/* RDC ='/BUFF25/* CAC ='/
DATA BUFF27/* CCOMP ='/
C ONLY FOR TTX-Filter (PIN 34 of L3030)
C DATA BUFF27/* CCOMP ='/,BUFF31/* RGTTX ='/
DATA BUFF26/* ZSLI ='/
*
OUT = 6
IN = 5
PI2 = 4.*DASIN(1.D0)
FILEOUT = ' ',
WRITE (OUT,'(A)')
& ' Enter input file name(xxxxxxxx.INP): ' 10
READ (IN,'(A)') INFILE
IF (INDEX(INFILE,'').EQ.1
& .OR.(INDEX(INFILE,'.INP').EQ.0
& .AND.(INDEX(INFILE,'.inp').EQ.0)) THEN
WRITE (OUT,'(A)') ' Enter correct input file name:
',
INFILE = ' ',
GOTO 10
ENDIF
WRITE (OUT,'(A)') ' Enter output file name (xxxxxxxx.SLI): ' 20
READ (IN,'(A)') FILEOUT
IF (INDEX(FILEOUT,'').EQ.1 THEN
WRITE (OUT,'(A)') ' Enter correct output file name (with extension .SLI): ' 20
FILEOUT = ' ',
GOTO 20
ENDIF
OPEN (30, FILE=FILEOUT, ERR=1000, STATUS= 'UNKNOWN')
OPEN (10, FILE=INFILE, ERR=1100, STATUS= 'OLD')
READ(10,'(A)')
WRITE(6,*) 'Reading input file'
READ(10,*) VOR
READ(10,'(A)')
READ(10,* RIR
READ(10,'(A)')
READ(10,* CKR
READ(10,'(A)')
READ(10,* VOX
READ(10,'(A)')
READ(10,* RIX
READ(10,'(A)')
READ(10,* CKX
READ(10,'(A)')
READ(10,* RP1ZAC
READ (10, ‘(A)’)
READ (10, *) RP2ZAC
READ (10, ‘(A)’)
READ (10, *) CP1ZAC
READ (10, ‘(A)’)
READ (10, *) CP2ZAC
READ (10, ‘(A)’)
READ (10, *) RSZAC
READ (10, ‘(A)’)
READ (10, *) CSZAC
READ (10, ‘(A)’)
READ (10, *) RP1A
READ (10, ‘(A)’)
READ (10, *) RP2A
READ (10, ‘(A)’)
READ (10, *) CP1A
READ (10, ‘(A)’)
READ (10, *) CP2A
READ (10, ‘(A)’)
READ (10, *) RSA
READ (10, ‘(A)’)
READ (10, *) CSA
READ (10, ‘(A)’)
READ (10, *) RP1B
READ (10, ‘(A)’)
READ (10, *) RP2B
READ (10, ‘(A)’)
READ (10, *) CP1B
READ (10, ‘(A)’)
READ (10, *) CP2B
READ (10, ‘(A)’)
READ (10, *) RSB
READ (10, ‘(A)’)
READ (10, *) CSB
READ (10, ‘(A)’)
READ (10, *) RPC
READ (10, ‘(A)’)
READ (10, *) RDC
READ (10, ‘(A)’)
READ (10, *) CAC
READ (10, ‘(A)’)
READ (10, *) CCOMP
READ (10, ‘(A)’)
C ONLY FOR TTX-Filter (PIN 34 of L3030)
C READ(10,*) RGTTX
C READ(10,‘(A)’)
READ (10, *) ZSLI
CLOSE (10)
WRITE (30,'(A)') BUFF1
WRITE (BUFF1,'(G12.5)') VOR
WRITE (BUFF2,'(G12.5)') RIR
WRITE (BUFF3,'(G12.5)') CKR
WRITE (30,'(A)') BUF2//BUFF1//BUF3//BUF2//BUF4//BUFF3
WRITE (BUFF1,'(G12.5)') VOX
WRITE (BUFF2,'(G12.5)') RIX
WRITE (BUFF3,'(G12.5)') CKX
WRITE (30,'(A)') BUF5//BUFF1//BUF6//BUF2//BUF7//BUFF3
WRITE (BUFF1,'(G12.5)') RP1ZAC
WRITE (BUFF2,'(G12.5)') RP1A
WRITE (BUFF3,'(G12.5)') RP1B
WRITE (30,'(A)') BUF8//BUFF1//BUF9//BUF2//BUF10//BUFF3
WRITE (BUFF1,'(G12.5)') RP2ZAC
WRITE (BUFF2,'(G12.5)') RP2A
WRITE (BUFF3,'(G12.5)') RP2B
WRITE (30,'(A)') BUF11//BUFF1//BUF12//BUF2//BUF13//BUFF3
WRITE (BUFF1,'(G12.5)') CP1ZAC
WRITE (BUFF2,'(G12.5)') CP1A
WRITE (BUFF3,'(G12.5)') CP1B
WRITE (30,'(A)') BUF14//BUFF1//BUF15//BUF2//BUF16//BUFF3
WRITE (BUFF1,'(G12.5)') CP2ZAC
WRITE (BUFF2,'(G12.5)') CP2A
WRITE (BUFF3,'(G12.5)') CP2B
WRITE (30,'(A)') BUF17//BUFF1//BUF18//BUF2//BUF19//BUFF3
WRITE (BUFF1,'(G12.5)') RSZAC
WRITE (BUFF2,'(G12.5)') RSA
WRITE (BUFF3,'(G12.5)') RSB
WRITE (30,'(A)') BUF20//BUFF1//BUF21//BUF2//BUF22//BUFF3
WRITE (BUFF1,'(G12.5)') CSZAC
WRITE (BUFF2,'(G12.5)') CSA
WRITE (BUFF3,'(G12.5)') CSB
WRITE (30,'(A)') BUF28//BUFF1//BUF29//BUF2//BUF30//BUFF3
WRITE (BUFF1,'(G12.5)') RPC
WRITE (BUFF2,'(G12.5)') RDC
WRITE (BUFF3,'(G12.5)') CAC
WRITE (30,'(A)') BUF23//BUFF1//BUF24//BUF2//BUF25//BUFF3
WRITE (BUFF1,'(G12.5)') CCOMP
WRITE (30,'(A)') BUF27//BUFF1
WRITE (BUFF2,'(G12.5)') RGTTX
WRITE (30,'(A)') BUF27//BUFF1//BUF31//BUFF2
WRITE (30,'(A)') 'ZSLI'
WRITE (30,'(G12.5)') ZSLI
C*******************************************************************
C      Calculation part
C*******************************************************************
C
C        M11 = 1. / ZML
C
ZM = CMPLX(1.,0.)
WRITE (OUT,*) ’ Running M11 calculation...’
WRITE (30,’(A)’) ’M11-TABLE’
DO 100 I=1,399
   FREQ = DBLE(I*10)
   CALL YZML(FREQ,ZML)
   M11 = ZM / ZML
   WRITE (30,*) FREQ,REAL(M11),AIMAG(M11)
100     CONTINUE
C
C        M12 = 2.0*AR/ZML
C
WRITE (OUT,*) ’ Running M12 calculation...’
WRITE (30,’(A)’) ’M12-TABLE’
DO 110 I=1,399
   FREQ = DBLE(I*10)
   CALL ARW(FREQ,AR)
   CALL YZML(FREQ,ZML)
   M12 = 2. * AR / ZML
   WRITE (30,*) FREQ,REAL(M12),AIMAG(M12)
110     CONTINUE
C
C        M21 = AX * TTX
C
WRITE (OUT,*) ’ Running M21 calculation...’
WRITE (30,’(A)’) ’M21-TABLE’
DO 120 I=1,399
   FREQ = DBLE(I*10)
   CALL AXW(FREQ,AX)
   CALL TTXW(FREQ,TTX)
   M21 = AX * TTX
   WRITE (30,*) FREQ,REAL(M21),AIMAG(M21)
120     CONTINUE
C
C       M22 = 2*AX*TTX*AR*(ZB/(ZA+ZB))
C
WRITE (OUT,*) ’ Running M22 calculation...’
WRITE (30,’(A)’) ’M22-TABLE’
DO 130 I=1,399
   FREQ = DBLE(I*10)
   CALL AXW(FREQ,AX)
   CALL ARW(FREQ,AR)
   CALL YZA(FREQ,ZA)
   CALL YZB(FREQ,ZB)
   CALL TTXW(FREQ,TTX)
   M22 = 2. * AX * AR * TTX
   Z = ZB / (ZA+ZB)
   M22 = M22 * Z
   WRITE (30,*) FREQ,REAL(M22),AIMAG(M22)
CONTINUE
   WRITE(30,\'(A1)\') \';\'
   CLOSE (30)
WRITE(OUT,\'(A)\') ' Data written in file: '//FILEOUT
STOP
1000  WRITE(OUT,\'(A)\') ' OPEN ERROR AT OUTPUT-FILE: '//FILEOUT
      STOP 1
1100  WRITE(OUT,\'(A)\') ' OPEN ERROR AT INPUT-FILE: '//INFILE
      STOP 2
END
SUBROUTINE ARW(FREQ, AR)

IMPLICIT LOGICAL (A-K, M-Z), CHARACTER (L)
*
REAL*8 FREQ, RIR, CKR, VOR, OMP, PI2
COMPLEX AR, V1, V2
*
COMMON /ARC/ RIR, CKR, VOR
COMMON /PI2C/ PI2
*
AR = CMPLX(1., 0.)
IF (CKR.EQ.0) THEN
GOTO 10
ELSE
OMP = PI2*FREQ*RIR*CKR
V1 = CMPLX(0., OMP)
V2 = CMPLX(1.D0, OMP)
AR = V1 / V2
ENDIF
10 AR = AR*VOR
RETURN
END
SUBROUTINE AXW(FREQ,AX)

* Name of Subroutine: AXW
* Formal parameter list: FREQ, AX
* Input parameters:
  FREQ    (DOUBLE)
* Output parameters:
  AX      (DOUBLE) ARRAY 2
* Task of this routine:

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)

REAL*8 FREQ, RIX, CKX, VOX, OMP, PI2
COMPLEX AX, V1, V2

COMMON /AXC/ RIX, CKX, VOX
COMMON /PI2C/ PI2

AX = CMPLX(1.,0.)
IF (CKX.EQ.0) THEN
  GOTO 10
ELSE
  OMP = PI2*FREQ*RIX*CKX
  V1 = CMPLX(0., OMP)
  V2 = CMPLX(1.D0, OMP)
  AX = V1 / V2
ENDIF
10 AX = AX*VOX
RETURN
END
SUBROUTINE YZML(FREQ,ZML)

Name of Subroutine: YZML

Formal parameter list: FREQ

Input parameters:

Output parameters:

Common blocks:

Task of this routine:

Required subroutines:

Required functions:

Routine called in the following subroutines or functions:

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL*8 FREQ, RPC, CCOMP
REAL*8 RP1ZAC, RP2ZAC, CP1ZAC, CP2ZAC, RSZAC, CSZAC
REAL*8 RDC, CAC, PI2
COMPLEX ZAC, ZML, ZMLZ, ZMLN, ZML1, XC

* COMMON /PI2C/ PI2
* COMMON /SGSC/ RPC, RDC, CAC, CCOMP
* COMMON /ZACC/RP1ZAC, RP2ZAC, CP1ZAC, CP2ZAC, RSZAC, CSZAC

CALL IMPED6(RP1ZAC, RP2ZAC, CP1ZAC, CP2ZAC, RSZAC, CSZAC, FREQ, ZAC)
IF (CCOMP.EQ.0) THEN
  GOTO 10
ELSE
  XC = CMPLX(0., (-1./(PI2*FREQ*CCOMP)))
  ZML = ZAC * XC
  ZMLZ = ZAC + XC
  ZAC = ZML / ZMLZ
END IF

10  ZMLZ = ZAC + RPC
    ZMLN = RPC + RDC
    ZML1 = ZMLZ / ZMLN
    ZML = CMPLX(0., (PI2 * FREQ * CAC * RDC))
ZML = ZML1 * ZML
ZML = 1 + ZML
ZMLZ = ZMLN * ZML
ZMLN = CMPLX(1., (PI2*FREQ*CAC*RDC))
ZML = ZMLZ / ZMLN
RETURN
END

C
C##############################################################
C
SUBROUTINE YZA(FREQ,ZA)
C
C##############################################################
C
C     Name of Subroutine: YZA
C
C     Formal parameter list: FREQ
C
C     Input parameters:
C
C     Output parameters:
C
C     Common blocks:
C
C     Task of this routine:
C
C     Required subroutines:
C
C     Required functions:
C
C     Routine called in the following subroutines or functions:
C
C##############################################################
C
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL*8 FREQ
REAL*8 RP1A, RP2A, CP1A, CP2A, RSA, CSA
COMPLEX ZA
*
COMMON /ZAC/ RP1A,RP2A,CP1A,CP2A,RSA,CSA
*
CALL IMPED6(RP1A,RP2A,CP1A,CP2A,RSA,CSA,FREQ,ZA)
RETURN
END
SUBROUTINE YZB(FREQ,ZB)

Name of Subroutine: YZB

Formal parameter list: FREQ

Input parameters:

Output parameters:

Common blocks:

Task of this routine:

Required subroutines:

Required functions:

Routine called in the following subroutines or functions:

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL*8 FREQ
REAL*8 RP1B,RP2B,CP1B,CP2B,RSB,CSB
COMPLEX ZB

COMMON /ZBC/RP1B,RP2B,CP1B,CP2B,RSB,CSB

CALL IMPED6(RP1B,RP2B,CP1B,CP2B,RSB,CSB,FREQ,ZB)
RETURN
END

SUBROUTINE TTXW(FREQ,TTX)

Name of Subroutine: TTXW

This subroutine calculates the Transfer function of the TTX-filter at pin 34 and pin 35.

Formal parameter list: FREQ,TTX
**Input parameters:**

- **FREQ** (DOUBLE)

**Output parameters:**

- **TTX** (COMPLEX)

**Task of this routine:**

```plaintext
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)

REAL*8 FREQ, RGTTX, OMP, PI2
COMPLEX TTX

COMMON /TTXC/ RGTTX
COMMON /PI2C/ PI2

OMP = FREQ * PI2
TTX = CMPLX(1., 0.)
RETURN
END
```

**SUBROUTINE IMPED6(RP1, RP2, CP1, CP2, RS, CS, FREQ, Zeq)**

**Modification Klaus Kliese 27.08.89**

**Note:** when a parameter is set to 0 then the corresponding resistor or capacitance does not exist

**Formal parameter list:** RP1, RP2, CP1, CP2, RS, CS, FREQ, Zeq

**Input parameters:**

- **RS** [REAL] ; series resistance
- **CS** [REAL] ; series capacitance
- **RP1** [REAL] ; parallel resistance
- **RP2** [REAL] ; parallel resistance
- **CP1** [REAL] ; parallel capacitance
- **CP2** [REAL] ; parallel capacitance
- **FREQ** [REAL] ; frequency
C### Output parameters:
C### Zeq [ COMPLEX ]
C### Common blocks: QPI2
C### Task of this routine: Equivalent impedance of:

C### SPECIAL CASES:
A. SYSTEM Parallel
  1. CP1 not 0
     1.1 rp1 not 0
     1.2 rp1 not 0
  2. CP1 = 0
     2.1 rp1 not 0
     2.2 rp1 = 0
  3. idem if CP2 = 0
  4. RP2 = 0 and rp1 = 0
  5. CP2 = 0 and CP1 = 0
REAL*8 CP1, CP2, RP1, RP2
REAL*8 CS, RS, N, UL
REAL*8 FREQ, PI2, OMEGA
COMPLEX D, C, Zeq, ZA, ZB

* COMMON /PI2C/ PI2
*
OMEGA = PI2*FREQ
IF (CP1.EQ.0) THEN
  C = CMPLX(RP1, 0.)
ELSE
  C = RP1 + 1 / CMPLX(0., OMEGA*CP1)
ENDIF
IF (CP2.EQ.0) THEN
  D = CMPLX(RP2, 0.)
ELSE
  D = RP2 + 1 / CMPLX(0., OMEGA*CP2)
ENDIF
N = CABS(C)
UL = CABS(D)
* if one of them is 0 then no parallel calculation
IF ((N.EQ.0).OR.(UL.EQ.0)) then
  ZA = C + D
ELSE
  ZA = C & D in parallel
  ZA = C*D/(C+D)
ENDIF
C System series
IF (CS .EQ. 0) THEN
  ZB = CMPLX(RS, 0.)
ELSE
  ZB = RS + (1. / CMPLX(0., OMEGA*CS))
ENDIF
C both
  Zeq = ZA + ZB
RETURN
END
**Appendix C: Spec File 'ST L3030.SPE'**

This specification file contains the specifications of the 'Deutsche Bundespost'.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value 1</th>
<th>Value 2</th>
<th>Value 3</th>
<th>Value 4</th>
<th>Value 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREF =</td>
<td>1014.0</td>
<td>LAW = A</td>
<td>VREF= 0.9480</td>
<td>RLX = 0.</td>
<td>RLR = -7.0</td>
</tr>
<tr>
<td>ABIMP =</td>
<td>ZI</td>
<td>ZLRP1= 820.</td>
<td>ZLCP1= 0.</td>
<td>ZLRP2= 0.</td>
<td>ZLCP2= 0.115E-06</td>
</tr>
<tr>
<td>ZLRS =</td>
<td>220.</td>
<td>ZIRP1= 820.</td>
<td>ZIRC1= 0.</td>
<td>ZIRP2= 0.</td>
<td>ZIRC2= 0.115E-06</td>
</tr>
<tr>
<td>ZIRS =</td>
<td>220.</td>
<td>Z3RP1= 820.</td>
<td>Z3CP1= 0.</td>
<td>Z3RP2= 0.</td>
<td>Z3CP2= 0.115E-06</td>
</tr>
<tr>
<td>ZRRS =</td>
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<td>ZRRP1= 820.</td>
<td>ZRCP1= 0.</td>
<td>ZRRP2= 0.</td>
<td>ZRCP2= 0.115E-06</td>
</tr>
<tr>
<td>Z3RS =</td>
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<td>Z3RS = 220.</td>
<td>Z3CS = 0.</td>
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<td></td>
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<tr>
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<td>ZRRS = 220.</td>
<td>ZRCS = 0.</td>
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<tr>
<td>ZRE</td>
<td>FR= 300</td>
<td>AT- = 0</td>
<td>AT+ = 16</td>
<td>AT- = 20</td>
<td>AT+ = 20</td>
</tr>
<tr>
<td>ZMIR</td>
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<td>AT+ = 30</td>
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<td></td>
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<tr>
<td>DA,UPPER</td>
<td>FR= 300</td>
<td>AT- = 100</td>
<td>AT+ = .75</td>
<td>AT- = .75</td>
<td>AT+ = .75</td>
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<tr>
<td>DA,LOWER</td>
<td>FR= 300</td>
<td>AT- = 0</td>
<td>AT+ = -.25</td>
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<td></td>
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<tr>
<td>DA,DELAY</td>
<td>FR= 500</td>
<td>GD- = 10k</td>
<td>GD+ = .420</td>
<td>.150</td>
<td>.085</td>
</tr>
<tr>
<td>AD,UPPER</td>
<td>FR= 300</td>
<td>AT- = 100</td>
<td>AT+ = .75</td>
<td>AT- = .75</td>
<td>AT+ = .75</td>
</tr>
<tr>
<td>AD,LOWER</td>
<td>FR= 300</td>
<td>AT- = 0</td>
<td>AT+ = -.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>500</td>
<td>600</td>
<td>1k</td>
<td>2.6k</td>
<td>2.8k</td>
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<td>--------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>FR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GD-</td>
<td>10k</td>
<td>.420</td>
<td>.150</td>
<td>.085</td>
<td>.150</td>
</tr>
<tr>
<td>GD+</td>
<td>.420</td>
<td>.150</td>
<td>.085</td>
<td></td>
<td>.150</td>
</tr>
<tr>
<td>DD</td>
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<td></td>
<td></td>
<td></td>
<td>10k</td>
</tr>
<tr>
<td>FR</td>
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<td>500</td>
<td>2.5k</td>
<td>3.4k</td>
<td></td>
</tr>
<tr>
<td>AT-</td>
<td>0</td>
<td>27</td>
<td>27</td>
<td>23</td>
<td></td>
</tr>
<tr>
<td>AT+</td>
<td>23</td>
<td>27</td>
<td>27</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
Appendix D: Result File 'ST L3030.RES'

Input file name: ST L3030.CTL  Date: 08.06.90 14:18
SPEC = L3030.SPE  SLIC = ST L3030.SLI
BYTE = REF.BYT  CHNR = 0,A
PLQ = N
ON = ALL  VERSION = 4.4  SHORT = N
OPT = Z+X+R+B  ZXRB = NNNN
ZAUTO = Y  ZREP = N  ZSIGN = 1
FZ = 300.00  FR = 300.00
RF = 300.00  RDISP = Y
FX = 300.00  XDISP = Y
RDISP = Y  RREFQ = N  RREF = 3.1501
XDISP = Y  XREFQ = N  XREF = -.50486
BAUTO = Y  BREP = N  BSIGN = 1
FB = 300.00  BLIM = 2.00  BDF = 1
APRE = .00  DPRE = .00  APOF = .00  DPOF = .00
AGX = 00  AGR = 00  TM3 = 000
XZQ = -.39062500E+00  XRQ = .81250000E+00
XXQ = .10317380E+01  XBQ = -.13671880E+00
XGQ = .52001950E+00

Bytes for Z-Filter (13):  B0,1C,25,4C,F1,3E,95,BA
Bytes for R-Filter (2B):   70,1A,4F,F1,C9,AA,0C,1B
Bytes for X-Filter (23):   70,E8,AF,FB,1A,45,02,65
Bytes for Gain-factors (30):  51,32,10,32
2nd part of bytes B-Filter (0B):  00,15,BB,CA,14,ED,B3,BB
1st part of bytes B-Filter (03):  5B,B1,B7,AB,32,2A,B2,14
Bytes for B-filter delay (18):  19,19,11,19

* ST SLIC L3030
* VOR = .50000  RIR = .10000E+06  CKR = .00000
* VOX = 1.0000  RIX = 10000.  CKX = .10000E-05
* RP1ZA = .00000  RP1A = .00000  RP1B = .00000
* RP2ZA = .00000  RP2A = .00000  RP2B = .00000
* CP1ZA = .00000  CP1A = .00000  CP1B = .00000
* CP2ZA = .00000  CP2A = .00000  CP2B = .00000
* RSZAC = 500.00  RSA = .50000E+08  RSB = 10000.
* CSZAC = .00000  CSA = .00000  CSB = .00000
* RPC = 100.00  RDC = 300.00  CAC = .22000E-04
* CCOMP = .68000E-07
Run # 2

Z-Filter calculation results
Reference impedance for optimization:
ZIRP1 = 820.  ZICP1 = .000  ZIRP2 = 0.  ZICP2 = .115E-06
ZIRS = 220.  ZICS = .000

Calculated and quantized coefficients:
XZ = -.39571  -.01763  .09355  .03834  -.11305
XZQ = -.39063  -.01764  .09351  .03857  -.11328
Bytes for Z-Filter (13):  B0,1C,25,4C,F1,3E,95,BA

RETURN LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>20.369</td>
<td>2000.</td>
<td>32.299</td>
</tr>
<tr>
<td>200.</td>
<td>25.997</td>
<td>2100.</td>
<td>33.062</td>
</tr>
<tr>
<td>300.</td>
<td>28.913</td>
<td>2200.</td>
<td>33.919</td>
</tr>
<tr>
<td>400.</td>
<td>30.415</td>
<td>2300.</td>
<td>34.819</td>
</tr>
<tr>
<td>500.</td>
<td>31.014</td>
<td>2400.</td>
<td>35.642</td>
</tr>
<tr>
<td>600.</td>
<td>31.082</td>
<td>2500.</td>
<td>36.164</td>
</tr>
<tr>
<td>700.</td>
<td>30.892</td>
<td>2600.</td>
<td>36.116</td>
</tr>
<tr>
<td>800.</td>
<td>30.612</td>
<td>2700.</td>
<td>35.400</td>
</tr>
<tr>
<td>900.</td>
<td>30.333</td>
<td>2800.</td>
<td>34.186</td>
</tr>
<tr>
<td>1000.</td>
<td>30.099</td>
<td>2900.</td>
<td>32.743</td>
</tr>
<tr>
<td>1100.</td>
<td>29.932</td>
<td>3000.</td>
<td>31.265</td>
</tr>
<tr>
<td>1200.</td>
<td>29.841</td>
<td>3100.</td>
<td>29.845</td>
</tr>
<tr>
<td>1300.</td>
<td>29.832</td>
<td>3200.</td>
<td>28.519</td>
</tr>
<tr>
<td>1400.</td>
<td>29.906</td>
<td>3300.</td>
<td>27.295</td>
</tr>
<tr>
<td>1500.</td>
<td>30.067</td>
<td>3400.</td>
<td>26.168</td>
</tr>
<tr>
<td>1600.</td>
<td>30.316</td>
<td>3500.</td>
<td>25.131</td>
</tr>
<tr>
<td>1700.</td>
<td>30.659</td>
<td>3600.</td>
<td>24.175</td>
</tr>
<tr>
<td>1800.</td>
<td>31.100</td>
<td>3700.</td>
<td>23.292</td>
</tr>
<tr>
<td>1900.</td>
<td>31.645</td>
<td>3800.</td>
<td>22.476</td>
</tr>
</tbody>
</table>

Min. Z-loop reserve: 6.834 dB at frequency: 7500.0 Hz
Min. Z-loop mirror reserve: 10.725 dB at frequency: 7000.0 Hz
Run # 2

X-FILTER calculation results
Reference impedance for optimization:
ZIRP1 = 820.  ZICP1 = .000  ZIRP2 = 0.  ZICP2 = .115E-06
ZIRS = 220.  ZICS = .000

Calculated and quantized coefficients:
XX = 1.03178  .03370  -.00468  -.00613  .00014
XXQ = 1.03174  .03369  -.00488  -.00610  .00012
Bytes for X-Filter (23): 70,E8,AF,FB,1A,45,02,65

X-filter attenuation function (in dB), (always absolute values)

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>-.462</td>
<td>.001</td>
<td>2000.</td>
<td>-.320</td>
<td>.001</td>
</tr>
<tr>
<td>200.</td>
<td>-.465</td>
<td>.001</td>
<td>2100.</td>
<td>-.285</td>
<td>.001</td>
</tr>
<tr>
<td>300.</td>
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<td>.001</td>
<td>2200.</td>
<td>-.250</td>
<td>.000</td>
</tr>
<tr>
<td>400.</td>
<td>-.476</td>
<td>.002</td>
<td>2300.</td>
<td>-.215</td>
<td>.001</td>
</tr>
<tr>
<td>500.</td>
<td>-.482</td>
<td>.002</td>
<td>2400.</td>
<td>-.181</td>
<td>.002</td>
</tr>
<tr>
<td>600.</td>
<td>-.489</td>
<td>.003</td>
<td>2500.</td>
<td>-.149</td>
<td>.003</td>
</tr>
<tr>
<td>700.</td>
<td>-.495</td>
<td>.003</td>
<td>2600.</td>
<td>-.119</td>
<td>.003</td>
</tr>
<tr>
<td>800.</td>
<td>-.501</td>
<td>.003</td>
<td>2700.</td>
<td>-.093</td>
<td>.004</td>
</tr>
<tr>
<td>900.</td>
<td>-.504</td>
<td>.004</td>
<td>2800.</td>
<td>-.069</td>
<td>.004</td>
</tr>
<tr>
<td>1000.</td>
<td>-.505</td>
<td>.004</td>
<td>2900.</td>
<td>-.049</td>
<td>.004</td>
</tr>
<tr>
<td>1100.</td>
<td>-.503</td>
<td>.005</td>
<td>3000.</td>
<td>-.033</td>
<td>.005</td>
</tr>
<tr>
<td>1200.</td>
<td>-.498</td>
<td>.005</td>
<td>3100.</td>
<td>-.020</td>
<td>.005</td>
</tr>
<tr>
<td>1300.</td>
<td>-.488</td>
<td>.005</td>
<td>3200.</td>
<td>-.010</td>
<td>.005</td>
</tr>
<tr>
<td>1400.</td>
<td>-.475</td>
<td>.005</td>
<td>3300.</td>
<td>-.003</td>
<td>.004</td>
</tr>
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<td>-.458</td>
<td>.004</td>
<td>3400.</td>
<td>.001</td>
<td>.004</td>
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<tr>
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<td>.004</td>
<td>3500.</td>
<td>.004</td>
<td>.004</td>
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<tr>
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<td>.005</td>
<td>.004</td>
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<td>.006</td>
<td>.003</td>
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<tr>
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<td>-.353</td>
<td>.002</td>
<td>3800.</td>
<td>.006</td>
<td>.003</td>
</tr>
</tbody>
</table>

GX results:
All attenuation values (in dB) refer to \( FREF = 1014.0 \) Hz

\[
\begin{align*}
\text{RLX} & \quad \text{SLIC}^+Z \quad \text{AGX} \quad \text{VREF/VSIC} \quad \text{XREF} \quad \text{TM3} \quad \text{GX} \\
.00 & \quad .24 \quad .00 \quad 4.41 \quad - .50 \quad .00 = -4.33 \quad \text{ideal} \\
.03 = & \quad .24 + .00 + 4.41 + -.50 + .00 + -4.30 \quad \text{quant}
\end{align*}
\]

Second byte for Gain: ,10,32

Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to \( FREF = 1014.0 \) Hz

\[
\begin{align*}
\text{TGREFCA} & = 0.252 \ \text{ms} \\
\text{TGREFCB} & = 0.265 \ \text{ms}
\end{align*}
\]
R-Filter calculation results

Reference impedance for optimization:
ZIRP1 = 820. ZICP1 = .000
ZIRP2 = 0. ZICP2 = .115E-06
ZIRS = 220. ZICS = .000

Calculated and quantized coefficients:
XR = .82771 -.19100 -.00410 -.00853 .00477
XRQ = .81250 -.19141 -.00415 -.00854 .00488

Bytes for R-Filter (2B): 70,1A,4F,F1,C9,AA,0C,1B

R-filter attenuation function (in dB), (always absolute values)

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
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<td>-.042</td>
<td>2000.</td>
<td>1.497</td>
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<tr>
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<tr>
<td>300.</td>
<td>4.139</td>
<td>-.040</td>
<td>2200.</td>
<td>1.154</td>
<td>.011</td>
</tr>
<tr>
<td>400.</td>
<td>4.057</td>
<td>-.038</td>
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<td>1.051</td>
<td>.011</td>
</tr>
<tr>
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<td>2500.</td>
<td>.854</td>
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<tr>
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<td>.758</td>
<td>.012</td>
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<tr>
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</tr>
<tr>
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<td>.019</td>
</tr>
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<td>.021</td>
</tr>
<tr>
<td>1400.</td>
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<td>3300.</td>
<td>.130</td>
<td>.022</td>
</tr>
<tr>
<td>1500.</td>
<td>2.251</td>
<td>.001</td>
<td>3400.</td>
<td>.060</td>
<td>.024</td>
</tr>
<tr>
<td>1600.</td>
<td>2.081</td>
<td>.003</td>
<td>3500.</td>
<td>-.000</td>
<td>.025</td>
</tr>
<tr>
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<td>.005</td>
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<td>-.049</td>
<td>.027</td>
</tr>
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<td>-.085</td>
<td>.027</td>
</tr>
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<td>.008</td>
<td>3800.</td>
<td>.000</td>
<td>.027</td>
</tr>
</tbody>
</table>

GR results:
All attenuation values (in dB) refer to FREF = 1014. Hz

-RLR SLIC+Z AGR VSIC/VREF RREF GR
7.00 = 2.58 + .00 + -4.41 + 3.15 = 5.68 quant
First byte for Gain (30): 51,32  
Calculation of receive transfer function (DA)  
All attenuation values (in dB) refer to FREF = 1014.0 Hz

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
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Run # 1  
B-Filter calculation results  
Reference impedance for optimization:  
ZLRP1 = 820. ZLCP1 = .000 ZLRP2 = 0. ZLCP2 = .115E-06  
ZLRS = 220. ZLCS = .000  
Calculated and quantized coefficients:  
\[
XB = -0.13494 -0.33311 -0.31893 0.00704 0.04508
-0.11252 -0.01736 0.09255 -0.09495 0.04363
\]
\[
XBQ = -0.13672 -0.32813 -0.32031 0.00696 0.04492
-0.11133 -0.01733 0.09277 -0.09570 0.04492
\]
2nd part of bytes B-Filter (0B): 00,15,BB,CA,14,ED,B3,BB  
1st part of bytes B-Filter (03): 5B,B1,B7,AB,32,2A,B2,14
## TRANS HYBRID LOSS

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<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
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<td>35.495</td>
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Additional B-filter delay (in seconds): .625E-04
Bytes for B-filter delay (18): 19,19,11,19
Appendix E:

Figure 14
ST-SLIC Circuitry With and Without the Multiplier
Figure 15
SICOFI® and ST-SLIC Connection Without Multiplier Used
Figure 16
Diagram of the Measurement System
Appendix G:

Figure 17

Figure 18
Figure 19

Figure 20
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1 Introduction

This application note describes the combination of a codec filter device (SICOFI) with an electronic SLIC (ST L3090/L3000) as it can be used on a line card for the connection of analog subscribers.

This note consists of:
- A general description of the ST-SLIC L3090/L3000
- A proposal for the interconnection of SICOFI and SLIC
- A description of the model for the SLIC’s function
- A listing of FORTRAN program to calculate SLIC transfer function
- Result of calculation and measurements generated for the requirements of the 'Deutsche Bundespost'.

2 Hardware SICOFI® and ST-SLIC L3090/L3000

2.1 ST-SLIC L3090/L3000

The SGS-THOMSON-SLIC (ST L3090/L3000) connects the SICOFI with the a,b lines to the subscriber. It has the following functions:
- Battery feeding
- Hybrid
- Ringing
- Ground key detection
- OFF/ON-hook

The SLIC is divided into two parts, a low voltage part (L3090) and a high voltage part (L3000).

The High Voltage Part
The high voltage part is connected with the line. It realizes the battery feeding through the SLIC and switches the ringing signal and the speech signal in both directions.

An internal temperature detection part switches the line current off, when the temperature gets to high.

The high voltage part is connected to the low voltage part using 6 wires.

The Low Voltage Part
The low voltage part synthesizes the DC characteristic, the AC output impedance performs the echo cancellation. Some of these functions may be realized by the SICOFI and therefore it is possible to reduce the number of external components.
The L3090 has a digital parallel interface with 5 pins. There are two output pins (NGDK and ONHK). These two pins detect ground-key and off-hook. The other three pins are chip select (NCS) and two input pins (PWON and RNG). The input pins can be configured to operate in four modes:

- **Power-Down**
  The SLIC presents a high impedance to the line and does not supply current.

- **Standby**
  The SLIC is able to supply current to the line (limited to 12 mA) and to recognize the off-hook condition.

- **Conversation**
  The SLIC supplies the line and is able to detect both the off-hook and ground key conditions. The DC characteristic shown to the line is divided into two regions:
  - current limiting region; the limiting level can be chosen between 4 and 62 mA applying a logical level at pin 24 of L3090 (Note that this pin is not latched by NCS-signal)
  - standard feeding region; the characteristic region is equivalent to a voltage generator with a series resistance, the value of which is defined by an external component.

- **Ringing**
  The SLIC injects a balanced ringing signal to the line with an amplitude of 60 Vrms with a superimposed DC voltage of 22 V. The ringing signal is produced by the battery and a small AC-voltage (1.5 Vrms) at pin 14 of L3090 (connected via a capacitor 1 µF to SICOFI VOUT). The ringing signal starts and stops when the signal crosses zero.
Figure 1
SICOFI® and ST SLIC L3090/L3000

Semiconductor Group 597
2.2 Programming the PBC, SICOFI® and ST-SLIC L3090/L3000
The ST-SLIC L3090/L3000 can be controlled through the SICOFI (see figure 1), setting properly its parallel interface.

For example:
SIG0 = A0 Conversation with $I_{\text{lim}} = 42$ mA
SIG0 = 40 Power down

The line status (off-hook/ground-key) can be read through the SICOFI (see figure 1).

For example:
SIG0: 40 off-hook
SIG0: 80 ground-key

2.3 Model of the ST-SLIC L3090/L3000
The ST-SLIC has some external components:

$Z_A$ SLIC impedance balancing network
$Z_B$ line impedance balancing network
$Z_{\text{LAC}}$ DC feeding system and AC
$R_D$ impedance adjustment
$R_{\text{PC}}$

The value of $R_D$ depends on the DC characteristic region.

![Figure 2](image)

$R_D$ is only used in part 1 infinite in part 2

The value of the impedance $R_D$ has to be written into the input file.
Software for ST-SLIC L3090/L3000

3.1 General SLIC-Parameters

To calculate the coefficients we need the mixed matrix parameters:

Objectives:
- Calculation of the mixed matrix parameters using a simplified three port model.

Method:
- A SLIC is a circuit with a number of elements accessible through three ports:

\[
\begin{align*}
I_1 &= M_{11}V_1 + M_{12}V_3 + M_{13}I_2 \\
V_2 &= M_{21}V_1 + M_{22}V_3 + M_{23}I_2 \\
I_3 &= M_{31}V_1 + M_{32}V_3 + M_{33}I_2
\end{align*}
\]

Note: Description of a port:

Simplification of the Three Port Model

When the SLIC is connected to the SICOFI, we can assume that:
- \( I_2 = 0 \) because the input impedance of SICOFI can be included in the three part model
- \( I_3 \) is not relevant in the following calculations because the equation (3) is not used in the SICOFI program.

\[
\begin{align*}
I_1 &= M_{11}V_1 + M_{12}V_3 \\
V_2 &= M_{21}V_1 + M_{22}V_3
\end{align*}
\]
The parameters $M_{11}$, $M_{12}$, $M_{21}$ and $M_{22}$ are determined as follows:

- $M_{11} = \frac{I_1}{V_1}$ for $V_3 = 0$ (6)
- $M_{12} = \frac{I_3}{V_1}$ for $V_1 = 0$ (7)
- $M_{21} = \frac{V_2}{V_1}$ for $V_3 = 0$ (8)
- $M_{22} = \frac{V_2}{V_3}$ for $V_1 = 0$ (9)

*Figure 4*
3.2 ST-SLIC Parameter

The mixed matrix parameters are:

\[
\text{Re } [M11] (10 – 400 \text{ Hz}) = \frac{(A + 4 \pi \times \pi \times f \times f \times C \times B \times B)}{(A \times A + 4 \pi \times \pi \times f \times f \times C \times C \times B \times B)}
\]

\[
\text{Im } [M11] (10 – 400 \text{ Hz}) = \frac{(2 \pi \times f \times B \times (A - C))}{(A \times A + 4 \pi \times \pi \times f \times f \times C \times C \times B \times B)}
\]

\[
\text{Re } [M11] (400 – 4 \text{ kHz}) = \frac{(E + 4 \pi \times \pi \times f \times f \times D \times D \times R_{PP}}{(E \times E + \pi \times \pi \times f \times f \times R_{PP} \times R_{PP} \times D \times D)}
\]

\[
\text{Im } [M11] (400 – 4 \text{ kHz}) = \frac{(2 \pi \times f \times B \times (A - C))}{(A \times A + 4 \pi \times \pi \times f \times f \times C \times C \times B \times B)}
\]

\[
\text{Re } [M12] (10 – 4 \text{ kHz}) = \frac{2 \pi \times f \times f \times B \times B \times C \times B \times B}{(A \times A + 4 \pi \times \pi \times f \times f \times C \times C \times B \times B)}
\]

\[
\text{Im } [M12] (10 – 4 \text{ kHz}) = \frac{2 \pi \times f \times f \times B \times B \times (A - C)}{(A \times A + 4 \pi \times \pi \times f \times f \times C \times C \times B \times B)}
\]

\[
\text{Re } [M21] (10 – 3 \text{ kHz}) = \frac{(L \times E)}{(E \times E + 4 \pi \times \pi \times f \times f \times H \times H)}
\]

\[
\text{Im } [M21] (10 – 3 \text{ kHz}) = \frac{(2 \pi \times f \times f \times A \times L \times A)}{(A \times A + 4 \pi \times \pi \times f \times f \times C \times C \times B \times B)}
\]

\[
\text{Re } [M21] (3 – 4 \text{ kHz}) = \frac{(L \times E)}{(E \times E + 4 \pi \times \pi \times f \times f \times H \times H)}
\]

\[
\text{Im } [M22] (10 – 3 \text{ kHz}) = \frac{2 \pi \times f \times f \times B \times B \times C \times M}{(A \times A + 4 \pi \times \pi \times f \times f \times B \times B \times C \times C)}
\]

\[
\text{Im } [M22] (10 – 4 \text{ kHz}) = \frac{(2 \pi \times f \times f \times B \times A \times (M - C))}{(A \times A + 4 \pi \times \pi \times f \times f \times B \times B \times C \times C)}
\]

where:

\[
A = R_D + R_{PP}
\]

\[
B = R_D \times C_D
\]

\[
C = \frac{R_{AC}}{25} + R_{PP}
\]

\[
D = (R_{AC} + R_{PC}) \times C_C
\]

\[
E = \frac{R_{AC}}{25} + R_{PP}
\]

\[
G = C_C \times R_{PC}
\]

\[
H = C_C \times R_{PP} \times (R_{AC} + R_{PC})
\]

\[
L = \frac{R_{AC} + R_{PC}}{25}
\]

\[
M = \frac{R_{PP} - R_{PC}}{25}
\]

\[
N = \frac{R_A}{(R_A + R_B)}
\]
3.3 Calculation

The SLIC has a 0 dB gain in the receive direction and therefore the SICOFI must attenuate the incoming signal in order to match the German specs (GR = –7 dB). Because of the attenuation being too high (>12 dB) for the SICOFI, either a voltage divider in receive direction is needed or the AGR of the SICOFI has to be programmed to 6 dB analog attenuation. The SLIC-program is written in FORTRAN and the user may modify this for his own SLIC. The program needs an input file with the values of the external circuit, and then it calculates the mixed matrix parameters and writes them into a SLIC-file. Together with the SICOFI-program you are able to calculate the SICOFI coefficients. It should be noted that the two impedances \( Z_A \) and \( Z_B \), used by the SLIC in order to perform the echo cancellation, can be avoided because the SICOFI is able to perform such a function (in this case \( Z_B \) is open and \( Z_A \) is shorted to ground. In special cases (very high signal levels) it could be necessary to introduce two resistors as \( Z_A \) and \( Z_B \) to avoid that the TX-SLIC-amplifier saturates (max. TX peak voltage = 3 V).

If you have no \( Z_A \) and \( Z_B \) than you are not allowed to switch a capacitor between SLIC and SICOFI in the receive direction because the SLIC input need a connection to ground.

Figure 5
L3090/L3000 Model
Note: For an easier representation some components names were changed in respect to the names on the data sheet; in particular:

- $R_{PP}$ correspond to $2 \times R_P$
- $R_D$ correspond to $R_{DC}$
- $R_{AC}$ correspond to $Z_{IAC}$
- $R_{PC}$ correspond to $R_{PC}$
- $R_A$ correspond to $Z_L$
- $R_B$ correspond to $Z_B$
- $C_D$ correspond to $C_{IAC}$
- $C_C$ correspond to $C_{COMP}$

4 Comparison between Calculation and Measurement
The values of the measurement conformed with the calculation. The difference between both are very small (see results of calculation and measurement in the appendix). Only the high attenuation of calculated echo return loss (> 35 dB) cannot be reached by measurement.

5 Appendix
On the next pages you will find the following details:
- SGS-THOMSON-SLIC L3090/L3000 FORTRAN program listing
- Calculated SICOFI-ST-SLIC transfer functions for the ST-SLIC model. The values of the external ST-SLIC components are listed on bottom at page...

Note: $R = 300 \, \Omega$
Input impedance of SLIC: $34750 \, \Omega$ parallel with ring input. In this case: $V_{OR} = 0.47$

- Measured SICOFI-ST-SLIC transfer functions.
Listing of FORTRAN program 'STL 3090.FOR'

C************************************************************************** TOP **************************************************************************
C**************************************************************************

PROGRAM SGS
C     17.05.88  Udo Stueting / Klaus Kliese / Walter Rossi  L 3090
C**************************************************************************

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
*
INTEGER IN,OUT,I
CHARACTER*14 BUF1,BUF2*7,BUF3*7,BUF4*7,BUF5*7
CHARACTER*7 BUF6,BUF7*7,BUF8*7,BUF9*7,BUFF2*12,BUFF3*12
CHARACTER*7 BUF10*7,BUF11*7,BUF12*7,BUF13*7,BUF14*7,BUF15*7
CHARACTER*7 BUFF1*12,FILEOUT*12,ANSW*1,INFILE*12
REAL*8 M11(2),M12(2),M21(2),M22(2),FREQ,AR(2),AX(2)
REAL*8 VOR,RIR,CKR,VOX,RIX,CKX,PI2,ZSLI
REAL*8 RPP,RD,RAC,RPC,RA,CD,CC
REAL*8 NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
*
COMMON /ARC/ RIR,CKR,VOR
COMMON /AXC/ RIX,CKX,VOX
COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
COMMON /RSGSC/ RPP,RD,RAC,RPC,RA,CD,CC
COMMON /PI2C/ PI2
C**************************************************************************
C      Initialisation part
C**************************************************************************

C
DATA BUF1/* SGS SLIC */
DATA BUF2/*/ VOR ='/,BUF3/* RIR ='/,BUF4/* CKR ='/
DATA BUF5/*/ VOX ='/,BUF6/* RIX ='/,BUF7/* CKX ='/
DATA BUF8/*/ RPP ='/,BUF9/* RD ='/,BUF10/* RAC ='/
DATA BUF11/*/ RPC ='/,BUF12/* RA ='/,BUF13/* RB ='/
DATA BUF14/*/ CD ='/,BUF15/* CC ='/
DATA BUF16/* ZSLI ='/
*
OUT = 6
IN  = 5
PI2  = 4.*DASIN(1.D0)
FILEOUT = ' ',
        WRITE(OUT,'(A)')
& ' Enter input file name(xxxxxxxx.INP): '
10      READ (IN,'(A)') INFILE
         IF (INDEX(INFILE,' ').EQ.1

Semiconductor Group 604
& .OR.(INDEX(INFILE,'.INP').EQ.0
& .AND.INDEX(INFILE,'.inp').EQ.0) THEN
   WRITE (OUT,'(A)') ' Enter correct input file name:  ' 
   INFILE=' '''
   GOTO 10
ENDIF
WRITE (OUT,'(A)') ' Enter output file name (xxxxxxxxx.SLI):  '
20 READ (IN,'(A)') FILEOUT
IF (INDEX(FILEOUT,' ').EQ.1) THEN
   WRITE (OUT,'(A)')
   &    ' Enter correct output file name (with extension .SLI):  ' 
   FILEOUT=' '''
   GOTO 20
ENDIF
OPEN (30, FILE=FILEOUT, ERR=1000, STATUS= 'UNKNOWN')
OPEN (10, FILE=INFILE, ERR=1100, STATUS= 'OLD')
READ(10,'(A)')
WRITE(6,*') 'Reading input file'
READ(10,*') VOR
READ(10,'(A)')
READ(10,*') RIR
READ(10,'(A)')
READ(10,*') CKR
READ(10,'(A)')
READ(10,*') VOX
READ(10,'(A)')
READ(10,*') RIX
READ(10,'(A)')
READ(10,*') CKX
READ(10,'(A)')
READ(10,*') RPP
READ(10,'(A)')
READ(10,*') RD
READ(10,'(A)')
READ(10,*') RAC
READ(10,'(A)')
READ(10,*') RPC
READ(10,'(A)')
READ(10,*') RA
READ(10,'(A)')
READ(10,*') RB
READ(10,'(A)')
READ(10,*') CD
READ(10,'(A)')
READ(10,*') CC
READ(10,'(A)')
READ(10,*') ZSLI
CLOSE (10)
WRITE (30,'(A)') BUF1
WRITE (BUFF1,'(G12.5)') VOR
WRITE (BUFF2,'(G12.5)') RIR
WRITE (BUFF3,'(G12.5)') CKR
WRITE (30,'(A)') BUF2//BUFF1//BUF3//BUFF2//BUF4//BUFF3
WRITE (BUFF1,'(G12.5)') VOX
WRITE (BUFF2,'(G12.5)') RIX
WRITE (BUFF3,'(G12.5)') CKX
WRITE (30,'(A)') BUF5//BUFF1//BUF6//BUF2//BUF7//BUFF3
WRITE (BUFF1,'(G12.5)') RPP
WRITE (BUFF2,'(G12.5)') RD
WRITE (BUFF3,'(G12.5)') RAC
WRITE (30,'(A)') BUF8//BUFF1//BUF9//BUF2//BUF10//BUFF3
WRITE (BUFF1,'(G12.5)') RPC
WRITE (BUFF2,'(G12.5)') RA
WRITE (BUFF3,'(G12.5)') RB
WRITE (30,'(A)') BUF11//BUFF1//BUF12//BUF2//BUF13//BUFF3
WRITE (BUFF1,'(G12.5)') CD
WRITE (BUFF2,'(G12.5)') CC
WRITE (30,'(A)') BUF14//BUFF1//BUF15//BUFF2
WRITE (30,'(A)') 'ZSLI'
WRITE (30,'(A)') 'ZSLI'

NA = RD +RPP
NB = RD * CD
NC = (RAC / 25.) + RPP
ND = (RAC + RPC) * CC
NE = (RAC / 25) + RPP
NG = CC * RPC
NH = CC * RPP * (RAC + RPC)
NL = (RAC + RPC) / 25.
NM = RPP - (RPC/ 25.)
NN = RA / (RA + RB)
C
C*************************************************************
C         Calculation part
C*************************************************************
C L3090
C
WRITE (OUT,*) ' Running M11 calculation...
WRITE (30,'(A)') 'M11-TABLE'
DO 100 I=1,40
   FREQ = DBLE(I*10)
   CALL PM11L(FREQ,M11)
   WRITE (30,*) FREQ,M11(1),M11(2)
100 CONTINUE
DO 101 I=41,399
   FREQ = DBLE(I*10)
   CALL PM11H(FREQ,M11)
   WRITE (30,*) FREQ,M11(1),M11(2)
101 CONTINUE
C
C        M12 =
C
WRITE (OUT,*) ' Running M12 calculation...
WRITE (30,'(A)') 'M12-TABLE'
DO 110 I=1,399
   FREQ = DBLE(I*10)
   CALL ARW(FREQ,AR)
   CALL PM12L(FREQ,M12)
   CALL CMUL(AR,M12,M12)
   WRITE (30,*) FREQ,M12(1),M12(2)
110 CONTINUE
C
C        M21 =
C
WRITE (OUT,*) ' Running M21 calculation...
WRITE (30,'(A)') 'M21-TABLE'
DO 120 I=1,300
   FREQ = DBLE(I*10)
   CALL AXW(FREQ,AX)
   CALL PM21L(FREQ,M21)
   CALL CMUL(AX,M21,M21)
   WRITE (30,*) FREQ,M21(1),M21(2)
120 CONTINUE
DO 121 I=301,399
   FREQ = DBLE(I*10)
   CALL AXW(FREQ,AX)
   CALL PM21H(FREQ,M21)
   CALL CMUL(AX,M21,M21)
   WRITE (30,*) FREQ,M21(1),M21(2)
121 CONTINUE
C
M22 =
C
WRITE (OUT,*) ' Running M22 calculation...'  
WRITE (30,'(A)') 'M22-TABLE'  
DO 130 I=1,399  
   FREQ = DBLE(I*10)  
   CALL AXW(FREQ,AX)  
   CALL ARW(FREQ,AR)  
   CALL PM22L(FREQ,M22)  
   CALL CMUL(AR,M22,M22)  
   CALL CMUL(AX,M22,M22)  
   WRITE (30,* ) FREQ,M22(1),M22(2)  
130   CONTINUE  
   WRITE(30,'(A1)') ';'  
   CLOSE (30)  
   WRITE(OUT,'(A)') ' Data written in file: //FILEOUT'  
1000  WRITE(OUT,'(A)') ' OPEN ERROR AT OUTPUT-FILE: //FILEOUT'  
1100  WRITE(OUT,'(A)') ' OPEN ERROR AT INPUT-FILE: //INFILE'  
END
C
C###################################################################
C
SUBROUTINE ARW(FREQ,AR)
C
C###################################################################
C
Name of Subroutine: ARW
C
Formal parameter list: FREQ,AR
C
Input parameters:
FREQ (DOUBLE)
C
Output parameters:
ARW (DOUBLE) ARRAY 2
C
Task of this routine: VOR*jwRIR*CKR/(1.+jwRIR*CKR)C
C
C###################################################################
C
IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
REAL*8 AR(2),FREQ,RIR,CKR,VOR,OMP,PI2,V1(2),V2(2)
*
COMMON /ARC/ RIR,CKR,VOR
COMMON /PI2C/ PI2
*
IF(CKR.EQ.0) THEN
AR(1) = 1.
AR(2) = 0.
ELSE

OMP = PI2*FREQ*RIX*CKX
V1(1) = 0
V1(2) = OMP
V2(1) = 1.D0
V2(2) = OMP
CALL CDIV(V1,V2,AR)
END IF
AR(1) = VOR * AR(1)
AR(2) = VOR * AR(2)
RETURN
END

C
C****************************************************************************=
C
SUBROUTINE AXW(FREQ,AX)
C****************************************************************************=
C
Name of Subroutine: AXW
Formal parameter list: FREQ,AX
Input parameters:
  FREQ  (DOUBLE)
Output parameters:
  AX    (DOUBLE)  ARRAY 2
Task of this routine:

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
*
REAL*8 AX(2),FREQ,RIX,CKX,VOX,OMP,PI2,V1(2),V2(2)
*
COMMON /AXC/ RIX,CKX,VOX
COMMON /PI2C/ PI2
*
IF(CKX.EQ.0) THEN
  AX(1) = 1.
  AX(2) = 0.
ELSE
  OMP   = PI2*FREQ*RIX*CKX
  V1(1) = 0.
  V1(2) = OMP
  V2(1) = 1.D0
V2(2) = 0MP
CALL CDIV(V1,V2,AX)
END IF
AX(1) = AX(1)*VOX
AX(2) = AX(2)*VOX
RETURN
END

C
C*************************************************************************
C
SUBROUTINE CMUL(C,D,E)
C*************************************************************************
C
C     Name of Subroutine: CMUL
C
C     Formal parameter list: C,D,P
C
C     Input parameters:
C         C       (DOUBLE)   ARRAY [2]
C         D       (DOUBLE)   ARRAY [2]
C
C     Output parameters:
C         E       (DOUBLE)   ARRAY [2]
C
C     Task of this routine:
C         SUBROUTINE COMPLEX MULTIPLICATION
C
C*************************************************************************
C
IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
REAL*8 C(2),D(2),P(2),E(2)
*
P(1)=C(1)*D(1)-C(2)*D(2)
P(2)=C(2)*D(1)+C(1)*D(2)
E(1)=P(1)
E(2)=P(2)
RETURN
END

C
C*************************************************************************
C
SUBROUTINE CDIV(C,D,E)
C*************************************************************************
C
C     Name of Subroutine: CDIV
C
C     Formal parameter list: C,D,P
Input parameters:

C (DOUBLE) ARRAY [2]
D (DOUBLE) ARRAY [2]

Output parameters:

E (DOUBLE) ARRAY [2]

Task of this routine:

SUBROUTINE COMPLEX DIVISION

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
*
REAL*8 C(2), D(2), P(3), E(2)
*
P(2) = D(1)*D(1) + D(2)*D(2)
P(1) = C(1)*D(1) + C(2)*D(2)
P(3) = C(2)*D(1) - C(1)*D(2)
*
E(1) = P(1)/P(2)
E(2) = P(3)/P(2)
RETURN
END

SUBROUTINE PM11L(FREQ,M11)

Name of Subroutine: PM11L

Formal parameter list: FREQ

Input parameters: FREQ

Output parameters: M11

Task of this routine: Re [M11] (10-400Hz)
Im [M11] (10-400Hz)

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL*8 PI2, FREQ, M11(2), NA, NB, NC, ND, NE, NG, NH, NL, NM, NN
*
COMMON /PI2C/ PI2
COMMON /NSGSC/ NA, NB, NC, ND, NE, NG, NH, NL, NM, NN
*
M11(1) = (NA + PI2*PI2*FREQ*FREQ*NC*NB*NB) /
& (NA*NA  +PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
  M11(2) = (PI2*FREQ*NB*(NA-NC)) / 
  & (NA*NA  +PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
RETURN
END

C*****************************************************
C SUBROUTINE PM11H(FREQ,M11)
C*****************************************************
C Name of Subroutine: PM11H
C Formal parameter list: FREQ
C Input parameters: FREQ
C Output parameters: M11
C Task of this routine: Re [M11] (410-3990Hz)
C Im [M11] (410-3990Hz)
C*****************************************************
C IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL*8 PI2,FREQ,M11(2),NA,NB,NC,ND,NE,NG,NH,NL,NN
REAL*8 RPP,RA,RB,CD,CC
*
COMMON /PI2C/ PI2
COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NN
COMMON /RSGSC/ RPP,RA,RB,CD,CC
*
M11(1) =(NE + PI2*PI2*FREQ*FREQ*ND*ND+RPP) / 
& (NE*NE  +PI2*PI2*FREQ*FREQ*RPP*RPP*ND*ND)
M11(2) = (PI2*FREQ*ND*(NE-RPP)) / 
& (NE*NE  +PI2*PI2*FREQ*FREQ*RPP*RPP*ND*ND)
RETURN
END

C*****************************************************
C SUBROUTINE PM12HL(FREQ,M12)
C*****************************************************
C Name of Subroutine: PM12HL
C Formal parameter list: FREQ
C Input parameters: FREQ
Output parameters:  M12

Task of this routine:  Re [M12] (10-3990Hz)
Im [M12] (10-3990Hz)

IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
REAL*8 PI2,FREQ,M12 (2),NA,NB,NC,ND,NE,NG,NH,NL,NN

COMMON /PI2C/ PI2
COMMON /NSGSC/ NA,NB,NC,NE,NG,NH,NL,NN

M12(1) = 2. * (NA + PI2*PI2*FREQ*FREQ*NC*NB*NB) /
&       (NA*NA + PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
M12(2) = 2. * (PI2*FREQ*NB*(NA-NC)) /
&       (NA*NA + PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
RETURN
END

SUBROUTINE PM12H(FREQ,M12)

Name of Subroutine:  PM12H
Formal parameter list:  FREQ
Input parameters:  FREQ
Output parameters:  M12
Task of this routine:  not used

IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
REAL*8 PI2,FREQ,M12 (2),NA,NB,NC,ND,NE,NG,NH,NL,NN
REAL*8 RPP,RD,RAC,RPC,RA,RB,CD,CC

COMMON /PI2C/ PI2
COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NN
COMMON /RSGSC/ RPP,RD,RAC,RPC,RA,RB,CD,CC

M12(1) = 2. * (NE + PI2*PI2*FREQ*FREQ*NH*NG) /
&       (NE*NE + PI2*PI2*FREQ*FREQ*NH*NH)
M12(2) = 2. * (PI2*FREQ*(NH-(NE*NG))) /
&       (NE*NE + PI2*PI2*FREQ*FREQ*NH*NH)
RETURN
END
SUBROUTINE PM21L(FREQ,M21)

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL*8 PI2,FREQ,M21(2),NA,NB,NC,ND,NE,NG,NH,NL,NM,NN

M21(1) = - (PI2*PI2*FREQ*FREQ*NB*NB*NL*NC) / (NA*NA + PI2*PI2*FREQ*FREQ*NC*NC*NB*NB) 
& M21(2) = - (PI2*FREQ*NB*NL*NA) / (NA*NA + PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)

RETURN
END
C SUBROUTINE PM21H(FREQ,M21)

C

C Name of Subroutine:  PM21H

C Formal parameter list:  FREQ

C Input parameters:  FREQ

C Output parameters:  M21

C Task of this routine:  Re [M21] (3010-3990Hz)
C Im [M21] (3010-3990Hz)

C

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL*8 PI2,FREQ,M21(2),NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
REAL*8 RPP,RD,RAC,RPC,RA,RB,CD,CC

*C
COMMON /PI2C/ PI2
COMMON /NSGSC/ NA,NB,NC,ND,NE,NG,NH,NL,NM,NN
COMMON /RSGSC/ RPP,RD,RAC,RPC,RA,RB,CD,CC

* M21(1) = - (NL * NE) / & (NE*NE +PI2*PI2*FREQ*FREQ*NH*NH)
& M21(2) = (PI2*FREQ*NL*NH) / & (NE*NE +PI2*PI2*FREQ*FREQ*NH*NH)
RETURN
END

C SUBROUTINE PM22L(FREQ,M22)

C

C Name of Subroutine:  PM22L

C Formal parameter list:  FREQ

C Input parameters:  FREQ

C Output parameters:  M22

C Task of this routine:  Re [M22] (10-3990Hz)
C Im [M22] (10-3990Hz)
IMPLICIT LOGICAL (A-K, M-Z), CHARACTER (L)
REAL*8 PI2, FREQ, M22(2), NA, NB, NC, ND, NE, NG, NH, NL, NM, NN

* COMMON /PI2C/ PI2
COMMON /NSGSC/ NA, NB, NC, ND, NE, NG, NH, NL, NM, NN
*
M22(1) = (-2.*NN) + 2.*((NA*NA*PI2*PI2*FREQ*FREQ*NB*NB*NC*NM)/
& (NA*NA+PI2*PI2*FREQ*FREQ*NC*NC*NB*NB))
&
M22(2) = 2. * (PI2*FREQ*NB*NA*(NM-NC)) /
& (NA*NA +PI2*PI2*FREQ*FREQ*NC*NC*NB*NB)
RETURN
END

SUBROUTINE PM22H(FREQ, M22)

IMPLICIT LOGICAL (A-K, M-Z), CHARACTER (L)
REAL*8 PI2, FREQ, M22(2), NA, NB, NC, ND, NE, NG, NH, NL, NM, NN
REAL*8 RPP, RD, RAC, RPC, RA, RB, CD, CC

* COMMON /PI2C/ PI2
COMMON /NSGSC/ NA, NB, NC, ND, NE, NG, NH, NL, NM, NN
COMMON /RSGSC/ RPP, RD, RAC, RPC, RA, RB, CD, CC
*
M22(1) = (-2.*NN) + 2.* (NM*NC) /
& (NC*NC +PI2*PI2*FREQ*FREQ*NH*NH)
&
M22(2) = 2. * (PI2*FREQ*NM*NH) /
& (NC*NC +PI2*PI2*FREQ*FREQ*NH*NH)
RETURN
END
SUBROUTINE IMPED1(RSER, RPAR, CSER, CPAR, FREQ, ZI)

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL*8 V1(2), V2(2), ZI(2), CSER, CPAR, FREQ, PI2, RPAR, RSER
COMMON /QP2/ PI2
V1(1) = 1.D0
V1(2) = PI2*FREQ*CPAR*RPAR
V2(1) = RPAR
V2(2) = 0.
CALL CDIV(V2, V1, ZI)
ZI(1) = ZI(1)+RSER
ZI(2) = ZI(2)+0.
RETURN
END

SUBROUTINE IMPED2(RSER, RPAR, CSER, CPAR, FREQ, ZI)

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL*8 V1(2), V2(2), ZI(2), CSER, CPAR, FREQ, PI2, RPAR, RSER
COMMON /QP2/ PI2
V1(1) = 1.D0
V1(2) = PI2*FREQ*CPAR*RPAR
V2(1) = RPAR
V2(2) = 0.
CALL CDIV(V2, V1, ZI)
ZI(1) = ZI(1)+RSER
ZI(2) = ZI(2)+0.
RETURN
END
C     Task of this routine:  CALCULATION OF COMPLEX IMPEDANCE
C
C###################################################################
C
IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)

REAL*8 V1(2),V2(2),ZI(2),CSER,CPAR,FREQ,PI2,RPAR,RSER,C(2)
REAL*8 OMEGA

COMMON /QP2/ PI2

OMEGA = PI2*FREQ
V1(1) = 1.D0
V1(2) = OMEGA*CPAR*RPAR
V2(1) = RPAR
V2(2) = 0.
call cdiv(v2,v1,zi)
V2(1) = 0.
V2(2) = OMEGA*CSER
V1(1) = 1.D0
V1(2) = V2(2)*RSER
CALL CDIV(V1,V2,C)
ZI(1)=ZI(1)+C(1)
ZI(2)=ZI(2)+C(2)
RETURN
END

C###################################################################
C
SUBROUTINE IMPED3(RSER,RPAR,CSER,CPAR,FREQ,ZL)
C
C###################################################################
C
C     Name of Subroutine:     IMPED3
C
C     Formal parameter list:  RSER,RPAR,CSER,CPAR,FREQ,ZI
C
C     Input parameters:      
C     RSER   (DOUBLE)   ; series resistance
C     RPAR   (DOUBLE)   ; parallel resistance
C     CSER   (DOUBLE)   ; series capacitance
C     CPAR   (DOUBLE)   ; parallel capacitance
C     FREQ   (DOUBLE)   ; frequency

C     Output parameters:  
C     ZI     (DOUBLE)   ARRAY [2]

C
Output parameters:

ZI (DOUBLE) ARRAY [2]

Task of this routine: CALCULATION OF COMPLEX IMPEDANCE

------------------------------------------------------------------

REAL*8 ZL(2),CSER,CPAR,FREQ,RPAR,RSER,PI2,OMEGA,A(2),B(2)

COMMON /QP2/ PI2

OMEGA = PI2*FREQ

IF (RPAR.EQ.0) THEN
  A(1) = 1.D0
  A(2) = OMEGA*CSER*RSER
  B(1) = 0
  B(2) = OMEGA*CSER
  CALL CDIV(A,B,ZL)
ELSE
  A(1) = RPAR
  A(2) = OMEGA*CSER*RSER*RPAR
  B(1) = 1.D0
  B(2) = OMEGA*CSER*(RSER+RPAR)
  CALL CDIV(A,B,ZL)
END IF
RETURN
END

Listing of SICOFI® Result File 'STL 3090.RES'

Input_file_name: L3090.CTL          Date: 20.05.88  11:25
SPEC = L3090.SPE                     SLIC = L3090.SLI
BYTE = L3090.BYT          CHNR = 0,A
PLQ = N
ON = ALL                    REL = Y                  SHORT = N
OPT = Z+X+R+B            ZXRB = NNNN
  FZ = 300.00              3400.0      ZLIM =  2.00
  ZREP = Y                ZSIGN =  1
  FR =  400.00             3300.0
  RFIL = Y                 RREFQ = N      RREF =  5.6550
  FX =  400.00             3300.0
  XFIL = Y                 XREFQ = N      XREF =-0.76499E-01
  FB =  300.00             3400.0      BLIM =  2.00 TBM =  1
  BREP = N                BSIGN =  1
APOF = 0.10  DPOF = 0.00E+00  APRE = 0.00E+00  DPRE = 0.00E+00
XZQ = 0.2773437500000000E+00  0.5000000000000000E+00
  0.4492187500000000E-01  -0.4531250000000000E+00
  0.1640625000000000E+00
XQ = 0.6875000000 -0.2832031250  0.0654296875 -0.0205078125
  0.0039062500
XXQ = 1.0468750000 -0.0527343750  0.0302734375 -0.0019531250
  0.0019531250
XQ = 0.4589843750  0.3906250000  0.2597656250  0.1152343750
  0.0722656250  0.0396250000  0.0120070312  0.0003906250
  0.0003906250
XQ = 0.6718750000  1.6562500000

Bytes for Z-Filter (13): 30,22,B9,5A,B1,F1,28,B3
Bytes for R-Filter (2B): 40,C8,2E,42,A4,3A,14,12
Bytes for X-Filter (23): 50,C8,8D,5C,9C,BC,02,A4
Bytes for Gain-factors (30): 21,A1,10,22
2nd part of bytes B-Filter (0B): 00,26,6E,25,72,2A,A6
1st part of bytes B-Filter (03): 4B,23,C3,22,25,A1,5B,C1
Bytes for B-Filter delay (18): 19,19,11,19

* SGS SLIC
* VOR = 0.47000  RIR = 34750.  CKR = 0.00000E+00
* VOX = 1.00000  RIX = 0.10000E+06  CKX = 0.22000E-04
* RPP = 60.000  RD = 750.00  RAC = 13500.
* RPC = 0.00000E+00  RA = 0.00000E+00  RB = 0.10000E+11
* CD = 0.23500E-04  CC = 0.33000E-09
Run # 1

Z-FILTER calculation results
Generator impedance ZI at a,b line!

Calculated and quantized coefficients:

\[ XZ = \begin{pmatrix} 0.27720 & 0.49984 & 0.04498 & -0.45004 & 0.16550 \\ XZQ = \begin{pmatrix} 0.27734 & 0.50000 & 0.04492 & -0.45312 & 0.16406 \\ \end{pmatrix} \]

Bytes for Z-Filter (13): 30,22,B9,5A,B1,F1,28,B3

RETURN LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>26.962</td>
<td>1800.</td>
<td>25.069</td>
</tr>
<tr>
<td>200.</td>
<td>26.741</td>
<td>1900.</td>
<td>25.314</td>
</tr>
<tr>
<td>300.</td>
<td>26.271</td>
<td>2000.</td>
<td>25.599</td>
</tr>
<tr>
<td>400.</td>
<td>25.716</td>
<td>2100.</td>
<td>25.919</td>
</tr>
<tr>
<td>500.</td>
<td>25.724</td>
<td>2200.</td>
<td>26.267</td>
</tr>
<tr>
<td>600.</td>
<td>25.483</td>
<td>2300.</td>
<td>26.631</td>
</tr>
<tr>
<td>700.</td>
<td>25.247</td>
<td>2400.</td>
<td>26.993</td>
</tr>
<tr>
<td>800.</td>
<td>25.031</td>
<td>2500.</td>
<td>27.330</td>
</tr>
<tr>
<td>900.</td>
<td>24.845</td>
<td>2600.</td>
<td>27.607</td>
</tr>
<tr>
<td>1000.</td>
<td>24.696</td>
<td>2700.</td>
<td>27.786</td>
</tr>
<tr>
<td>1100.</td>
<td>24.588</td>
<td>2800.</td>
<td>27.829</td>
</tr>
<tr>
<td>1200.</td>
<td>24.523</td>
<td>2900.</td>
<td>27.705</td>
</tr>
<tr>
<td>1300.</td>
<td>24.501</td>
<td>3000.</td>
<td>27.405</td>
</tr>
<tr>
<td>1400.</td>
<td>24.525</td>
<td>3100.</td>
<td>26.821</td>
</tr>
<tr>
<td>1500.</td>
<td>24.594</td>
<td>3200.</td>
<td>26.159</td>
</tr>
<tr>
<td>1600.</td>
<td>24.708</td>
<td>3300.</td>
<td>25.427</td>
</tr>
<tr>
<td>1700.</td>
<td>24.866</td>
<td>3400.</td>
<td>24.657</td>
</tr>
</tbody>
</table>

Min. Z-loop reserve: 1.443 dB at frequency: 7000.0 Hz
Min. Z-loop mirror signal reserve: 5.092 dB at frequency: 6500.0 Hz

Warning! SICOFI specs (noise, gain tracking ...) not guaranteed
Increase SLIC attenuation in receive path at least by 1.13 dB

X-FILTER calculation results
Calculated and quantized coefficients:

\[ XX = \begin{pmatrix} 1.03976 & -0.05284 & 0.03052 & -0.00288 & 0.00233 \\ XXQ = \begin{pmatrix} 1.04687 & -0.05273 & 0.03027 & -0.00195 & 0.00195 \\ \end{pmatrix} \]

Bytes for X-Filter (23): 50,C8,8D,5C,9C,BC,02,A4
X-filter attenuation function (in dB), (always absolute values)
<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
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</table>

**GX results:**

All attenuation values (in dB) refer to FREF = 1014. Hz

RLX SLIC+Z VREF/VSICOFI -XREF GX
0.00 - 0.03 - 4.42 - -0.08 = -4.37 ideal
-0.02 = 0.03 + 4.42 + -0.08 + -4.38 quant

Second byte for Gain: ,10,22

Calculation of transmit transfer function (AD)

All attenuation values (in dB) refer to FREF = 1014.0 Hz

Generator impedance ZI at a,b line!

TGREF CA = 0.273 ms TGREF CB = 0.287 ms

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<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
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</table>
Run # 1

R-FILTER calculation results
Calculated and quantized coefficients:

\[
\begin{align*}
XR &= 0.68422 -0.28458 0.06639 -0.01965 0.00512 \\
XRQ &= 0.68750 -0.28320 0.06543 -0.02051 0.00391 \\
\end{align*}
\]

Bytes for R-Filter (2B): 40,C8,2E,42,A4,3A,14,12

R-filter attenuation function (in dB), (always absolute values)

<table>
<thead>
<tr>
<th>FREQ</th>
<th>loss</th>
<th>GD</th>
<th>FREQ</th>
<th>loss</th>
<th>GD</th>
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<tbody>
<tr>
<td>Hz</td>
<td>(dB)</td>
<td>(msec)</td>
<td>Hz</td>
<td>(dB)</td>
<td>(msec)</td>
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<td>-0.004</td>
<td>3600.</td>
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GR results:
All attenuation values (in dB) refer to FREF = 1014. Hz

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<th>VSICOFI/VREF</th>
<th>RREF</th>
<th>GR</th>
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<td>5.65</td>
<td>3.45 quant</td>
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First byte for Gain (30): 21,A1
Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF = 1014.0 Hz
Terminating impedance ZI at a,b line!

TGREF CA = 0.223 ms TGREF CB = 0.205 ms
B-FILTER calculation results
Terminating impedance ZL at a,b line!

Calculated and quantized coefficients:

XB = 0.04525  0.39813  0.25930  0.11590  0.07329  0.01268  0.00503  0.04196  -0.03075  0.01917
XBQ = 0.04590  0.39062  0.25977  0.11523  0.07227  0.01221  0.00537  0.04102  -0.03075  0.01904

2nd part of bytes B-Filter (0B): 00,26,DB,6E,25,72,2A,A6
1st part of bytes B-Filter (03): 4B,23,C3,22,25,A1,5B,C1

TRANS HYBRID LOSS

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<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
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<tr>
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<td>44.041</td>
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</table>

Additional B-filter delay (in seconds): .625E-04
Bytes for B-filter delay (18): 19,19,11,19
Figure 6
Equivalent Circuit Diagram 1
The configurations 1b) and 1c) can be derived from the equivalent circuit diagram 1a) by zeroing the elements that are not used.

Figure 7
Equivalent Circuit Diagram 2
With $R_{par} = 0$ the entry of a series impedance 2b) becomes possible with equivalent circuit diagram 2a).

Figure 8
Equivalent Circuit Diagram 3
Figure 9

Figure 10
Figure 11

Figure 12
Figure 13

MODUS A11 PEGELMESSG. SE: -- EM: +0.0 dB

EM: ZKAN 2
RESULT dBm0

SE: ZKAN 1 +0.00 dBm0 201 Hz Δ = 100 Hz

A-A
A-D
D-A
D-D
WOB/E
FREQ.

Figure 14

MODUS A33 FREQUENZ SE: -- EM: +0.0 dB

EM: ZKAN 2
RESULT dB

SE: ZKAN 1 +0.00 dBm0 201 Hz Δ = 100 Hz

A-A
A-D
D-A
D-D
WOB/E
FREQ.
# SICOFi® Application Together with Transformer SLIC with Series Feeding

## Contents

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<td>4</td>
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<td>Measurements</td>
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<td>7</td>
<td>Strategies</td>
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## Appendixes

<table>
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<td>A1</td>
<td>Specifications</td>
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<tr>
<td>A2</td>
<td>Measurements</td>
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1 Introduction
Although the trend in Subscriber Line Interface Circuit design is to integrate as many functions as possible, transformers are still often used in the design of public or private exchange line cards mainly because of their low cost, high reliability and better symmetry and galvanic separation.

This note describes an application of the Siemens Signal processing COdec FIlter (SICOFI) in a line card equipped with a transformer for the connection of analog subscriber lines. This is intended to be an example from which the user can build his own circuit and program.

Terminology:
In the following, we will call “SLIC” the hardware and software corresponding to the analog components in a Subscriber Line Interface Circuit excluding the SICOFI chip.

Overview:
This note begins with generalities about transformers and SLIC functions. Then comes an example of line card circuitry. The third part is the calculation of the model for the SLIC. The corresponding software is then described and used in combination with the SICOFI coefficient program. Measurements show the fulfilment of the German Post specifications. Next comes a word about possible strategies. A listing of the TRAFOS SLIC FORTRAN program can be printed by the user from the source file.

2 General

2.1 SLIC Functions
The main functions of the SLIC are to provide the BORSHT functions (Battery feeding, Over-voltage protection, Ringing, Signaling, Hybrid function, Testing).

In the case of a SLIC circuit in combination with the SICOFI, the hybrid function is splitted into the two-wire to four-wire conversion realized by the SLIC and the hybrid balancing provided by the internal B-filter of the SICOFI.

The other functions (such as off-hook detection, metering, standby mode, ringing) do not affect the speech signal. Therefore we will not consider these in the scope of this paper.

The signal on a telephone line can be considered as comprising of two parts:
A DC voltage to feed the subscriber terminal.

An AC voltage (the speech signal) which has to be transferred in both directions: PABX-line (TRANSMIT) and line-PABX (RECEIVE) with the right attenuation and without distortion.

To separate AC and DC correctly, the circuit has to present a high pass at low frequencies and a specified input impedance (matching impedance) in regard to the AC signal.

A flat frequency response is also required.

2.2 Principles

Schematic: A simple SLIC circuit can be schematized as follows:

The feeding can be of different kind:

- Series feeding
  Transformer: Generally iron core

Advantages:
The high frequency current is stopped by the coils of the transformer itself.

Drawbacks:
It is difficult to dimension a transformer with a low leakage inductance. High current in the primary half coils.

A large core is required in order to prevent saturation.
Parallel feeding
Transformer: Generally ferrite core (allows lower leakage inductance but comes easier in saturation)

Advantages:
Blocks the DC current before the transformer coils.

Drawbacks:
Necessity of a blocking circuit before the transformer which includes often a large coil or an electronic circuit with problems of non linearities. Therefore the feeding circuit often presents a frequency dependant equivalent impedance which is not easy to model.

2.3 Transformer Characteristics
Philosophy of the simplifications:

Let us take an ideal transformer with 1 to 1 ratio, let us consider the AC signal only and only one direction at a time.

The equivalent circuit in transmit direction will be:

![Figure 2](image)

and in receive direction:

![Figure 3](image)
We can see that if $Z_L = Z_0$ the attenuation in both directions is 6 dB.

The real circuit is more complicated because of the loop added by the SICOFI Z-filter and because of the non-ideal transformer.

Optional amplifier are also used for several purposes:
- The SICOFI can drive loads only above typically 300 $\Omega$, so that an opamp is not necessary.
- Add gain in receive direction.
- Add possibly group delay if the SICOFI B-filter can not compensate fully the transformer distortion. (Improves the trans hybrid loss at low frequencies).

### 2.4 Equivalent Circuit of the Transformer

A low frequency transformer can be modelled with simple parts:

- $L_1$ main inductance
- $L_{s1}, L_{s2}$ stray inductances
- $R_{CU1}, R_{CU2}$ primary and secondary copper resistance
- $C_W$ winding capacitance
- $W_1, W_2$ number of windings at primary and secondary
- $ZSP$ with $C_{SP}, R_{SP}$ feeding (parallel or serial)

![Figure 4](image-url)

**Figure 4**
2.5 Transformer Measurements

Method:
- Measurement of the primary and secondary copper resistances with a simple Ohmmeter. ($R_{CU1}$ and $R_{CU2}$)
- Short circuit at the secondary:
  Measurement of leakage inductance ($L_{s1}$ and $L_{s2}$) and winding capacitance ($C_w$) with an impedance analyser at 1 kHz.
- Open circuit at the secondary:
  Measurement of the main inductance ($L_1$) with the impedance analyser.
- The other data (number of turns primary and secondary: $W_1$, $W_2$) have to be obtained from the supplier.

Results:
In order to prove the capabilities of the SICOFI for Germany, we have chosen a transformer with series feeding which is simple to use. It has been dimensioned for the specifications of the German Post: $Z_{in}$ must be close to $220 \Omega + (820 \Omega / 115 \text{nF})$ (see specifications in appendix A1)

- $R_{CU1} = 123 \Omega$
- $R_{CU2} = 121 \Omega$
- $L_{s2} = L_{s1} = 4.2 \text{ mH}$
- $C_w = 0.1 \text{ nF}$
- $L_1 = 0.835 \text{ H}$
- $W_1 = 1400$
- $W_2 = 1400$

Note: The main inductance has a large influence on the frequency response at low frequencies: It forms a high pass filter with the copper resistances and the line impedance; the cut-off frequency should be kept as low as possible by increasing $L_1$. The leakage inductances influence more the high frequency response (they form a low pass with the winding capacitance and therefore limit the frequency band of the transformer). The winding capacitance can be decreased by using a shielding screen between the primary and secondary windings.
3 Hardware

Our circuit is a didactic circuit with a series feeding and values for \( Z_0 \) that have been optimized by trying different resistors and capacitors in order to obtain an optimum with the SLIC alone (Z-filter switched off).

Figure 5

Transformer Siemens EK 25 Nr. EK C39030-Z4-C15

\[
\begin{align*}
Z_{\text{GRA1}} & = 953 \, \Omega \\
Z_{\text{OCA2}} & = 200 \, \text{nF} \\
D1 & = 3V9 \\
D2 & = 3V9 \\
C_{\text{SP}} & = 2.2 \, \mu \text{F}, 63 \, \text{V} \\
R_{\text{SP}} & = 4 \times 100 \, \Omega, 1 \, \text{W}
\end{align*}
\]
4 Software

4.1 Introduction

The following two ports models ("black boxes" which the user can change as he wishes) are used to model the transformer.

Admittance Matrix:

\[
\begin{align*}
&i_1 = Y_{11} v_1 + Y_{12} v_2 \\
&i_2 = Y_{21} v_1 + Y_{22} v_2
\end{align*}
\]

Chain Matrix:

\[
\begin{align*}
&v_1 = A_{11} v_2 + A_{12} i_2 \\
&i_1 = A_{21} v_2 + A_{22} i_2 \\
&\text{where } i_2 = -i_2
\end{align*}
\]

In the model, chain matrix (A-matrix) are first used in order to make easy chain multiplications and improve the modularity of the program.

Then the transformer is considered by its admittance matrix (subroutine TRSLIC).
4.2 Conventions
As we are working with two ports model, we need $2 \times 2$ matrixes and because we work with complex numbers we need a third dimension:

The matrixes are declared as arrays of dimension 3:

$$A(2,2,2)$$

where the first number is 1 for real and 2 for imaginary part and the two other ones are for lines and columns of the matrix.

After the multiplications, these matrixes are reduced to their elements (complex):

$$A_{11}(2), A_{12}(2), A_{21}(2), A_{22}(2)$$

in other words:

$$A(1,1,1) + j \times A(2,1,1) = A_{11}(1) + j \times A_{11}(2)$$

4.3 Subroutines
The transformer is modelled in the subroutine TRSLIC.

Input is FREQ (frequency);
Output of this routine are the $Y$ parameter of the transformer, including the $Y$-matrix determinant.

TRSLIC uses subroutines which are the elementary $A$-matrix calculations:

4.4 Elementary $A$-Matrixes

4.4.1 SERA
SERies A-matrix
$Y$: admittance in series

$$\begin{align*}
Y_{I_1} & = V_{1} + V_{2} / Y \\
I_{1} & = I_{2}
\end{align*}$$

$$\begin{bmatrix}
1 & 1/Y \\
0 & 1
\end{bmatrix}$$
4.4.2 PARA
PARallel A-matrix
Y: admittance in parallel

\[
\begin{align*}
V_1 &= V_2 \\
I_1 &= Y \times V_2 + I_2 \\
\text{PARA} &= \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}
\end{align*}
\]

4.4.3 Transformer

\[
\begin{align*}
V_1 &= \left(\frac{w_1}{w_2}\right) \\
I_1 &= \left(\frac{w_1}{w_2}\right) \\
u &= \left(\frac{w_1}{w_2}\right) \\
A6 &= \begin{bmatrix} 1/u & 0 \\ 0 & u \end{bmatrix}
\end{align*}
\]

If the transformer has inverted coils then change the sign of \(u\) (it is equivalent to make \(w_2 = -w_2\)).
4.5 Model Calculations

The resulting A-matrix is: \[ A = A_5 \times A_7 \times A_1 \times A_2 \times A_6 \times A_3 \times A_4 \]

**Figure 6**

**Note**: "x" is a complex matrix multiplication: See subroutine CMATMUL

Admittance elements of the different matrices:

\[ W = 2\pi \times F_{REQ} \]

* \[ Y_1 = 1 / (R_{CU1} + j \times W \times L_{S1}) \]
* \[ Y_2 = 1 / j \times W \times L_1 \]
* \[ Y_3 = 1 / (R_{CU1} + j \times W \times L_{S2}) \]
* \[ Y_4 = j \times W \times C_W \]

Parallel feeding

* \[ Y_5 = 1 / Z_{SP} \]
* \[ Y_7 = j \times W \times C_{SP} \]

Series feeding

* \[ Y_5 = 0 \]
* \[ Y_7 = C_{SP} / R_{SP} \]

\[ = 1 / R_{SP} + j \times W \times C_{SP} \]
4.5.1 Y-Matrix
From the A parameters, we can compute the Y parameters (*):
\[ Y_{11} = \frac{A_{22}}{A_{12}} \quad Y_{12} = -\frac{\text{DETA}}{A_{12}} \]
\[ Y_{21} = -\frac{1}{A_{12}} \quad Y_{22} = \frac{A_{11}}{A_{12}} \]
and \( Y_{\text{DET}} = Y_{11} \times Y_{22} - Y_{12} \times Y_{21} \)

4.5.2 SLIC M-Matrix
An additional amplifier (AX) has been added in transmit direction so that the circuit is as general as possible.
Schematic circuit diagram of transformer SLIC software: figure 7 and figure 8.
Figure 7
Figure 8

Impedance Models
Notes: ● Each block is modifyable by the user.
  ● The gains are controllable by 9 parameters:
    Example for AR (similar for AX)
  ● Denominator impedance: ARZD using the model ERZD=1, ERZD=2 or ERZD=3
  ● Nominator impedance: ARZN using the model ERZN=1, ERZN=2 or ERZN=3.
    Normally ERZN > 0 : AR = 1 + ARZN / ARZD
    Normally ERZN < 0 means that there is no gain in this direction (AR=1)
    ERZN < 0 : AR = – ARZN / ARZD

The matching impedance $Z_0$ is modelled with 6 parameters:
$Z_{0RA1}, Z_{0CA1}, Z_{0RA2}, Z_{0CA2}$: parallel part
$Z_{0RS}, Z_{0CS}$: serial part

Calculations:
Transformer equations:
(1) $I_1 = Y_{11} \times V_1 + Y_{12} \times V_{20}$
(2) $I_{20} = Y_{21} \times V_1 + Y_{22} \times V_{20}$
  determinant: $YDET = Y_{11} \times Y_{22} - Y_{12} \times Y_{21}$
A. Calculation of M11 Matrix Parameter:

\[ M_{11} = \frac{I_1}{V_1} \text{ when } V_3 = 0 \]

This is exactly the admittance \( Y_p \) seen at the primary side of the transformer when the impedance \( Z_0 \) is at the secondary. (*)

\[ Y_p = \frac{Y_{11} \times 1/Z_0 + Y_{DET}}{Y_{22} + 1/Z_0} \]

\[ = \frac{Y_{11} + Y_{DET} \times Z_0}{Y_{22} \times Z_0 + 1} \]

Then:

\[ M_{11} = \frac{Y_{11} + Y_{DET} \times Z_0}{1 + Y_{22} \times Z_0} \]

B. Calculation of M12 Matrix Parameter:

\[ M_{12} = \frac{I_1}{V_3} \text{ when } V_1 = 0 \]

The equations (1) and (2) are now:

1. \( I_1 = Y_{12} \times V_{20} \)
2. \( I_2 = Y_{22} \times V_{20} \)

The impedance seen at the secondary side of the transformer when a short circuit is at the primary side (*):

3. \( Z_{OUT} = \frac{1}{Y_{22}} \)
4. \( V_{20} / Z_{OUT} = AR \times V_3 / (Z_0 + Z_{OUT}) \) (voltage divider)

then from (3) and (4): \( V_{20}/V_3 = AR / (1 + Y_{22} \times Z_0) \)
and with (1):

\[ M_{12} = \frac{I_1}{V_3} = Y_{12} \times AR / (1 + Y_{22} \times Z_0) \]

C. Calculation of M21 Matrix Parameter:

\[ M_{21} = \frac{V_2}{V_1} \text{ when } V_3 = 0 \]

The relation between \( V_2 \) and \( I_2 \) is: \( V_{20} = -Z_0 \times I_2 \)
Then by replacing this in (2), we obtain:

\[ - \frac{V_{20}}{Z_0} = Y_{21} \times V_1 + Y_{22} \times V_{20} \]

which is equivalent to: \( V_{20}/V_1 = -Y_{21}/Y_{22} + 1/Z_0 \)

\[ V_2 = AX \times V_{20} \]

Therefore:

\[ M_{21} = -AX \times Z_0 \times Y_{21} / (1 + Z_0 \times Y_{22}) \]
D. Calculation of M22 Matrix Parameter:

\[
M22 = \frac{V_2}{V_3} \text{ when } V_1 = 0
\]

The calculations are then straightforward:

\[
\frac{V_2}{V_3} = Ax \times Ar \times \left( \frac{Z_{IN}}{Z_{IN} + Z_0} \right)
\]

\( Z_{IN} \) is the impedance seen at the secondary side of the transformer when there is a short circuit at the primary. (*)

\[
Z_{IN} = \frac{1}{Y_{22}}
\]

Then:

\[
M22 = \frac{V_2}{V_3} = \frac{Ax \times Ar}{1 + Z_0 \times Y_{22}}
\]

(*) See "Linear Integrated Networks"

G.S. Moschytz

Bell Telephone Laboratories Series

Van Nostrand Reinhold Company

Summary:

\[
M_{11} = \frac{A}{(Y_{11} + Y_{DET} \times Z_0)/(1 + Y_{22} \times Z_0)}
\]

\[
M_{12} = \frac{B}{Y_{12} \times AR / (1 + Z_0 \times Y_{22})}
\]

\[
M_{21} = \frac{C}{-AX \times Z_0 \times Y_{21} / (1 + Z_0 \times Y_{22})}
\]

\[
M_{22} = \frac{D}{AX \times AR / (1 + Z_0 \times Y_{22})}
\]
5 Optimization

5.1 Input Data

The TRAFOS SLIC program needs a file as input which contains the data of the SLIC:

*ERZN : receive gain = 1+arzn/arzd or -arzn/arzd if erzn < 0
  0
*ARRSN, ARRPN, ARCSN, ARCPN
  0. 0. 0. 0.
*ERZD
  0
*ARRSD, ARRPD, ARCSD, ARCPD
  0. 0. 0. 0.
*EXZN : transmit gain = 1+axzn/axzd or -axzn/axzd if exzn < 0
  0
*AXRSN, AXRPN, AXCSN, AXCPN
  0. 0. 0. 0.
*EXZD
  0
*AXRSD, AXRPD, AXCSD, AXCPD
  0. 0. 0. 0.
*RCU1 RCU2 : copper resistance of primary (resp. secondary)
  123. 121.
*L1
  0.835
*L1
  0.42E-02
*LS1 LS2 : leakage inductances primary and secondary
  0.42E-02
*CW
  0.1E-09
*RSP CSP : feeding resistance and capacitance
  400.0 0.22E-05
*W1 W2 : Number of turn for windings
  0.14E+04 0.14E+04
*ZSLI
  0.5
*Z0 : matching impedance (with 6 elements)
  *Z0RA1, Z0CA1, Z0CA2, Z0RA2
  953. 0. 0.2E-06 0.
*Z0RS, Z0CS
  0. 0.

5.2 Runs

Specifications:

The specifications for West-Germany (see BRD.SPE in appendix A1)

A first run with automatical Z-filter optimization (PZIN = 0) does not give satisfying results for the return loss.

A second run with modified specifications (see BRD4.SPE in appendix A1) is necessary with repetition of the Z-filter optimization (ZREP = Y).

Result file:

NICE.RES is a result file which has been obtained with a version V3.x of SICOFI program.
NICE.RES:

Input_file_name: NICE.CTL         Date: 18.04.88 10:03
SPEC = BRD4.SPE                SLIC = TRAFOS.SLI
BYTE = REF.BYT               CHNR = 0,A
PLO = N

ON = ALL            REL = Y          SHORT = N
OPT = Z+X+R+B     ZXR = NNNN
FZ = 300.00   3400.0      ZLIM = 2.00
ZREP = N         ZSIGN = 1
FR = 360.00    3390.0
RFIL = N           RREFQ = N    RREF = 1.5367
FX = 500.00    3300.0
XFIL = N           XREFQ = N    XREF = -2.5370
PB = 10       GWFB = 0.500E-01 TBM = 1
FB = 300.00    500.00     700.00  1000.0  1500.0
   2100.0   2300.0   2900.0  3200.0  3300.0
WFB = 4.0000    2.0000    1.0000  5.0000  1.0000
   2.0000    1.0000    5.0000  1.0000  1.0000
APOF = 0.00E+00 DPOF = 0.00E+00 APRE = 0.00E+00 DPRE = 0.00E+00
XZQ = 0.49121093750000000E+00 -0.14257812500000000E+00
   -0.40625000000000000E+00 -0.12988281250000000E+00
   0.18359375000000000E+00
XRQ = 0.65625000000 0.2695312500 0.0332031250 0.0234375000
   0.0244140625
XXQ = 1.2187500000 0.1542968750 -0.1640625000 -0.0078125000
   -0.0019531250
XBQ = 0.35937500000000000E+00 0.13671875000000000E+00
   0.74218750000000000E+00 -0.57031250000000000E+00
   -0.60937500000000000E+00
XGQ = 0.5742187500 1.6406250000

; Bytes for Z-Filter (13): 30,C1,5B,92,1B,3B,13,3E
Bytes for R-Filter (2B): 50,BA,94,42,C9,42,12,22
Bytes for X-Filter (23): D0,C8,8C,BB,22,23,0C,B2
Bytes for Gain-factors (30): 31,A2,10,32
2nd part of bytes B-Filter (0B): 00,1A,0A,AB,38,24,B1,21
1st part of bytes B-Filter (03): 92,B2,39,13,D1,33,2B,B1
Bytes for B-filter delay (18): 19,19,11,19

* TRAFO SLIC

*Z0RA1= 953.00   *Z0CA1= .00000   *Z0RA2= .00000
*Z0CA2= .20000E-06*Z0RS = .00000   *Z0CS = .00000
* ERZN= 0     *ARRSN= .00000   *ARCSN= .00000   *ARRPN= .00000   *ARCPN= .00000
* ERZD= 0   *ARRSD= .00000   *ARCSD= .00000   *ARRPD= .00000   *ARCPD= .00000
* EXZN= 0  *AXRSN= .00000   *AXCSN= .00000   *AXRPN= .00000   *AXCPN= .00000
* EXZD= 0
Z-FILTER calculation results
Generator impedance ZI at a,b line!
Calculated and quantized coefficients:

\[
\begin{align*}
XZ &= 0.49089 - 0.14218 - 0.41298 - 0.13023 + 0.18335 \\
XZQ &= 0.49121 - 0.14258 - 0.40625 - 0.12988 + 0.18359 \\
\end{align*}
\]

Bytes for Z-Filter (13): 30, C1, 5B, 92, 1B, 3B, 13, 3E

RETURN LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>10.464</td>
<td>1800.</td>
<td>24.463</td>
</tr>
<tr>
<td>200.</td>
<td>12.502</td>
<td>1900.</td>
<td>23.683</td>
</tr>
<tr>
<td>300.</td>
<td>14.850</td>
<td>2000.</td>
<td>23.095</td>
</tr>
<tr>
<td>400.</td>
<td>17.047</td>
<td>2100.</td>
<td>22.680</td>
</tr>
<tr>
<td>500.</td>
<td>19.118</td>
<td>2200.</td>
<td>22.432</td>
</tr>
<tr>
<td>600.</td>
<td>21.177</td>
<td>2300.</td>
<td>22.359</td>
</tr>
<tr>
<td>700.</td>
<td>23.354</td>
<td>2400.</td>
<td>22.477</td>
</tr>
<tr>
<td>800.</td>
<td>25.792</td>
<td>2500.</td>
<td>22.824</td>
</tr>
<tr>
<td>900.</td>
<td>28.673</td>
<td>2600.</td>
<td>23.458</td>
</tr>
<tr>
<td>1000.</td>
<td>32.201</td>
<td>2700.</td>
<td>24.485</td>
</tr>
<tr>
<td>1100.</td>
<td>35.992</td>
<td>2800.</td>
<td>26.083</td>
</tr>
<tr>
<td>1200.</td>
<td>36.559</td>
<td>2900.</td>
<td>28.532</td>
</tr>
<tr>
<td>1300.</td>
<td>33.524</td>
<td>3000.</td>
<td>31.690</td>
</tr>
<tr>
<td>1400.</td>
<td>30.624</td>
<td>3100.</td>
<td>31.133</td>
</tr>
<tr>
<td>1500.</td>
<td>28.425</td>
<td>3200.</td>
<td>26.214</td>
</tr>
<tr>
<td>1600.</td>
<td>26.758</td>
<td>3300.</td>
<td>21.848</td>
</tr>
<tr>
<td>1700.</td>
<td>25.469</td>
<td>3400.</td>
<td>18.387</td>
</tr>
</tbody>
</table>

Min. Z-loop reserve: 1.053 dB
at frequency: 7000.0 Hz

Min. Z-loop mirror signal reserve: 4.793 dB
at frequency: 6500.0 Hz

Run # 1

X-FILTER calculation results
Calculated and quantized coefficients:

\[
\begin{align*}
XX &= 1.21418 \ 0.15483 \ -0.16741 \ -0.00821 \ -0.00233 \\
XXQ &= 1.21875 \ 0.15430 \ -0.16406 \ -0.00781 \ -0.00195 \\
\end{align*}
\]

Bytes for X-Filter (23): D0, C8, 8C, BB, 22, 23, 0C, B2

GX results:
All attenuation values (in dB) refer to FREF = 1014. Hz
Calculation of transmit transfer function (AD)

All attenuation values (in dB) refer to FREF = 1014.0 Hz

Generator impedance ZI at a,b line!

TGREF CA = 0.327 ms  TGREF CB = 0.340 ms

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>18.755</td>
<td>3.232</td>
<td>2000.</td>
<td>0.000</td>
<td>0.013</td>
</tr>
<tr>
<td>200.</td>
<td>1.722</td>
<td>2.198</td>
<td>2100.</td>
<td>-0.006</td>
<td>0.018</td>
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<tr>
<td>300.</td>
<td>0.411</td>
<td>0.815</td>
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<td>0.032</td>
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<td>0.040</td>
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<td>-0.016</td>
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<tr>
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<td>0.101</td>
<td>2600.</td>
<td>-0.015</td>
<td>0.062</td>
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<tr>
<td>800.</td>
<td>-0.024</td>
<td>0.065</td>
<td>2700.</td>
<td>-0.013</td>
<td>0.076</td>
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<tr>
<td>900.</td>
<td>-0.008</td>
<td>0.042</td>
<td>2800.</td>
<td>-0.007</td>
<td>0.093</td>
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<tr>
<td>1000.</td>
<td>0.008</td>
<td>0.026</td>
<td>2900.</td>
<td>0.002</td>
<td>0.113</td>
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<tr>
<td>1100.</td>
<td>0.020</td>
<td>0.015</td>
<td>3000.</td>
<td>0.018</td>
<td>0.136</td>
</tr>
<tr>
<td>1200.</td>
<td>0.028</td>
<td>0.008</td>
<td>3100.</td>
<td>0.043</td>
<td>0.166</td>
</tr>
<tr>
<td>1300.</td>
<td>0.032</td>
<td>0.003</td>
<td>3200.</td>
<td>0.086</td>
<td>0.202</td>
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<tr>
<td>1400.</td>
<td>0.032</td>
<td>0.001</td>
<td>3300.</td>
<td>0.156</td>
<td>0.249</td>
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<td>1500.</td>
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<td>1600.</td>
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<td>0.001</td>
<td>3500.</td>
<td>0.473</td>
<td>0.395</td>
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<td>1700.</td>
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<td>0.002</td>
<td>3600.</td>
<td>0.828</td>
<td>0.519</td>
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<tr>
<td>1800.</td>
<td>0.012</td>
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R-FILTER calculation results

Calculated and quantized coefficients:

XR = 0.65560  0.27251  0.03267  0.02341  0.02505
XRQ = 0.65625  0.26953  0.03320  0.02344  0.02441

Bytes for R-Filter (23): 50,BA,94,42,C9,42,12,22

GR results:

All attenuation values (in dB) refer to FREF = 1014.0 Hz

TGREF CA = 0.264 ms  TGREF CB = 0.247 ms
Run # 1
B-FILTER calculation results
Terminating impedance ZL at a,b line!

Calculated and quantized coefficients:

\[
\begin{align*}
\mathbf{XB} &= 0.35600 \quad 0.13862 \quad 0.74342 \quad -0.56848 \quad -0.60448 \\
& \quad 0.65780 \quad 0.36312 \quad -1.13668 \quad 0.89881 \quad -0.34413 \\
\mathbf{XBQ} &= 0.35937 \quad 0.13867 \quad 0.74219 \quad -0.57031 \quad -0.60937 \\
& \quad 0.65625 \quad 0.35937 \quad -1.13281 \quad 0.90625 \quad -0.34375 \
\end{align*}
\]

2nd part of bytes B-Filter (0B): 00,1A,0A,AB,38,24,B1,21
1st part of bytes B-Filter (03): 92,B2,39,13,D1,33,2B,B1

TRANS HYBRID LOSS

\[
\begin{align*}
\text{FREQ} & \quad \text{loss} \\
(\text{Hz}) & \quad (\text{dB}) \\
100. & \quad 22.902 \\
200. & \quad 13.779 \\
300. & \quad 18.401 \\
400. & \quad 23.795 \\
500. & \quad 29.665 \\
600. & \quad 32.722 \\
700. & \quad 31.077 \\
800. & \quad 29.704 \\
900. & \quad 29.509 \\
1000. & \quad 30.459 \\
1100. & \quad 32.798 \\
1200. & \quad 37.665 \\
1300. & \quad 51.231 \\
1400. & \quad 38.240 \\
1500. & \quad 32.000 \\
1600. & \quad 28.571 \\
1700. & \quad 26.415 \\
1800. & \quad 22.902 \\
1900. & \quad 13.779 \\
2000. & \quad 18.401 \\
2100. & \quad 23.795 \\
2200. & \quad 29.665 \\
2300. & \quad 32.722 \\
2400. & \quad 31.077 \\
2500. & \quad 29.704 \\
2600. & \quad 29.509 \\
2700. & \quad 30.459 \\
2800. & \quad 32.798 \\
2900. & \quad 37.665 \\
3000. & \quad 51.231 \\
3100. & \quad 38.240 \\
3200. & \quad 32.000 \\
3300. & \quad 28.571 \\
3400. & \quad 26.415 \\
3500. & \quad 22.902 \\
3600. & \quad 13.779 \\
3700. & \quad 18.401 \\
3800. & \quad 23.795 \\
3900. & \quad 29.665 \\
4000. & \quad 32.722 \\
4100. & \quad 31.077 \\
4200. & \quad 29.704 \\
4300. & \quad 29.509 \\
4400. & \quad 30.459 \\
4500. & \quad 32.798 \\
4600. & \quad 37.665 \\
4700. & \quad 51.231 \\
4800. & \quad 38.240 \\
4900. & \quad 32.000 \\
5000. & \quad 28.571 \\
5100. & \quad 26.415 \\
\end{align*}
\]

Additional B-filter delay (in seconds): .625E-04
Bytes for B-filter delay (18): 19,19,11,19
6 Measurements

See appendix A2
The measurements are made with a "PCM4" from Wandel & Goltermann.

Return loss: correct.

Transmit direction (AD): Level at 1 kHz: – 0.18 dB (wanted: 0 dB). A small manual correction will be necessary.


Attenuation distortion (AD and DA): correct.

Trans Hybrid Loss (THL): should be improved!

To have a better THL, it is necessary to design an other transformer.

7 Strategies

The SICOFI makes it possible to use the same hardware for different countries specifications by changing the coefficients programming of the SICOFI.

In general, it is necessary to already have a good return loss with the transformer alone without SICOFI. Then SICOFI improves the figures.

This requires us however to optimize the SLIC circuitry using the program as a simulation tool (especially Z-filter optimization):

1. Set \( Z_0 \) to a given value
2. Run automatical Z-filter optimization for the given \( Z_0 \) impedance and for all the specifications.
3. Change the impedance \( Z_0 \)
4. Redo step 1 until having obtained an optimum.
Appendix A1

Specifications

**BRD.SPE**

- **FREF = 1014.0**  **LAW = A**
- **UREF= 0.9488**  **RLX = 0**  **RLR = -7.0**
- **ABIMP = ZI**
- **ERZI= 1**  **RSER= 220.**  **CPAR= 0.115E-06**
- **ERZL= 1**  **RSL = 220.**  **CPL = 0.115E-06**

| ZIN | FR | 300 | 500 | 3k | 3.4k |
| AT- | 0  | 20  | 20  | 16 |
| AT+ | 16 | 20  | 20  | 0  |

| ZMIR | FR | 4k | 12k |
| AT- | 30 | 3  |
| AT+ | 30 | 3  |

| DA,UPPER | FR | 300 | 500 | 2.7k | 3k | 3.4k |
| AT- | 100 | .75 | .25 | .35 | .75 |
| AT+ | .75 | .25 | .35 | .75 | 100 |

| DA,LOWER | FR | 300 | 3.4k |
| AT- | 0   | -.25 |
| AT+ | -.25 | 0   |

| DA,DELAY | FR | 500 | 600 | 1k | 2.6k | 2.8k |
| GD- | 10k | .420 | .150 | .085 | .150 |
| GD+ | .420 | .150 | .085 | .150 | 10k |

| AD,UPPER | FR | 300 | 500 | 2.7k | 3k | 3.4k |
| AT- | 100 | .75 | .25 | .35 | .75 |
| AT+ | .75 | .25 | .35 | .75 | 100 |

| AD,LOWER | FR | 300 | 3.4k |
| AT- | 0   | -.25 |
| AT+ | -.25 | 0   |

| AD,DELAY | FR | 500 | 600 | 1k | 2.6k | 2.8k |
| GD- | 10k | .420 | .150 | .085 | .150 |
| GD+ | .420 | .150 | .085 | .150 | 10k |

| DD | FR | 300 | 500 | 2.5k | 3.4k |
| AT- | 0   | 27  | 27  | 23 |
| AT+ | 23  | 27  | 27  | 0  |
## BRD4.SPE

**FREF = 1014.0**  
**LAW = A**

**UREF= 0.9480**  
**RLX = 0.**  
**RLR = -7.0**

**ABIMP = ZI**

**ERZI= 1**  
**RSER= 220.**  
**RPAR= 820.**  
**CPAR= 0.115E-06**

**ERZL= 1**  
**RSL = 220.**  
**RPL = 820.**  
**CPL = 0.115E-06**

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Appendix A2

Measurements

Figure 9
Figure 10

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SICOFI® Application Together with Transformer SLIC with Transverse Feeding

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1 Introduction

Although the trend in Subscriber Line Interface Circuit is to integrate as many functions as possible, transformers are still often used in the design of public or private exchange line cards mainly because of their low cost, high reliability and better symmetry and galvanic separation.

This note describes an application of the Siemens Signal COdec Filter (SICOFI) in a line card equipped with a transformer for the connection of analog subscriber lines.

Terminology:
In the following, we will call "SLIC" the hardware and software corresponding to the analog components in a Subscriber Line Interface Circuit excluding the SICOFI chip.

Overview:
This note begins with generalities about SLIC functions.

Then comes an example of solution for the line card circuitry.

The next part is the calculation of the model for the SLIC.

The corresponding software is then described and used in combination with the SICOFI coefficient program.

Measurements show the fulfilment of the German Post specifications. Next comes a word about possible strategies to optimize SICOFI coefficients. In the appendix, the listing of the TRAFO SLIC FORTRAN program (written with Microsoft FORTRAN compiler) is given.

2 Generalities

2.1 SLIC Functions

The main functions of the SLIC are to provide the BORSHT functions (Battery feeding, Overvoltage protection, Ringing, Signaling, Hybrid function, Testing). In the case of a SLIC circuit in combination with the SICOFI, the Hybrid function is splitted into the two-wire to four-wire conversion realized by the SLIC and the hybrid balancing provided by the internal B-filter of the SICOFI. The other functions (such as off-hook detection, metering, standby mode, ringing) do not affect the speech signal. Therefore we will not consider these in the scope of this note.

The signal on a telephone line can be considered as comprising of two parts:

- A DC voltage to feed the subscriber terminal.
- An AC voltage (the speech signal) which has to be transferred in both directions: PABX-line (TRANSMIT) and line-PABX (RECEIVE) with the right attenuation and without distortion.

To separate AC and DC correctly, the circuit has to present a high pass with a very low cut-off frequency and a specified input impedance (matching impedance) in regard to the AC signal. A flat frequency response is also required.
2.2 Principles

Schematic:

A simple SLIC circuit can be schematized as follow:

![Schematic of a SLIC circuit](image)

**Figure 1**

The feeding can be of different kind:

- **Series feeding**
  Transformer: Generally iron core
  Advantages:
  - The high frequency current is stopped by the coils of the transformer itself.
  Drawbacks:
  - It is difficult to dimension a transformer with a low leakage inductance.
  - High current in the primary half coils.
  - A large core is required in order to prevent saturation.

- **Parallel feeding**
  Transformer: Generally ferrite core (allows lower leakage inductance but comes faster in saturation)
  Advantages:
  - Blocks the DC current before the transformer coils.
  Drawbacks:
  - Necessity of blocking circuit before the transformer which includes often a large coil or an electronic circuit with problems of non linearities. Therefore the feeding circuit often presents a frequency dependant equivalent impedance which is not easy to model.
2.3 Transformer Characteristics
Philosophy of the simplifications:
Let us take an ideal transformer with 1 to 1 ratio, let us consider the AC signal only and only one direction at a time.
The equivalent circuit in transmit direction will be:

![Figure 2](image1)

Figure 2
and in receive direction:

![Figure 3](image2)

Figure 3

We can see that if $Z_L = Z_0$ the attenuation in both directions is 6 dB.
The real circuit is more complicated because of the loop added by the SICOFI Z-filter and because of the non-ideal transformer.
The SICOFI can drive loads only above typically 300 $\Omega$, so that an opamp is not necessary.
3 Hardware
A transformer SLIC with transverse feeding was chosen with the corresponding T-circuit model with mutual inductance.

3.1 Equivalent Circuit

![Equivalent Circuit Diagram]

**Figure 4**

Components of the equivalent circuit:

- **M**: mutual inductance
- **L_{1s}, L_{2s}**: theoretical stray inductances \((L_{1s} = L_1 - M, L_{2s} = L_2 - M)\)
- **R_{CU1}, R_{CU2}**: primary and secondary resistances
- **C_{W1}, C_{W2}**: primary and secondary winding capacitances
- **ZFEED**: complex feeding impedance
3.2 Measurement Method

The whole measurement occurs in 7 steps:

**Step 1: Measurement** of the primary and secondary copper resistance with a simple Ohmmeter ($R_{CU1}$ and $R_{CU2}$).

**Step 2: open circuit at the secondary**
Measurement of the transformer resonance frequencies by using an impedance analyzer, with Parallel equivalent circuit [P] or Series equivalent circuit [S].

- primary side $\rightarrow f_{01}$ with [P] and $f_{02}$ with [S]
- secondary side $\rightarrow f_{01}'$ with [P] and $f_{02}'$ with [S]

**Step 3: open circuit at the secondary**
Measurement of winding inductance $L_{1M}$ and $L_{2M}$ at low frequency ($f_m = 300$ Hz) and with [S].

**Step 4: Determination** of the correction factors $n_1$ and $n_2$

with $n_1 = f_m / f_{01}$ and $n_2 = f_m / f_{01}'$

**Step 5: Calculation** of the actual primary and secondary inductance

$L_1 = L_{1M} (1 - n_1^2)$ and $L_2 = L_{2M} (1 - n_2^2)$

**Step 6: short circuit at the secondary**
Measurement of the stray inductance $L_{1k}$ at frequency $f_{01}$ with [S]

**Step 7: Determination** of the theoretical mutual inductance $M$, stray factor $s$ and response ratio

\[
M = \sqrt{L_2 \times (L_1 - L_{1k})} \quad \hat{u} = \sqrt{L_1 / L_2}
\]

$L_{1s} = L_1 - M$ \hspace{1cm} $s = L_{1s} / L_1$

\[
C_{W1} = \frac{\hat{u}}{(2\pi \times f_{02}^{'})^2 \times L_1 \times s}
\]

\[
C_{W2} = \frac{1}{(2\pi \times f_{02}^{'})^2 \times L_2 \times s \times \hat{u}}
\]
Results:
In order to prove the capabilities of the SICOFI for Germany with this model, we have chosen a transformer with following data.

\[ R_{CU1} = 84 \, \Omega \quad R_{CU2} = 105 \, \Omega \]
\[ L_1 = 1.15 \, H \quad L_2 = 1.15 \, H \]
\[ M = 1.148 \, H \]
\[ C_1 = C_{W1} = 113 \, pF \quad C_2 = C_{W2} = 135 \, pF \]

3.3 Trafo SLIC Layout

Figure 5
D1, D2 : Overvoltage protection zener-diodes C2V7

\[ C_{SP} = 1 \, \mu F \]
\[ Z_{ORA1} = 700 \, \Omega \]
\[ Z_{OCA2} = 0.1 \, \mu F \]
\[ R_F = R_{CU} + R_1 + R_2 = 792 \, \Omega \]
\[ L_F = 2 \, H \]
\[ C_F = 2 \, nF \]

\( R_{CU} \) is the copper resistor of the coil \( L_F \);
\( C_F \) is the stray capacitor of the coil. It is therefore not actually in the layout of the circuit but was measured with the impedance analyser.

Our circuit is a didactic circuit with a value for \( Z_0 \) that has been optimized by trying different resistors and capacitors with a decade in order to obtain an optimal return loss with the SLIC while the Z-filter is switched off.
4 Software

4.1 Introduction
The following two ports model ("black box" which the user can change as he wishes) is used to model the transformer.

Chain matrix:

\[\begin{align*}
  i_1 & = A_{11} v_1 + A_{12} i_2 \\
  v_1 & = A_{21} v_1 + A_{22} i_2 \\
  i_2 & = -i_2
\end{align*}\]

The model matrix (A-matrix) are used in order to make easy matrix multiplications and improve the modularity of the program.

4.2 Conventions
As we are working with two ports model, we need \(2 \times 2\) matrixes and because we work with complex numbers, we need a third dimension:

The matrixes are declared as arrays of dimension 3:

\[A(2,2,2)\]

where the first number is 1 for real and 2 for imaginary part and the two other ones are for lines and columns of the matrix.

After the multiplications, these matrixes are reduced to their elements (complex):

\[A_{11}, A_{12}, A_{21}, A_{22}\]

Example: \(A_{12} = A(1,1,2) + j \times A(2,1,2)\)

4.3 Subroutines
The transformer is modeled in the subroutine TRSLIC.

The input variable is FREQ (frequency);

Outputs of this routine are the A-parameter of the transformer, including the determinant.

The feeding circuit is modelled in the subroutine ZFEED.
**Note**: The subroutines TRSLIC and ZFEED have to be modified by the user in order to model his own circuit.

TRSLIC uses subroutines which are the elementary A-matrix calculations:

Subroutine SERA (SERies A-matrix)
Y: admittance in series

\[
\begin{align*}
V_1 &= V_2 + I_2 / Y \\
I_1 &= I_2 \\
\end{align*}
\]

Subroutine SERA:
\[
\begin{pmatrix}
1 & 1/Y \\
0 & 1 \\
\end{pmatrix}
\]

Subroutine PARA (PARallel A-matrix)
Y: admittance in parallel

\[
\begin{align*}
V_1 &= V_2 \\
I_1 &= Y V_2 + I_2 \\
\end{align*}
\]

Subroutine PARA:
\[
\begin{pmatrix}
1 & 0 \\
Y & 1 \\
\end{pmatrix}
\]
4.4 Model of the Transformer with Transverse Feeding

Figure 7

\[ A = A_5 \times A_7 \times A_2 \times A_1 \times A_6 \times A_3 \times A_4 \]

Note: "\( \times \)" is a complex multiplication: see subroutine CMATMUL

Admittance elements of the different matrices:

\[ w = 2\pi \times f \]

\[ Y_1 = \frac{1}{R_{CU1} + j \times W \times (L_{1M})} \]
\[ Y_2 = j \times 2 \times C_{W1} \]
\[ Y_3 = \frac{1}{R_{CU2} + j \times W \times (L_{2M})} \]
\[ Y_4 = j \times W \times C_{W2} \]
\[ Y_6 = \frac{1}{j \times W \times M} \]

here transverse feeding:

\[ Y_5 = \frac{1}{Z_{FEED}} = \frac{1}{(R_F + (j \times W \times L_F)) // C_F} \]
\[ Y_7 = j \times W \times C_{SP} \]

4.5 K or M Matrix Calculations

(see the SICOFI program description for the definition of these parameters)

Transformer equations:

(1) \[ V_1 = A_{11} \times V_{20} + A_{12} \times (-I_{20}) \]
(2) \[ I_1 = A_{21} \times V_{20} + A_{22} \times (-I_{20}) \]

and \( ADET = A_{11} \times A_{22} - A_{12} \times A_{21} \)

(see figure 1)
4.5.1 M-Parameters
The SLIC is described by the following two equations:
\[ I_1 = M_{11} \times V_1 + M_{12} \times V_3 \]
\[ V_2 = M_{21} \times V_1 + M_{22} \times V_3 \]

A. Calculation of M11 Matrix Parameter

\[ M_{11} = \frac{I_1}{V_1} \text{ when } V_3 = 0 \]

This is exactly the admittance \( Y_p \) seen at the primary side of the transformer when the impedance \( Z_0 \) is at the secondary. (*)
\[ Y_p = \frac{(A_{21} \times Z_0 + A_{22})}{(A_{11} \times Z_0 + A_{12})} \]

Then:
\[ M_{11} = \frac{(A_{21} \times Z_0 + A_{22})}{(A_{11} \times Z_0 + A_{12})} \]

B. Calculation of M12 Matrix Parameter

\[ M_{12} = \frac{I_1}{V_3} \text{ when } V_1 = 0 \]

The equations (1) and (2) are now:
(1) \( I_{20} = -\frac{A_{11}}{A_{12}} \times V_{20} \)
(2) \( I_1 = A_{21} \times V_{20} + A_{22} \times (-I_{20}) \)

\[ (2) \Leftrightarrow I_1 = A_{21} \times V_{20} + A_{22} \times (-\frac{A_{11}}{A_{12}}) \times V_{20} \]
\[ \Leftrightarrow I_1 = -\frac{A_{DET}}{A_{12}} \times V_{20} \]

The impedance seen at the secondary side of the transformer when a short circuit is at the primary side is (*):

\[ Z_{OUT} = \frac{A_{12}}{A_{11}} \]
\[ V_{20} / Z_{OUT} = V_3 / (Z_0 + Z_{OUT}) \] (voltage divider)

then from (3) and (4):
\[ V_{20} = V_3 \times \frac{A_{12}}{A_{12} + A_{11} \times Z_0} \]
and with (2):
\[ M_{12} = \frac{I_1}{V_3} = -\frac{A_{DET}}{A_{12} + A_{11} \times Z_0} \]
C. Calculation of M21 Matrix Parameter

\[ M_{21} = \frac{V_2}{V_1} \text{ when } V_3 = 0 \]

The relation between \( V_2 \) and \( I_2 \) is: \( V_{20} = -Z_0 \times I_2 \)

Then by replacing this in (2), we obtain:

\[ -\frac{V_{20}}{Z_0} = (-\frac{1}{A_{12}}) \times V_1 + (\frac{A_{11}}{A_{12}}) \times V_{20} \]

which is equivalent to:

\[ \frac{V_{20}}{V_1} = Z_0 / (A_{11} \times Z_0 + A_{12}) \]

\[ V_2 = V_{20} \text{ therefore:} \]

\[ M_{21} = Z_0 / (A_{12} + A_{11} \times Z_0) \]

D. Calculation of M22 Matrix Parameter:

\[ M_{22} = \frac{V_2}{V_3} \text{ when } V_1 = 0 \]

The calculations are then straightforward:

\[ \frac{V_2}{V_3} = \left( \frac{Z_{eq}}{Z_{eq} + Z_0} \right) \]

\( Z_{eq} \) is the impedance seen at the secondary side of the transformer when there is a short circuit at the primary. (*)

\[ Z_{eq} = \frac{A_{12}}{A_{11}} \]

Then:

\[ M_{22} = \frac{V_2}{V_3} = 1 / (1 + Z_0 \times (A_{11}/A_{12})) \]

4.5.2 K-Parameters

These parameters are easier to measure than the M-parameters but the calculations necessitate the knowledge of the generator impedance \( Z_g \) and of the generator voltage \( V_g \).

The SLIC is described by the following two equations:

\[ b_1 = K_{11} \times a_1 + K_{12} \times V_3 \]

\[ V_2 = K_{21} \times a_1 + K_{22} \times V_3 \]

with \( a_1 = V_1 - Z_g \times I_1 \)

\[ b_1 = V_1 + Z_g \times I_1 \]

and (4) \( V_1 = V_0 - Z_g \times I_1 \)
A. Calculation of K11 Matrix Parameter

K11 = b1/a1 when \( V_3 = 0 \)

\[
K11 = \frac{(Z_{IN} - Z_0)}{(Z_{IN} + Z_0)}
\]

with \( Z_{IN} \): admittance seen at the primary side of the transformer when the impedance \( Z_0 \) is at the secondary.\(^(*)\)

\[
Z_{IN} = \frac{(A11 \times Z_0 + A12)}{(A12 \times Z_0 + A22)}
\]

**Note:** The return loss (RL) is defined by:

\[
RL = -20 \times \log_{10}\left( \left| \frac{Z_{IN} + Z_g}{Z_{IN} - Z_g} \right| \right)
\]

that is:

\[
RL = 20 \times \log_{10}(\left|K11\right|)
\]

B. Calculation of K12 Matrix Parameter

K12 = 2 \times \frac{V_1}{V_3} \text{ when } a_1 = 0

The equations (1) and (2) are now:

1. \( V_1 = A11 \times V_2 + A12 \times (-I_2) \)
2. \( I_1 = A21 \times V_2 + A22 \times (-I_2) \)
3. \( V_3 = V_2 + Z_0 \times I_2 \)
4. \( V_1 = -Z_g \times I_1 \)

(3) \( \Leftrightarrow V_2 = V_3 - Z_0 \times I_2 \)

by reporting in (1) and (2):

5. \( V_1 = A11 \times (V_3 - Z_0 \times I_2) - A12 \times I_2 \)
6. \( I_1 = A21 \times (V_3 - Z_0 \times I_2) - A22 \times I_2 \)

by combination of (4), (5) and (6):

\[
V_1/V_3 = \frac{(A22 + A11 \times Z_0) + (1/Z_0) \times (A12 + A11 \times Z_0)}{A11(A22 + A21 \times Z_0) - A21 \times (A12 + A11 \times Z_0)}
\]

then

\[
V_1/V_3 = \frac{2 \times ADET \times Z_0}{Z_0 \times (A22 + A21 \times Z_0) + (A12 + A11 \times Z_0)}
\]
C. Calculation of K21 Matrix Parameter

K21 = $V_2 / V_g$ when $V_3 = 0$

The equations are now:

\[
\begin{align*}
V_2 &= V_{20} \\
I_2 &= I_{20} \\
V_{20} &= -Z_0 \times I_{20} \\
(1) \quad V_1 &= A_{11} \times V_{20} - A_{12} \times I_{20} \\
(2) \quad I_1 &= A_{21} \times V_{20} - A_{22} \times I_{20} \\
(4) \quad V_g - V_1 &= Z_g \times I_1
\end{align*}
\]

the relation between $V_2$ and $I_2$ is:

\[
V_{20} = -Z_0 \times I_{20}
\]

replacing (4) in (1) and (2):

\[
\begin{align*}
(1) \quad V_g - Z_g \times I_1 &= A_{11} \times V_{20} - A_{12} \times I_{20} \\
(2) \quad I_1 &= A_{21} \times V_{20} - A_{22} \times I_{20}
\end{align*}
\]

by combination:

\[
V_g = (A_{11} + Z_g \times A_{21}) \times V_{20} + (A_{12} + A_{22} \times Z_g) \times (-I_{20})
\]

and by replacing $I_{20}$:

\[
\frac{V_2}{V_g} = \frac{Z_0}{(A_{11} + A_{21} \times Z_g) \times Z_0 + A_{12} + Z_g \times A_{22}}
\]

D. Calculation of K22 Matrix Parameter

K22 = $V_2/V_3$ when $a1 = 0$

The equations are now:

\[
\begin{align*}
V_2 &= V_{20} \\
I_2 &= I_{20} \\
V_{20} &= -Z_0 \times I_{20} \\
(1) \quad V_1 &= A_{11} \times V_{20} - A_{12} \times I_{20} \\
(2) \quad I_1 &= A_{21} \times V_{20} - A_{22} \times I_{20} \\
(4) \quad V_g - V_1 &= Z_g \times I_1
\end{align*}
\]

The calculations are then straightforward:

\[
\frac{V_2}{V_3} = \frac{Z_{eq}}{(Z_{eq} + Z_0)}
\]
$Z_{eq}$ is the impedance seen at the secondary side of the transformer when there is a short circuit at the primary.(*)

$Z_{eq} = (A22 \times Z_g + A12) / (A11 + A21 \times Z_g)$

Then:

$$K22 = \frac{V_2}{V_3} = \frac{(A22 \times Z_g + A12)}{(A22 \times Z_g + A12) + Z_0 \times (A11 + Z_g \times A21)}$$

Summary:

$$M11 = \frac{(A21 \times Z_0 + A22)}{(A11 \times Z_0 + A12)}$$

$$M12 = -\frac{ADET}{(A12 + A11 \times Z_0)}$$

$$M21 = \frac{Z_0}{(A12 + A11 \times Z_0)}$$

$$M22 = \frac{A12}{(A12 + Z_0 \times A11)}$$

$$K11 = \frac{(Z_{IN} - Z_g)}{(Z_{IN} + Z_g)}$$

with $Z_{IN} = (A21 \times Z_0 + A22) / (A11 \times Z_0 + A12)$

$$K12 = \frac{2 \times ADET \times Z_0}{Z_g \times (A22 + A21 \times Z_0) + (A12 + A11 \times Z_0)}$$

$$K21 = \frac{Z_0}{(A11 + A21 \times Z_g) \times Z_0 + A12 + Z_g \times A22}$$

$$K22 = \frac{(A22 \times Z_g + A12)}{(A22 \times Z_g + A12) + Z_0 \times (A11 + Z_g \times A21)}$$
Schematic circuit diagram of transformer SLIC software:

**Note:** Each block is modifyable by the user.

**Impedances**

The matching impedance $Z_0$ and the generator impedance are modeled with 6 parameters:

Example:

- $Z_{0,R1}, Z_{0,C1}, Z_{0,R2}, Z_{0,C2}$: parallel part
- $Z_{0,R}, Z_{0,C}$: serial part

---

**Figure 8**

**Figure 9**
5 Optimization

5.1 Input Data

The TRAFOT SLIC program (written with Microsoft FORTRAN compiler) needs an input file which contains the data for the SLIC:

TRAFOT.INP:

* PARAmeter (K[default] or M)
K
RCU1    *RCU2 :copper resistor of primary (resp. secondary)
  84.     105.
*CW1,    *CW2 :winding capacitors primary and secondary
  1.135E-10  135.4E-12
*LS1    *LS2    *M :leaking inductances primary and secondary
  1.15    1.15    1.148
*CSP :blocking capacitor
  1.E-6
*RF    *LF     *CF :feeding ( cannot be all 0 at the same time)
  792.    2.23    2.67E-9
*ZSLI :worst case half loop
  0.5
*Z0 : matching impedance (with 6 elements)
ZR0A1, Z0CA1, Z0CA2, Z0RA2, Z0RS, Z0CS
  700.  .1E-6  0.  0.  0.
*Zg : source/line impedance (with 6 elements)
ZgRA1, ZgCA1, ZgCA2, ZgRA2, ZgRS, ZgCS
  820.  0.  115.E-09  0.  220.  0.

5.2 Runs

Specifications:

The .SPE file needed by the SICOFI coefficient program makes use of values based on the specifications for West-Germany (see BRD.SPE in appendix A1). A first run with automatical Z-filter optimization (PZIN=0) does not give satisfying results for the return loss.

A second run with modified specifications (see BRD2.SPE in appendix A1) is necessary with repetition of the Z-filter optimization (ZREP=Y).

Result file:

The corresponding result file TRAFOT.RES can be found in appendix A3.
6 Measurements
Measurements are made with a "PCM4" from Wandel & Goltermann. The specifications for West-Germany are fulfilled.

We have measured the return loss, the (attenuation in) transmit direction (AD), the attenuation in the receive direction (DA), the attenuation distortion (AD and DA) and the transhybrid loss (DD).

Correlation
The correlation between the calculated values and the measured values for return loss (all filters off and calculated values with the "Sim"-function of the SICOFI program) can be seen in the last diagram of appendix A2. The lower line in the picture stands for the calculated values.

7 Strategies
The SICOFI makes it possible to use the same hardware for different country specifications by changing the programming of the SICOFI.

In general, it is necessary to already have a good return loss with the transformer alone without SICOFI. Then SICOFI improves the figures.

This requires us however to optimize the SLIC circuitry in four steps using the SICOFI program as an simulation tool (especially Z-filter optimization):

1. Set $Z_0$ to a given value
2. Run automatical Z-filter optimization for the given $Z_0$ impedance and for all the specifications.
3. Change the impedance $Z_0$
4. Redo step 1 until having obtained an optimal return loss.
## Appendix A1

### Specifications

#### BRD.SPE

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#### ZIN

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**ZIN**

| FR | 300 | 500 | 3K | 3.4k |
| AT- | 0 | 20 | 20 | 20 |
| AT+ | 16 | 20 | 20 | 0 |

**ZMIR**

| FR | 4k | 12k |
| AT- | 30 | 3 |
| AT+ | 30 | 3 |

**DA, UPPER**

| FR | 300 | 500 | 2.7k | 3k | 3.4k |
| AT- | 100 | .75 | .25 | .35 | .75 |
| AT+ | .75 | .25 | .35 | .75 | 100 |

**DA, LOWER**

| FR | 300 | 3.4k |
| AT- | 0 | -.25 |
| AT+ | -.25 | 0 |

**DA, DELAY**

| FR | 500 | 600 | 1k | 2.6k | 2.8k |
| GD- | 10k | .420 | .150 | .085 | .150 |
| GD+ | .420 | .150 | .085 | .150 | 10k |

**AD, UPPER**

| FR | 300 | 500 | 2.7k | 3k | 3.4k |
| AT- | 100 | .75 | .25 | .35 | .75 |
| AT+ | .75 | .25 | .35 | .75 | 100 |

**AD, LOWER**

| FR | 300 | 3.4k |
| AT- | 0 | -.25 |
| AT+ | -.25 | 0 |

**AD, DELAY**

| FR | 500 | 600 | 1k | 2.6k | 2.8k |
| GD- | 10k | .420 | .150 | .085 | .150 |
| GD+ | .420 | .150 | .085 | .150 | 10k |

**DD**

| FR | 300 | 500 | 2.5k | 3.4k |
| AT- | 0 | 29 | 29 | 23 |
| AT+ | 23 | 29 | 29 | 0 |
Appendix A2
Measurements

Note: The masks on the plots corresponds to CCITT Recommendations G.712 and G.714
Figure 10

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Figure 11

| MODUS A11 PEGELMESSG. SE: +0.0 EM: -- dBm0 | 200Hz | 1000Hz | 2000Hz | 3000Hz | 3600Hz | 2208 | -0.01 | 2309 | -0.02 | 2409 | -0.04 | 2509 | -0.08 | 2610 | -0.13 | 2710 | -0.16 | 2811 | -0.18 | 2911 | -0.19 | 3011 | -0.20 | 3112 | -0.21 | 3212 | -0.24 | 3312 | -0.28 | 3413 | -0.36 | 3513 | -0.58 | 3614 | -0.60 | 3715 | -0.62 | 3816 | -0.64 | 3917 | -0.66 | 4018 | -0.68 | 4119 | -0.70 | 4220 | -0.72 | 4321 | -0.74 | 4422 | -0.76 | 4523 | -0.78 | 4624 | -0.80 | 4725 | -0.82 | 4826 | -0.84 | 4927 | -0.86 | 5028 | -0.88 | 5129 | -0.90 | 5230 | -0.92 | 5331 | -0.94 | 5432 | -0.96 | 5533 | -0.98 | 5634 | -1.00 | 5735 | -1.02 | 5836 | -1.04 | 5937 | -1.06 | 6038 | -1.08 | 6139 | -1.10 | 6240 | -1.12 | 6341 | -1.14 | 6442 | -1.16 | 6543 | -1.18 | 6644 | -1.20 | 6745 | -1.22 | 6846 | -1.24 | 6947 | -1.26 | 7048 | -1.28 | 7149 | -1.30 | 7250 | -1.32 | 7351 | -1.34 | 7452 | -1.36 | 7553 | -1.38 | 7654 | -1.40 | 7755 | -1.42 | 7856 | -1.44 | 7957 | -1.46 | 8058 | -1.48 | 8159 | -1.50 | 8260 | -1.52 | 8361 | -1.54 | 8462 | -1.56 | 8563 | -1.58 | 8664 | -1.60 | 8765 | -1.62 | 8866 | -1.64 | 8967 | -1.66 | 9068 | -1.68 | 9169 | -1.70 | 9270 | -1.72 | 9371 | -1.74 | 9472 | -1.76 | 9573 | -1.78 | 9674 | -1.80 | 9775 | -1.82 | 9876 | -1.84 | 9977 | -1.86 | 10078 | -1.88 | 10179 | -1.90 | 10280 | -1.92 | 10381 | -1.94 | 10482 | -1.96 | 10583 | -1.98 | 10684 | -2.00 | 10785 | -2.02 | 10886 | -2.04 | 10987 | -2.06 | 11088 | -2.08 | 11189 | -2.10 | 11290 | -2.12 | 11391 | -2.14 | 11492 | -2.16 | 11593 | -2.18 | 11694 | -2.20 | 11795 | -2.22 | 11896 | -2.24 | 11997 | -2.26 | 12098 | -2.28 | 12199 | -2.30 | 122100 | -2.32 | 123101 | -2.34 | 124102 | -2.36 | 125103 | -2.38 | 126104 | -2.40 | 127105 | -2.42 | 128106 | -2.44 | 129107 | -2.46 | 130108 | -2.48 | 131109 | -2.50 | 132110 | -2.52 | 133111 | -2.54 | 134112 | -2.56 | 135113 | -2.58 | 136114 | -2.60 | 137115 | -2.62 | 138116 | -2.64 | 139117 | -2.66 | 140118 | -2.68 | 141119 | -2.70 | 142120 | -2.72 | 143121 | -2.74 | 144122 | -2.76 | 145123 | -2.78 | 146124 | -2.80 | 147125 | -2.82 | 148126 | -2.84 | 149127 | -2.86 | 150128 | -2.88 | 151129 | -2.90 | 152130 | -2.92 | 153131 | -2.94 | 154132 | -2.96 | 155133 | -2.98 | 156134 | -3.00 | 157135 | -3.02 | 158136 | -3.04 | 159137 | -3.06 | 160138 | -3.08 | 161139 | -3.10 | 162140 | -3.12 | 163141 | -3.14 | 164142 | -3.16 | 165143 | -3.18 | 166144 | -3.20 | 167145 | -3.22 | 168146 | -3.24 | 169147 | -3.26 | 170148 | -3.28 | 171149 | -3.30 | 172150 | -3.32 | 173151 | -3.34 | 174152 | -3.36 | 175153 | -3.38 | 176154 | -3.40 | 177155 | -3.42 | 178156 | -3.44 | 179157 | -3.46 | 180158 | -3.48 | 181159 | -3.50 | 182160 | -3.52 | 183161 | -3.54 | 184162 | -3.56 | 185163 | -3.58 | 186164 | -3.60 | 187165 | -3.62 | 188166 | -3.64 | 189167 | -3.66 | 190168 | -3.68 | 191169 | -3.70 | 192170 | -3.72 | 193171 | -3.74 | 194172 | -3.76 | 195173 | -3.78 | 196174 | -3.80 | 197175 | -3.82 | 198176 | -3.84 | 199177 | -3.86 | 200178 | -3.88 | 201179 | -3.90 | 202180 | -3.92 | 203181 | -3.94 | 204182 | -3.96 | 205183 | -3.98 | 206184 | -4.00 |
### Figure 12

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Figure 16 Correlation (all filters OFF)

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</table>
Appendixes A3

Result File  TRAFOT.RES

Input_file_name: TRAFOT.CTL          Date:  11.08.88  13:35
SPEC = BRD2.SPE            SLIC = TRAFOT.SLI
BYTE = REF.BYT     CHNR = 0,A
PLQ = N

ON = ALL             REL = Y          SHORT = N
OPT = Z+X+R+B             ZXRB = NNNN
PZIN= 0            PSP = 0
FZ =  300.00        3400.0       ZLIM =  2.00
ZREP =Y              ZSIGN =  1
FR =  300.00        3400.0
RFIL = Y             RREFQ = N       RREF =  .66179
FX =  300.00        3400.0
XFIL = Y             XREFO = N       XREF = -.13731
FB =  300.00        3400.0       BLIM =  2.00  TBM =  1
BREP = N             BSIGN =  1
APOF = .00          DPOF = .00      APRE = .00      DPRE = .00
XZQ = -.10888671875000000E+00   .28906250000000000E+00
   .63476562500000000E-02   -.30468750000000000E+00
  .19531250000000000E+00       
XRQ = .96777343750000000E+00   -.48828125000000000E-01
   -.14526367187500000E-01   -.48828125000000000E-03
  .90332031250000000E-02       
XXQ = .10175781250000000E+01   .15075683593750000E-01
   .11474609375000000E-01   .34179687500000000E-02
  .97351074218750000E-02       
XBQ = .21093750000000000E+00   .34375000000000000E+00
   .25415039062500000E+00   -.12158203125000000E+00
  -.95703125000000000E-01      
XGQ = .534912109375000000E+00   .21171875000000000E+01
;

Bytes for Z-Filter (13):  20,BA,2A,7B,1B,32,B2,5B
Bytes for R-Filter (2B):   70,23,8F,EC,3C,AC,OB,5D
Bytes for X-Filter (23):    70,E2,97,73,C1,D6,03,36
Bytes for Gain-factors (30):  41,C3,00,C3
2nd part of bytes B-Filter (0B):  00,2C,31,C1,AA,6F,33,23
1st part of bytes B-Filter (03):  BB,CA,DB,2B,46,22,21,2B
Bytes for B-filter delay (18):  19,19,11,19
* TRAFO SLIC
* PARAMETER : M
*Z0R1=  700.0     *Z0C1=  .0000     *Z0R2=  .0000     *Z0C2= .1000E-06
*Z0RS=  .0000     *Z0CS=  .0000
*RCU1=  84.00     *RCU2= 105.0     *CW1 =  .1135E-09  *CW2 = .1354E-09
*L1 =  1.150     * L2 =  1.150     * M =   1.148
*CSP =  .1000E-05
* RF =  792.0     * LF =  2.230     * CF =  .2670E-08
*ZSLI = 0.500

Run #  1

Z-FILTER calculation results

Reference impedance for optimization (ZI):
ERZI = 1  RSER =  220.  CSER =  0.00  RPAR =  820.  CPAR =  0.115E-0

Calculated and quantized coefficients:
XZ  =    -.10895    .28881    .00646   -.30563    .19882
XZQ =    -.10889    .28906    .00635   -.30469    .19531
Bytes for Z-Filter (13):  20,BA,2A,7B,1B,32,B2,5B

RETURN LOSS

<table>
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<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>1800.</td>
<td>32.679</td>
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<tr>
<td>200.</td>
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<td>2100.</td>
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<td>2200.</td>
<td>32.712</td>
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<td>31.454</td>
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<td>32.901</td>
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<tr>
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<td>32.608</td>
<td>3400.</td>
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</table>
Min. Z-loop reserve: 5.721 dB
at frequency: 8500.0 Hz
Min. Z-loop mirror signal reserve: 10.365 dB
at frequency: 9000.0 Hz

Run # 1

X-FILTER calculation results
Calculated and quantized coefficients:

XX = 1.01799  .01508  .01135  .00340  .00974
XXQ = 1.01758  .01508  .01147  .00342  .00974

Bytes for X-Filter (23): 70,E2,97,73,C1,D6,03,36

X-filter attenuation function (in dB), (always absolute values)

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
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<tbody>
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<tr>
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GX results:
All attenuation values (in dB) refer to FREF = 1014. Hz

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<th>VREF/VSIDOFI</th>
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Second byte for Gain: ,00,C3

Calculation of transmit transfer function (AD)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

Reference impedance for optimization (ZI):
ERZI = 1 RSER = 220. CSER = .000 RPAR = 820. CPAR = .115E-0
TGREF CA = .305 ms    TGREF CB = .318 ms

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<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
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<th>GD (msec)</th>
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Run # 1

R-FILTER calculation results
Calculated and quantized coefficients:

XR =  .96755  -.04884  -.01447  -.00040  .00910
XRQ =  .96777  -.04883  -.01453  -.00049  .00903
Bytes for R-Filter (2B):  70,23,8F,EC,3C,AC,0B,5D

R-filter attenuation function (in dB), (always absolute values)

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>.008</td>
</tr>
<tr>
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<td>.798</td>
<td>-.008</td>
<td>2000.</td>
<td>.065</td>
<td>.009</td>
</tr>
<tr>
<td>500.</td>
<td>.796</td>
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<td>.040</td>
<td>.009</td>
</tr>
<tr>
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<td>.788</td>
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<td>2200.</td>
<td>.026</td>
<td>.008</td>
</tr>
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<td>.020</td>
<td>.007</td>
</tr>
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<td>.749</td>
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<tr>
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<td>2700.</td>
<td>.050</td>
<td>.002</td>
</tr>
<tr>
<td>1200.</td>
<td>.551</td>
<td>-.005</td>
<td>2800.</td>
<td>.057</td>
<td>.001</td>
</tr>
<tr>
<td>1300.</td>
<td>.482</td>
<td>-.003</td>
<td>2900.</td>
<td>.061</td>
<td>.000</td>
</tr>
<tr>
<td>1400.</td>
<td>.409</td>
<td>-.001</td>
<td>3000.</td>
<td>.060</td>
<td>.000</td>
</tr>
<tr>
<td>1500.</td>
<td>.337</td>
<td>.001</td>
<td>3100.</td>
<td>.052</td>
<td>.000</td>
</tr>
<tr>
<td>1600.</td>
<td>.267</td>
<td>.004</td>
<td>3200.</td>
<td>.039</td>
<td>.000</td>
</tr>
<tr>
<td>1700.</td>
<td>.203</td>
<td>.005</td>
<td>3300.</td>
<td>.020</td>
<td>.001</td>
</tr>
<tr>
<td>1800.</td>
<td>.147</td>
<td>.007</td>
<td>3400.</td>
<td>-.002</td>
<td>.002</td>
</tr>
<tr>
<td>1900.</td>
<td>.101</td>
<td>.008</td>
<td>3500.</td>
<td>-.007</td>
<td>.000</td>
</tr>
<tr>
<td>2000.</td>
<td>.065</td>
<td>.009</td>
<td>3600.</td>
<td>-.008</td>
<td>.000</td>
</tr>
</tbody>
</table>

GR results:
All attenuation values (in dB) refer to FREF = 1014 Hz
-RLR     SLIC+Z     VSICOFI/VREF     RREF     GR
7.00     5.32     -4.42     -.66     =     5.44     ideal
7.00     5.32     +4.42     +.66     +     5.43     quant

First byte for Gain (30): 41,C3

Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

Reference impedance for optimization (ZI):
ERZI = 1 RSER = 220. CSER = .000 RPAR = 820. CPAR = .115E-0
TGREF CA = .262 ms TGREF CB = .244 ms

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>3.702</td>
<td>2.741</td>
</tr>
<tr>
<td>200.</td>
<td>.355</td>
<td>.717</td>
</tr>
<tr>
<td>300.</td>
<td>.008</td>
<td>.300</td>
</tr>
<tr>
<td>400.</td>
<td>-.086</td>
<td>.159</td>
</tr>
<tr>
<td>500.</td>
<td>-.105</td>
<td>.093</td>
</tr>
<tr>
<td>600.</td>
<td>-.094</td>
<td>.056</td>
</tr>
<tr>
<td>700.</td>
<td>-.070</td>
<td>.034</td>
</tr>
<tr>
<td>800.</td>
<td>-.044</td>
<td>.019</td>
</tr>
<tr>
<td>900.</td>
<td>-.021</td>
<td>.010</td>
</tr>
<tr>
<td>1000.</td>
<td>-.004</td>
<td>.004</td>
</tr>
<tr>
<td>1100.</td>
<td>.004</td>
<td>.001</td>
</tr>
<tr>
<td>1200.</td>
<td>.004</td>
<td>.000</td>
</tr>
<tr>
<td>1300.</td>
<td>-.004</td>
<td>.000</td>
</tr>
<tr>
<td>1400.</td>
<td>-.017</td>
<td>.002</td>
</tr>
<tr>
<td>1500.</td>
<td>-.035</td>
<td>.005</td>
</tr>
<tr>
<td>1600.</td>
<td>-.054</td>
<td>.008</td>
</tr>
<tr>
<td>1700.</td>
<td>-.072</td>
<td>.012</td>
</tr>
<tr>
<td>1800.</td>
<td>-.088</td>
<td>.016</td>
</tr>
<tr>
<td>1900.</td>
<td>-.099</td>
<td>.020</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>GD (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000.</td>
<td>-.105</td>
<td>.025</td>
</tr>
<tr>
<td>2100.</td>
<td>-.099</td>
<td>.037</td>
</tr>
<tr>
<td>2200.</td>
<td>-.089</td>
<td>.043</td>
</tr>
<tr>
<td>2300.</td>
<td>-.075</td>
<td>.051</td>
</tr>
<tr>
<td>2400.</td>
<td>-.075</td>
<td>.051</td>
</tr>
<tr>
<td>2500.</td>
<td>-.059</td>
<td>.059</td>
</tr>
<tr>
<td>2600.</td>
<td>-.043</td>
<td>.069</td>
</tr>
<tr>
<td>2700.</td>
<td>-.028</td>
<td>.082</td>
</tr>
<tr>
<td>2800.</td>
<td>-.014</td>
<td>.097</td>
</tr>
<tr>
<td>2900.</td>
<td>-.003</td>
<td>.115</td>
</tr>
<tr>
<td>3000.</td>
<td>.008</td>
<td>.137</td>
</tr>
<tr>
<td>3100.</td>
<td>.021</td>
<td>.164</td>
</tr>
<tr>
<td>3200.</td>
<td>.043</td>
<td>.199</td>
</tr>
<tr>
<td>3300.</td>
<td>.083</td>
<td>.243</td>
</tr>
<tr>
<td>3400.</td>
<td>.158</td>
<td>.302</td>
</tr>
<tr>
<td>3500.</td>
<td>.300</td>
<td>.384</td>
</tr>
<tr>
<td>3600.</td>
<td>.577</td>
<td>.506</td>
</tr>
<tr>
<td>3700.</td>
<td>1.166</td>
<td>.703</td>
</tr>
<tr>
<td>3800.</td>
<td>2.625</td>
<td>1.041</td>
</tr>
</tbody>
</table>

Run # 1
B-FILTER calculation results

Reference impedance for optimization (ZL):
ERZL = 1 RSL = 220. CSL = .000 RPL = 820. CPL = .115E-0

Calculated and quantized coefficients:

\[
XB = \begin{bmatrix}
0.20818 \\
0.15308 \\
0.21094 \\
0.15234
\end{bmatrix},
XBQ = \begin{bmatrix}
0.34529 \\
0.01798 \\
0.34375 \\
0.01782
\end{bmatrix},
XB = \begin{bmatrix}
0.25405 \\
-0.12179 \\
0.25415 \\
-0.12158
\end{bmatrix},
XBQ = \begin{bmatrix}
-0.09620 \\
0.18355 \\
-0.09570 \\
0.18359
\end{bmatrix}
\]

2nd part of bytes B-Filter (0B): 00,2C,31,C1,AA,6F,33,23
1st part of bytes B-Filter (03): BB,CA,DB,2B,46,22,21,2B

TRANS HYBRID LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>22.979</td>
<td>1800.</td>
<td>38.757</td>
</tr>
<tr>
<td>200.</td>
<td>21.665</td>
<td>1900.</td>
<td>36.141</td>
</tr>
<tr>
<td>300.</td>
<td>26.651</td>
<td>2000.</td>
<td>34.677</td>
</tr>
<tr>
<td>400.</td>
<td>32.370</td>
<td>2100.</td>
<td>34.020</td>
</tr>
<tr>
<td>500.</td>
<td>42.075</td>
<td>2200.</td>
<td>34.049</td>
</tr>
<tr>
<td>600.</td>
<td>47.207</td>
<td>2300.</td>
<td>34.748</td>
</tr>
<tr>
<td>700.</td>
<td>37.954</td>
<td>2400.</td>
<td>36.166</td>
</tr>
<tr>
<td>800.</td>
<td>34.818</td>
<td>2500.</td>
<td>38.311</td>
</tr>
<tr>
<td>900.</td>
<td>33.479</td>
<td>2600.</td>
<td>40.525</td>
</tr>
<tr>
<td>1000.</td>
<td>33.128</td>
<td>2700.</td>
<td>40.436</td>
</tr>
<tr>
<td>1100.</td>
<td>33.521</td>
<td>2800.</td>
<td>37.955</td>
</tr>
<tr>
<td>1200.</td>
<td>34.636</td>
<td>2900.</td>
<td>35.622</td>
</tr>
<tr>
<td>1300.</td>
<td>36.631</td>
<td>3000.</td>
<td>34.139</td>
</tr>
<tr>
<td>1400.</td>
<td>40.013</td>
<td>3100.</td>
<td>33.619</td>
</tr>
<tr>
<td>1500.</td>
<td>46.646</td>
<td>3200.</td>
<td>34.277</td>
</tr>
<tr>
<td>1600.</td>
<td>57.076</td>
<td>3300.</td>
<td>36.848</td>
</tr>
<tr>
<td>1700.</td>
<td>43.595</td>
<td>3400.</td>
<td>44.261</td>
</tr>
</tbody>
</table>

Additional B-filter delay (in seconds): .625E-04
Bytes for B-filter delay (18): 19,19,11,19
Appendix A4
Listing of FORTRAN SLIC Program

C#$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$C
C###
C### PROGRAM TRAFOT
C###
C### Version  V3.1  Mr. Glasser  Jan 1989
C### Revision V3.2  Mr. Kliese  Feb 1989
C### Revision V3.3  Subroutine IMPED6
C###                   Mr. Kliese     Aug 1989
C###
C### Copyright 1989 Siemens AG Munich, West Germany
C### Mr Kliese tel (089) 4144-3662
C###
C### The following program calculates the M- or K-
C### parameters of a transformer slic.
C### It uses complex calculations and A-parameters matrixes.
C### The data to be hold during the execution are stored
C### in 'COMMON fields', which names begin by 'Q'.
C### The transformer is calculated in the subroutine
C### TRSLIC and its feeding in the subroutine ZFEED.
C### Complex matrix multiplication is made by the
C### subroutine CMATMUL.
C###
C### Note: FORTRAN requires at least 7 spaces at the
C### beginning of a line ; a sign (e.g.'&')in the 6th
C### place means that the line continues underneath.
C### '*'or 'c' are comments.
C###
C###*$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$C
*
**********************************************************************
*        Declaration of Variables                              *
**********************************************************************
* implicit variables beginning with A,B,...K and
* M...Z are declared as logical; variables beginning
* with L are declared as character : if a variable
* has not been declared the compiler will give a warning.
*
* IMPLICIT LOGICAL (A-K,M-Z),CHARACTER (L)
*
* INTEGER IN,OUT,I,ERZ0
*
* CHARACTER*1 PARA
* CHARACTER*12 FILEOUT,INFILE,B1,B2,B3,B4
*
* REAL CSP,CW1,M,L1,L2,RCU1,RCU2,RF,LF,CF,CW2
* REAL P12,R5,R6,R7,C5,R4,R3,C3,ZSLI,FREQ
REAL Z0R1, Z0R2, Z0C1, Z0C2, Z0RS, Z0CS
REAL ZgR1, ZgR2, ZgC1, ZgC2, ZgRS, ZgCS
COMPLEX Z0, A, B, A11, A12, A21, A22, ADET, AR, AX, ZIN, Zg, DEN
COMPLEX M11TAB(399), M12TAB(399), M21TAB(399), M22TAB(399)
COMPLEX M11, M12, M21, M22
COMPLEX K11TAB(399), K12TAB(399), K21TAB(399), K22TAB(399)
COMPLEX K11, K12, K21, K22
LOGICAL LINFIL

* data storage for 2*Pi
COMMON /QPI2/ PI2
* data storage for PARAmeter
COMMON /QPARA/ PARA
* data storage for matching impedance Z0
COMMON /QZ0/ Z0R1, Z0R2, Z0C1, Z0C2, Z0RS, Z0CS
* data storage for line/source impedance Zg
COMMON /QZg/ ZgR1, ZgR2, ZgC1, ZgC2, ZgRS, ZgCS
* data storage for transformer
COMMON /QTR/ RCU1, RCU2, CW1, L1, CW2, RF, LF, CF, CSP, L2, M
* data storage for M-parameters tables (containing 399 values each)
COMMON /QM/ M11TAB, M12TAB, M21TAB, M22TAB

*****************************************************************
*        Program Begins:                                        *
*****************************************************************

* screen
OUT = 6
* keyboard
IN = 5
* 2*pi calculation
PI2 = 4.* ASIN(1.)
* reading file names
FILEOUT = '
INFILE = '
WRITE(OUT,'(A)') 'TRAFOT SLIC Program Version V3.3
Siemens AG Munich, Aug. 1989'
WRITE(OUT,'(A)') & Enter input file name(xxxxxxxxx.INP):
10   READ (IN,'(A)') INFILE
INQUIRE (FILE = INFILE,EXIST = LINFIL)
   IF (INDEX(INFILE,'').EQ.1.OR.(.NOT.LINFIL)
      .OR.(INDEX(INFILE,'.INP').EQ.0
      .AND.INDEX(INFILE,'.inp').EQ.0))THEN
      WRITE (OUT,'(A)')'Enter correct input file name:'
      INFILE='
      GOTO 10
ENDIF
* Reading input file
* note: every second line is read
OPEN (10, FILE=INFILE, ERR=1100, STATUS='OLD')
WRITE(6,*) 'Reading input file'
READ(10,'(A)')
READ(10,'(A)') PARA
READ(10,'(A)')
READ(10,*) RCU1,RCU2
READ(10,'(A)')
READ(10,*) CW1,CW2
READ(10,'(A)')
READ(10,*) L1,L2,M
READ(10,'(A)')
READ(10,*) CSP
READ(10,'(A)')
READ(10,*) RF,LF,CF
READ(10,'(A)')
READ(10,*) ZSLI
READ(10,'(A)')
READ(10,'(A)')
READ(10,*) Z0R1,Z0C1,Z0C2,Z0R2,Z0RS,Z0CS
READ(10,'(A)')
READ(10,'(A)')
READ(10,*) ZgR1,ZgC1,ZgC2,ZgR2,ZgRS,ZgCS
READ(10,'(A)')
CLOSE (10)

*    ***********************************************
C      Screen picture of TRAFOT SLIC
C     using ANSI.SYS driver
C    ***********************************************

WRITE (OUT,'(A)')'       ---------
&        |    +---------+
&      +---------|Vin |
&       |         |   |
&      |         |   |
WRITE (OUT,'(A)')' _ _ _ feeding _ _ _
&___ ___ | ___ |   |
WRITE (OUT,'(A)')' +--|++++--o--|++++--o--|++++--o--|++++--o--|++++--o--|
&___+++|++++--o--|+++---|Vout |' 
WRITE (OUT,'(A)')|Zg/2| CSP=|RCU1= L1-M | L
&Z0-M RCU2= | |Z0 |   |
WRITE (OUT,20) CSP, RCU1 RCU2
20 FORMAT (' O |!','G10.4,'| ',' ,G10.4,'|
& ',G10.4,' | | S |') 
WRITE (OUT,21) M
21 FORMAT (' | |+++ | --- |+++ M=
& ',G10.4,' | | |!')
WRITE (OUT,'(A)')' |+++ZSP | --- CW1= +++
& CW2= +++ | | C |'
WRITE (OUT,22) CW1, CW2
22 FORMAT (' O | |!','G10.4,' |
& ',G10.4,' | | | O!')
WRITE (OUT,'(A)')' ! | | |
& WRITE (OUT,'(A)')' +--|__+---o----------o-----------------o----
&------------------o |   | '.
WRITE (OUT,'(A)')' Zg/2 |   |
&        |
WRITE (OUT,'(A)')'   |_________|    <-receive
&        |   +---------+
WRITE (OUT,42) ZSLI
42 FORMAT('SLIC Loop Attenuation ZSLI=', G10.4)
WRITE (OUT,43) RF, LF, CF
43 FORMAT('Feeding ZSP:   RF=',G10.4,'   LF=',G10.4,
&   CF=',G10.4)
WRITE (OUT,44) L1, L2
44 FORMAT('Leaking inductance: L1=',G10.4,' L2=',G10.4)
WRITE(OUT,45)
45 FORMAT('Matching impedance: Z0R1  Z0C1  Z0C2  Z0R2
 & Z0RS  Z0CS')
WRITE(OUT,46) Z0R1, Z0C1, Z0C2, Z0R2, Z0RS, Z0CS
46 FORMAT('   ',G10.4, G10.4, G10.4,
 &   ', G10.4,',' ', G10.4,',' ,G10.4)
 & G10.4, G10.4, G10.4)
WRITE(OUT,47)
47 FORMAT('Source/line impedance: ZgR1  ZgC1  ZgC2  ZGR2
 & ZgRS  ZgCS')
WRITE(OUT,48) ZgR1, ZgC1, ZgC2, ZGR2, ZgRS, ZgCS
48 FORMAT('   ', G10.4, G10.4, G10.4,
 &   ', G10.4,',' ', G10.4,',' ,G10.4)
 & G10.4, G10.4, G10.4)
C****************************************************************************
WRITE(OUT,'(A)')' Enter output file name (xxxxxxxx.SLI):'
50 READ (IN,'(A)') FILEOUT
If (INDEX(FILEOUT,'').EQ.1
 & .OR.(INDEX(FILEOUT,'.SLI').EQ.0
 & .AND.INDEX(FILEOUT,'.sli').EQ.0)) THEN
 WRITE (OUT,'(A)')'
 & 'Enter correct output file name (with extention .SLI):'
 FILEOUT=''
GOTO 50
ENDIF
OPEN (30, FILE=FILEOUT, ERR=1000, STATUS='UNKNOWN')

WRITE (30,'(A)') '* TRAFO SLIC'
WRITE (30,'(A)') '* PARAMETER:/'//PARA
IF (PARA.NE.'M') THEN
  WRITE (B1,'(G11.4)') ZgR1
  WRITE (B2,'(G11.4)') ZgC1
  WRITE (B3,'(G11.4)') ZgR2
  WRITE (B4,'(G11.4)') ZgC2
  WRITE (30,'(A)') '*ZgR1='//B1//*ZgC1='//B2//
    '*ZgR2='//B3//*ZgC2='//B4
  WRITE (B2,'(G11.4)') ZgRS
  WRITE (B3,'(G11.4)') ZgCS
  WRITE (30,'(A)') '*ZgRS='//B2//*ZgCS='//B3
ENDIF
WRITE (B1,'(G11.4)') Z0R1
WRITE (B2,'(G11.4)') Z0C1
WRITE (B3,'(G11.4)') Z0R2
WRITE (B4,'(G11.4)') Z0C2
WRITE (30,'(A)') '* Z0R1='//B1//*Z0C1='//B2//
  '*Z0R2='//B3//*Z0C2='//B4
WRITE (B2,'(G11.4)') Z0RS
WRITE (B3,'(G11.4)') Z0CS
WRITE (30,'(A)') '* Z0RS='//B2//*Z0CS='//B3
WRITE (B1,'(G11.4)') RCU1
WRITE (B2,'(G11.4)') RCU2
WRITE (B3,'(G11.4)') CW1
WRITE (B4,'(G11.4)') CW2
WRITE (30,'(A)') '* RCU1='//B1//*RCU2='//B2//
  '*CW1='//B3//*CW2='//B4
WRITE (B1,'(G11.4)') L1
WRITE (B2,'(G11.4)') L2
WRITE (B3,'(G11.4)') M
WRITE (30,'(A)') '* L1='//B1//*L2='//B2//* M ='/B3
WRITE (B2,'(G11.4)') CSP
WRITE (30,'(A)') '* CSP ='/B2
WRITE (B1,'(G11.4)') RF
WRITE (B2,'(G11.4)') LF
WRITE (B3,'(G11.4)') CF
WRITE (30,'(A)') '* RF ='/B1//*LF ='/B2//* CF ='/B3
* ZSLI: worst case half loop
WRITE (B2,'(G11.4)') ZSLI
WRITE (30,'(A)')'*ZSLI='//B2
WRITE (30,'(A)')'ZSLI'
WRITE (30,'(G11.4)') ZSLI

******************************************************
*          Calculation Part                              *
******************************************************
* WRITE (OUT,*)'Running preliminary calculations...'*
DO 177 I=1,399
   FREQ = REAL(I*10)
* calculates for M parameters
   IF (PARA.EQ.'M') THEN
      * M11
         CALL ZOW(FREQ,Z0)
         CALL TRSLIC(FREQ,A11,A12,A21,A22,ADET)
         DEN = A11*Z0 + A12
         M11 = (A21*Z0+A22)/DEN
         C (A11*Z0+A12)
      * M12
         M12 = -ADET/DEN
         C (A12+A11*Z0)
      * M21
         M21 = Z0/DEN
         C (A12+Z0*A11)
      * M22
         M22 = A12/DEN
         C (A12+Z0*A11)
      * put the calculated values in the corresponding tables
         M11TAB(i)=M11
         M12TAB(i)=M12
         M21TAB(i)=M21
         M22TAB(i)=M22
   ELSE
      * calculates for K parameters
      * K11
         CALL ZOW(FREQ,Z0)
         CALL ZgW(FREQ,Zg)
         CALL TRSLIC(FREQ,A11,A12,A21,A22,ADET)
         ZIN = (A11*Z0+A12)/(A21*Z0+A22)
         K11 = (Zin-Zg)/(Zin+Zg)
         C (Zg*(A22+A21*Z0) + (A12+A11*Z0))
      * K12
         K12 = 2.*ADET*Zg/
         & (Zg*(A22+A21*Z0) + (A12+A11*Z0))
      * K21
         K21 = Z0/
         & (Z0*(A11+A21*Zg) + (A12+A22*Zg))
      * K22
         K22 = (A22*Zg+A12)/
         & (Z0*(A11+A21*Zg) + (A12+A22*Zg))
      C put the calculated values in the corresponding tables
         K11TAB(i)=K11
         K12TAB(i)=K12
         K21TAB(i)=K21
         K22TAB(i)=K22
   END
ENDIF
177  CONTINUE
*
IF (PARA.EQ.'M') THEN

* Writing the Mij values in the output file
write (30,'(A)')'M11-TABLE'
WRITE (OUT,'(A)')'+Running M11 calculation...
DO 100 I=1,399
  FREQ = REAL(I*10)
  WRITE (30,*) FREQ,REAL(M11TAB(i)),AIMAG(M11TAB(i))
100  CONTINUE
WRITE (30,'(A)')'M12-TABLE'
WRITE (OUT,'(A)')'+Running M11, M12 calculation...
DO 110 I=1,399
  FREQ = REAL(I*10)
  WRITE (30,*) FREQ,REAL(M12TAB(i)),AIMAG(M12TAB(i))
110  CONTINUE
WRITE (30,'(A)')'M21-TABLE'
WRITE (OUT,'(A)')'+Running M11, M12, M21 calculation...
DO 120 I=1,399
  FREQ = REAL(I*10)
  WRITE (30,*) FREQ,REAL(M21TAB(i)),AIMAG(M21TAB(i))
120  CONTINUE
WRITE (30,'(A)')'M22-TABLE'
WRITE (OUT,'(A)')'+Running M11, M12, M21, M22 calculation...
DO 130 I=1,399
  FREQ = REAL(I*10)
  WRITE (30,*) FREQ,REAL(M22TAB(i)),AIMAG(M22TAB(i))
130  CONTINUE

ELSE

* Writing the Kij value in the output file
write (30,'(A)')'K11-TABLE'
WRITE (OUT,'(A)')'+Running K11 calculation...
DO 200 I=1,399
  FREQ = REAL(I*10)
  WRITE (30,*) FREQ,REAL(K11TAB(i)),AIMAG(K11TAB(i))
200  CONTINUE
WRITE (30,'(A)')'K12-TABLE'
WRITE (OUT,'(A)')'+Running K12 calculation...
DO 210 I=1,399
  FREQ = REAL(I*10)
  WRITE (30,*) FREQ,REAL(K12TAB(i)),AIMAG(K12TAB(i))
210  CONTINUE
WRITE (30,'(A)')'K21-TABLE'
WRITE (OUT,'(A)')'+Running K21 calculation...
DO 220 I=1,399
  FREQ = REAL(I*10)
  WRITE (30,*) FREQ,REAL(K21TAB(i)),AIMAG(K21TAB(i))
220  CONTINUE
WRITE (30,'(A)')'K22-TABLE'
WRITE (OUT,'(A)')'+Running K22 calculation...
DO 230 I=1,399
  FREQ = REAL(I*10)
WRITE (30,*) FREQ, REAL(K22TAB(i)), AIMAG(K22TAB(i))  
200 CONTINUE
ENDF
WRITE(30,‘(A1)’);’
CLOSE (30)
WRITE(OUT,’(A)’)+Data written in file: ’//FILEOUT
STOP
* error melding
1000 WRITE(OUT,’(A)’)+OPEN ERROR AT OUTPUT-FILE:’//FILEOUT
STOP 1
1100 WRITE(OUT,’(A)’)+OPEN ERROR AT INPUT-FILE:’//INFILE
STOP 2
END
* end of main program
*
* auxiliary subroutines:
C
C###############################################################C
C
SUBROUTINE ZFEED(FREQ,Y5)
C
C###############################################################C
C
C  Input parameters: FREQ
C
C  Output parameters: Y5 [COMPLEX]
C             (admittance of transverse feeding)
C
C  Common blocks:     QTR,QPI2
C
C  Task of this routine: Calculates the equivalent admittance
C                      of the transverse feeding:
C                   Y5 = (RF + LF) // CF
C
C  Routine called in the following subroutines or functions:
C                  TRSLIC
C###############################################################C
C
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL FREQ, PI2, OMEGA, RF, LF, CF, QU
REAL RCU1, RCU2, CW1, L1, CW2, CSP, L2, M
COMPLEX Y5
*
COMMON/QTR/RCU1, RCU2, CW1, L1, CW2, RF, LF, CF, CSP, L2, M
COMMON/QPI2, PI2
C
OMEGA = PI2*FREQ
Y5 = (1./CMPLX(RF, OMEGA*LF)) + CMPLX(0, OMEGA*CF)
RETURN
END
C
SUBROUTINE TRSLIC(FREQ,A11,A12,A21,A22,ADET)

Input parameters:  FREQ  [REAL]

Output parameters:  A11, A12, A21, A22, ADET  [COMPLEX]

Common blocks:     QTR,QSLIC,QPI2

Task of this routine: Calculates the A-parameters describing the transformer.

Required subroutines: ZFEED,CMATMUL

Note: AA(1,i,j): REAL part of AA(i,j)
      AA(2,i,j): IMAGinary part of AA(i,j)

IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
REAL R(6,3),Y(2,2,2),OMCSP
REAL X(4,2),OMEGA,PI2
REAL CSP,CW2,FREQ,CW1,L1,L2,RCU1,RCU2,RF,LF,CF,M
REAL AA(2,2,2),BB(2,2,2),YINV(2,2,2)
REAL A1(2,2,2),A2(2,2,2),A3(2,2,2),A4(2,2,2)
REAL A5(2,2,2),A6(2,2,2),A7(2,2,2)
COMPLEX Y1,Y2,Y3,Y4,Y5,Y6,Y7
* COMMON/QTR/RCU1,RCU2,CW1,L1,L2,CW2,RF,LF,CF,CSP,L2,M
* COMMON/QPI2/PI2

OMEGA = PI2*FREQ
OMCSP = OMEGA*CSP
* blocking capacitor
   Y7 = CMPLX(0.,OMCSP)
* parallel feeding
   CALL ZFEED(FREQ,Y5)
* admitances in the equivalent circuit
* Y1
   Y1 = 1./CMPLX(RCU1,(OMEGA*(L1-M)))
*Y2
   Y2 = CMPLX(0.,(OMEGA*CW1))
*Y3
   Y3 = 1./CMPLX(RCU2,(OMEGA*(L2-M)))
*Y4
   Y4=CMPLX(0.,OMEGA*CW2))
*Y6
Y6=CMPLX(0.,(-1./(omega*M)))

* corresponding matrices
CALL PARA(Y6,A6)
CALL SERA(Y1,A1)
CALL SERA(Y3,A3)
CALL PARA(Y2,A2)
CALL PARA(Y4,A4)
CALL PARA(Y5,A5)
CALL SERA(Y7,A7)

* matrix multiplications
CALL CMATMUL(A5,A7,BB,2,2,2)
CALL CMATMUL(BB,A2,AA,2,2,2)
CALL CMATMUL(AA,A1,BB,2,2,2)
CALL CMATMUL(BB,A6,AA,2,2,2)
CALL CMATMUL(AA,A3,BB,2,2,2)
CALL CMATMUL(BB,A4,AA,2,2,2)

C making complex out of two REAL
A11 = CMPLX(AA(1,1,1),AA(2,1,1))
A12 = CMPLX(AA(1,1,2),AA(2,1,2))
A21 = CMPLX(AA(1,2,1),AA(2,2,1))
A22 = CMPLX(AA(1,2,2),AA(2,2,2))

C adet=(a11*a22)-(a12*a21) is the determinant of the a-matrix
ADET = (A11*A22)-(A12*A21)
RETURN
END
SUBROUTINE SERA(Y,A)

 Input parameters: Y [COMPLEX]

 Output parameters: A(2,2,2) [ARRAY OF REAL]

 Common blocks: /

 Task of this routine: A matrix for serial admittance

 Routine called in the following subroutines or functions:
 TRSLIC

 IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
 REAL A(2,2,2)
 COMPLEX Y,Z

 *  
 Z = 1./Y  
 A(1,1,1) = 1.  
 A(2,1,1) = 0.  
 A(1,1,2) = REAL(Z)  
 A(2,1,2) = AIMAG(Z)  
 A(1,2,1) = 0.  
 A(2,2,1) = 0.  
 A(1,2,2) = 1.  
 A(2,2,2) = 0.  
 RETURN
 END

SUBROUTINE PARA(Y,A)

 Input parameters: Y [COMPLEX]

 Output parameters: A(2,2,2) [array of REAL]

 Common blocks: /

 Task of this routine: A matrix for serial admittance

 Routine called in the following subroutines or functions:
 TRSLIC

 IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)  
 REAL A(2,2,2)  
 COMPLEX Y
* A(1,1)
  A(1,1,1) = 1.
  A(2,1,1) = 0.
* A(1,2)
  A(1,1,2) = 0.
  A(2,1,2) = 0.
* A(2,1)
  A(1,2,1) = REAL(Y)
  A(2,2,1) = AIMAG(Y)
* A(2,2)
  A(1,2,2) = 1.
  A(2,2,2) = 0.
RETURN
END
C
C**************************************************************************C
C
SUBROUTINE Z0W(FREQ,Z0)
C
C**************************************************************************C
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER(L)
COMPLEX Z0
REAL Z0R1,FREQ,Z0R2,Z0C1,Z0C2,Z0RS,Z0CS
COMMON/QZ0/Z0R1,Z0R2,Z0C1,Z0C2,Z0RS,Z0CS
*
CALL IMPED6(Z0R1,Z0R2,Z0C1,Z0C2,Z0RS,Z0CS,FREQ,Z0)
RETURN
END
C**************************************************************************C
C
SUBROUTINE ZgW(FREQ,Zg)
C
C**************************************************************************C
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER(L)
COMPLEX Zg
REAL ZgR1,FREQ,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS
COMMON/QZg/ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS
*
call imped6(ZgR1,ZgR2,ZgC1,ZgC2,ZgRS,ZgCS,FREQ,Zg)
RETURN
END
SUBROUTINE IMPED6(RP1, RP2, CP1, CP2, RS, CS, FREQ, Zeq)

Note: when a parameter is set to 0 then the corresponding resistor or capacitance does not exist.

Formal parameter list: RP1, RP2, CP1, CP2, RS, CS, FREQ, Zeq

Input parameters:
- RS [REAL]; series resistance
- CS [REAL]; series capacitance
- RP1 [REAL]; parallel resistance
- RP2 [REAL]; parallel resistance
- CP1 [REAL]; parallel capacitance
- CP2 [REAL]; parallel capacitance
- FREQ [REAL]; frequency

Output parameters:
- Zeq [COMPLEX]

Common blocks: QPI2
Task of this routine: Equivalent impedance of:

SPECIAL CASES:

A. SYSTEM Parallel

1. CP1 not 0
   1.1 rp1 not 0
   1.2 rp1 = 0

2. CP1 = 0
   2.1 rp1 not 0
   2.2 rp1 = 0

3. idem if CP2 = 0
4. RP2 = 0 and rp1 = 0
C###            5. CP2 = 0 and CP1 = 0                         ###C
C###           C. Conclusion: Zeq = sum of the two          ###C
C###                 systems in any case                    ###C
C###                                                        ###C
C###############################################################C
C                                                          ###C
IMPLICIT LOGICAL (A-K, M-Z), CHARACTER (L)
REAL CP1, CP2, RP1, RP2
REAL CS, RS, N, UL
REAL FREQ, PI2, OMEGA
COMPLEX D, C, Zseq, ZA, ZB
*
COMMON/QPI2/PI2
*
OMEGA = PI2*FREQ
IF (CP1.EQ.0) THEN
   C = CMPLX(RP1, 0.)
ELSE
   C = RP1 + (1./CMPLX(0., OMEGA*CP1))
ENDIF
IF (CP2.EQ.0) THEN
   D = CMPLX(RP2, 0.)
ELSE
   D = RP2 + (1./CMPLX(0., OMEGA*CP2))
ENDIF
N = CABS(C)
UL = CABS(D)
* if one of them is 0 then no parallel calculation
IF ((N.EQ.0.).OR.(UL.EQ.0.)) then
   ZA = C + D
ELSE
   ZA = C & D in parallel
   ZA = C*D/(C+D)
ENDIF
C System series
IF (CS.EQ.0) THEN
   ZB = CMPLX(RS, 0.)
ELSE
   ZB = RS + (1./CMPLX(0., OMEGA*CS))
ENDIF
c both
Zeq=ZA+ZB
RETURN
END

C
C SUBROUTINE CMATMUL(A,B,C,L,MM,N)
C
C#******************************************************************************
C
C Input parameters:
C A [REAL] ARRAY [2,L,MM]
C B [REAL] ARRAY [2,MM,N]
C L (INTEGER)
C MM (INTEGER)
C N (INTEGER)
C
C Example: A(i,j) = A(1,i,j) + j*A(2,i,j)
C
C Output parameters:
C C = [REAL] ARRAY [2,L,N]
C
C Task of this routine: C = A*B
C SUBROUTINE FOR THE COMPLEX MATRIX MULTIPLICATION
C
C Routine called in the following subroutines or functions:
C TRSLIC
C Important notice: It is not possible to do A*A=A
C#******************************************************************************
C
IMPLICIT LOGICAL (A-K,M-Z), CHARACTER (L)
INTEGER I,J,K,L,MM,N
REAL A(2,L,MM),B(2,MM,N)
REAL C(2,L,N)
*
DO 10 I=1,L
DO 10 J=1,N
C(1,I,J)=0.0
C(2,I,J)=0.0
C COMPLEX multiplication: a(2,i,k) * b(2,k,j) = d(2,i,j)
DO 20 K=1,MM
C(1,I,J)=C(1,I,J)+A(1,I,K)*B(1,K,J)-A(2,I,K)*B(2,K,J)
20 CONTINUE
10 CONTINUE
RETURN
END
Appendix A5

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   G.S.Moschytz
   Bell Telephone Laboratories series
   Van Nostrand Reinhold Company
# SICOFI® Application Together with Transformer SLIC for USA Specification

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1 Introduction

The requirements for an analog line card on the USA market are oriented on the AT&T specification for the public network.

The return loss has to be very high (> 32 dB) and it is a 3 dB gain in transmit direction and a 3 dB loss in receive direction needed. If a transformer SLIC with series line feeding will be used, a great transformer (for DC-current) has to be taken.

In this note a SLIC circuit for the USA-specification with series feeding, a high return loss and a good echo return loss is presented.

2 Circuit Description

This SLIC needs some external components, which support the 3 dB gain in transmit direction and a loss of 3 dB in receive direction. This hardware supports the B-filter of the SICOFI, too. In the following refer to figure 1 on the next page.

The resistor $R_8$ is used for serial feeding. The feeding has to be symmetrically to ground and therefore it is possible to place the battery between the half of $R_8$ of both lines. This resistor and the impedance $Z_0$ put in the return loss. The $Z_0$ is transformed with the winding ratio of the transformer. By the resistor $R_8$ and by the ratio of the transformer (here: $\bar{\omega} = 1$) the OP1 has to amplify the signal. The OP1 amplifies the received signal and the transmit direction must have a gain of 3 dB, therefore the B-filter of the SICOFI can not set the echo return loss. The OP2 is used as a subtraction amplifier. OP2 amplifies the transmit signal and subtracts the receive signal. In this case a good echo return loss can be achieved.

$R_5$ and $R_6$ set the gain of the transmit signal. $C_3$, $R_3$ and $R_4$ set the subtracting factor. The capacitances $C_1$ and $C_2$ are decoupling the DC of the OP's. Because the input impedance of the SICOFI is very high (MΩ – GΩ). $R_7$ forms together with $C_2$ a defined time constant.
Figure 1
Transformer SLIC with Series Feeding
3 Calculation

The SICOFI coefficient program calculates the coefficients for this transformer SLIC application. The result file is shown now:

Result file:

Input_file_name: SPEC = USA.SPE
BYTE = COM.BYT CHNR = 0,A
PLQ = N
ON = ALL REL = Y SHORT = N
OPT = Z+X+R+B ZXRB = OOON
FZ = 300.00 3400.0 ZLIM = 2.00
ZREP =N ZSIGN = 1
FR = 200.00 3400.0
RFIL = Y RREFQ = N RREF = 0.13303
FX = 300.00 3300.0
XFIL = Y XREFQ = N XREF =-0.20747
FB = 300.00 3400.0 BLIM = 2.00 TBM = 1
BREP = Y BSIGN = 1
APOF = 0.00E+00 DPOF = 0.00E+00 APRE = 0.00E+00 DPRE = 0.00E+00
XZQ = 0.4296875000000000E-01 -0.97656250000000000E-03
-0.21484375000000000E-01 -0.11962890625000000E-01
0.23681640625000000E-01
XRQ = 0.9921875000 -0.0019531250 0.0087890625 0.0000000000
0.0058590000
XXQ = 1.0234375000 0.0175781250 -0.0058593750 0.0175781250 -0.000976000
XBQ = 0.12451171875000000E+00 -0.20312500000000000E+00
0.24023437500000000E+00 -0.66894531250000000E-01
-0.19531250000000000E+00
0.18359375000000000E+00 0.46630859375000000E-01
-0.27929687500000000E+00 0.26953125000000000E+00
-0.13671875000000000E+00
XGQ = 0.5390625000 1.9062500000

Bytes for Z-Filter (13): 50,DA,AE,EC,A1,8F,5B,A1
Bytes for R-Filter (2B): 60,29,90,60,B9,8D,0C,9E
Bytes for X-Filter (23): D0,D8,95,EB,29,95,0B,A5
Bytes for Gain-factors (30): 31,1A,00,AB
2nd part of bytes B-Filter (0B): 00,4B,21,24,3A,5C,E1,13
1st part of bytes B-Filter (03): AC,BA,4C,23,2D,BA,31,9F
Bytes for B-filter delay (18): 19,19,11,19
Run # 1

Z-FILTER calculation results
Reference impedance for optimization (ZI):
ERZI = 1  RSER = 0.60E+03  CSER = 0.00E+00  RPAR = 0.00E+00  CPAR = 0.00E+0
Calculated and quantized coefficients:

XZ = 0.04365 -0.00107 -0.02153 -0.01207  0.02380
XZQ = 0.04297 -0.00098 -0.02148 -0.01196  0.02368
Bytes for Z-Filter (13): 50,DA,AE,EC,A1,8F,5B,A1

RETURN LOSS

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>20.730</td>
<td>1800.</td>
<td>45.638</td>
</tr>
<tr>
<td>200.</td>
<td>26.652</td>
<td>1900.</td>
<td>45.382</td>
</tr>
<tr>
<td>300.</td>
<td>30.370</td>
<td>2000.</td>
<td>46.163</td>
</tr>
<tr>
<td>400.</td>
<td>34.691</td>
<td>2100.</td>
<td>47.060</td>
</tr>
<tr>
<td>500.</td>
<td>36.589</td>
<td>2200.</td>
<td>48.100</td>
</tr>
<tr>
<td>600.</td>
<td>40.543</td>
<td>2300.</td>
<td>48.591</td>
</tr>
<tr>
<td>700.</td>
<td>44.228</td>
<td>2400.</td>
<td>49.615</td>
</tr>
<tr>
<td>800.</td>
<td>47.593</td>
<td>2500.</td>
<td>50.019</td>
</tr>
<tr>
<td>900.</td>
<td>51.728</td>
<td>2600.</td>
<td>51.354</td>
</tr>
<tr>
<td>1000.</td>
<td>57.415</td>
<td>2700.</td>
<td>54.655</td>
</tr>
<tr>
<td>1100.</td>
<td>60.717</td>
<td>2800.</td>
<td>55.913</td>
</tr>
<tr>
<td>1200.</td>
<td>53.655</td>
<td>2900.</td>
<td>54.597</td>
</tr>
<tr>
<td>1300.</td>
<td>50.692</td>
<td>3000.</td>
<td>53.429</td>
</tr>
<tr>
<td>1400.</td>
<td>47.352</td>
<td>3100.</td>
<td>52.410</td>
</tr>
<tr>
<td>1500.</td>
<td>46.852</td>
<td>3200.</td>
<td>51.385</td>
</tr>
<tr>
<td>1600.</td>
<td>46.116</td>
<td>3300.</td>
<td>49.153</td>
</tr>
<tr>
<td>1700.</td>
<td>45.321</td>
<td>3400.</td>
<td>47.402</td>
</tr>
</tbody>
</table>

Min. Z-loop reserve: 42.834 dB
at frequency: 8500.0 Hz

Min. Z-loop mirror signal reserve: 44.918 dB
at frequency: 16000.0 Hz
Run # 1

X-FILTER calculation results

Calculated and quantized coefficients:

\[
\begin{align*}
XX &= 1.02160 \quad 0.01799 \quad -0.00562 \quad 0.01789 \quad -0.00021 \\
XXQ &= 1.02344 \quad 0.01758 \quad -0.00586 \quad 0.01758 \quad -0.00098 \\
\end{align*}
\]

Bytes for X-Filter (23): D0,D8,95,EB,29,95,0B,A5

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300.</td>
<td>-0.409</td>
<td>1900.</td>
<td>-0.219</td>
</tr>
<tr>
<td>400.</td>
<td>-0.387</td>
<td>2000.</td>
<td>-0.243</td>
</tr>
<tr>
<td>500.</td>
<td>-0.361</td>
<td>2100.</td>
<td>-0.265</td>
</tr>
<tr>
<td>600.</td>
<td>-0.331</td>
<td>2200.</td>
<td>-0.286</td>
</tr>
<tr>
<td>700.</td>
<td>-0.300</td>
<td>2300.</td>
<td>-0.302</td>
</tr>
<tr>
<td>800.</td>
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<td>2400.</td>
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<tr>
<td>900.</td>
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</tr>
<tr>
<td>1000.</td>
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<td>-0.313</td>
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<tr>
<td>1100.</td>
<td>-0.188</td>
<td>2700.</td>
<td>-0.301</td>
</tr>
<tr>
<td>1200.</td>
<td>-0.170</td>
<td>2800.</td>
<td>-0.280</td>
</tr>
<tr>
<td>1300.</td>
<td>-0.158</td>
<td>2900.</td>
<td>-0.250</td>
</tr>
<tr>
<td>1400.</td>
<td>-0.154</td>
<td>3000.</td>
<td>-0.213</td>
</tr>
<tr>
<td>1500.</td>
<td>-0.156</td>
<td>3100.</td>
<td>-0.170</td>
</tr>
<tr>
<td>1600.</td>
<td>-0.164</td>
<td>3200.</td>
<td>-0.122</td>
</tr>
<tr>
<td>1700.</td>
<td>-0.179</td>
<td>3300.</td>
<td>-0.072</td>
</tr>
<tr>
<td>1800.</td>
<td>-0.197</td>
<td>3400.</td>
<td>-0.021</td>
</tr>
<tr>
<td>1900.</td>
<td>-0.219</td>
<td>3500.</td>
<td>0.005</td>
</tr>
<tr>
<td>2000.</td>
<td>-0.243</td>
<td>3600.</td>
<td>0.004</td>
</tr>
</tbody>
</table>

GX results:

All attenuation values (in dB) refer to FREF = 1014. Hz

RLX  SLIC+Z  VREF/V Sicofi  XREF  GX
-3.00  -3.33  - 6.17  - -0.21  =  -5.63  ideal
-2.97  -3.33  + 6.17  + -0.21  +  -5.60  quant

Second byte for Gain: ,00,AB

Calculation of transmit transfer function (AD)

All attenuation values (in dB) refer to FREF = 1014.0 Hz

Reference impedance for optimization (ZI):

ERZI = 1  RSER = 600.  CSER = 0.000E+00  RPAR = 0.  CPAR = 0.000E+0

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>44.913</td>
<td>2000.</td>
<td>-0.055</td>
</tr>
<tr>
<td>200.</td>
<td>0.339</td>
<td>2100.</td>
<td>-0.082</td>
</tr>
<tr>
<td>300.</td>
<td>-0.121</td>
<td>2200.</td>
<td>-0.098</td>
</tr>
<tr>
<td>400.</td>
<td>-0.089</td>
<td>2300.</td>
<td>-0.115</td>
</tr>
<tr>
<td>500.</td>
<td>-0.082</td>
<td>2400.</td>
<td>-0.126</td>
</tr>
<tr>
<td>600.</td>
<td>-0.073</td>
<td>2500.</td>
<td>-0.130</td>
</tr>
</tbody>
</table>
### R-FILTER calculation results

**Calculated and quantized coefficients:**

- \( XR = 0.98877 \; -0.00364 \; 0.00934 \; 0.00048 \; 0.00679 \)
- \( XRQ = 0.99219 \; -0.00195 \; 0.00879 \; 0.00000 \; 0.00586 \)

**Bytes for R-Filter (2B):**

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>-0.014</td>
<td>1900</td>
<td>0.097</td>
</tr>
<tr>
<td>400</td>
<td>0.006</td>
<td>2000</td>
<td>0.094</td>
</tr>
<tr>
<td>500</td>
<td>0.029</td>
<td>2100</td>
<td>0.094</td>
</tr>
<tr>
<td>600</td>
<td>0.053</td>
<td>2200</td>
<td>0.097</td>
</tr>
<tr>
<td>700</td>
<td>0.077</td>
<td>2300</td>
<td>0.103</td>
</tr>
<tr>
<td>800</td>
<td>0.099</td>
<td>2400</td>
<td>0.109</td>
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<tr>
<td>900</td>
<td>0.118</td>
<td>2500</td>
<td>0.116</td>
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<tr>
<td>1000</td>
<td>0.131</td>
<td>2600</td>
<td>0.122</td>
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<td>1100</td>
<td>0.140</td>
<td>2700</td>
<td>0.124</td>
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<tr>
<td>1200</td>
<td>0.144</td>
<td>2800</td>
<td>0.123</td>
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<tr>
<td>1300</td>
<td>0.142</td>
<td>2900</td>
<td>0.118</td>
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<tr>
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<td>0.107</td>
</tr>
<tr>
<td>1500</td>
<td>0.129</td>
<td>3100</td>
<td>0.091</td>
</tr>
<tr>
<td>1600</td>
<td>0.120</td>
<td>3200</td>
<td>0.071</td>
</tr>
<tr>
<td>1700</td>
<td>0.111</td>
<td>3300</td>
<td>0.048</td>
</tr>
<tr>
<td>1800</td>
<td>0.103</td>
<td>3400</td>
<td>0.023</td>
</tr>
<tr>
<td>1900</td>
<td>0.097</td>
<td>3500</td>
<td>1.003</td>
</tr>
<tr>
<td>2000</td>
<td>0.094</td>
<td>3600</td>
<td>0.002</td>
</tr>
</tbody>
</table>

**GR results:**

All attenuation values (in dB) refer to \( FREF = 1014 \) Hz

<table>
<thead>
<tr>
<th>-RLR</th>
<th>SLIC+Z</th>
<th>VSICOFI/VREF</th>
<th>RREF</th>
<th>GR</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.00</td>
<td>3.70</td>
<td>-6.17</td>
<td>0.13</td>
<td>5.34 ideal</td>
</tr>
<tr>
<td>3.03</td>
<td>3.70</td>
<td>-6.17</td>
<td>0.13</td>
<td>5.37 quant</td>
</tr>
</tbody>
</table>

**First byte for Gain (30):**

31,1A

Calculation of receive transfer function (DA)
All attenuation values (in dB) refer to FREF = 1014.0 Hz

Terminating impedance ZI at a,b line!
ERZI = 1 RSER = 600. CSER = 0.000E+00 RPAR = 0. CPAR = 0.000E+0

<table>
<thead>
<tr>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
<th>FREQ (Hz)</th>
<th>loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100.</td>
<td>35.758</td>
<td>2000.</td>
<td>-0.079</td>
</tr>
<tr>
<td>200.</td>
<td>0.033</td>
<td>2100.</td>
<td>-0.079</td>
</tr>
<tr>
<td>300.</td>
<td>-0.086</td>
<td>2200.</td>
<td>-0.076</td>
</tr>
<tr>
<td>400.</td>
<td>-0.067</td>
<td>2300.</td>
<td>-0.065</td>
</tr>
<tr>
<td>500.</td>
<td>-0.064</td>
<td>2400.</td>
<td>-0.054</td>
</tr>
<tr>
<td>600.</td>
<td>-0.059</td>
<td>2500.</td>
<td>-0.037</td>
</tr>
<tr>
<td>700.</td>
<td>-0.036</td>
<td>2600.</td>
<td>-0.021</td>
</tr>
<tr>
<td>800.</td>
<td>-0.024</td>
<td>2700.</td>
<td>-0.009</td>
</tr>
<tr>
<td>900.</td>
<td>-0.005</td>
<td>2800.</td>
<td>0.010</td>
</tr>
<tr>
<td>1000.</td>
<td>-0.002</td>
<td>2900.</td>
<td>0.025</td>
</tr>
<tr>
<td>1100.</td>
<td>0.007</td>
<td>3000.</td>
<td>0.039</td>
</tr>
<tr>
<td>1200.</td>
<td>0.011</td>
<td>3100.</td>
<td>0.062</td>
</tr>
<tr>
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<td>-0.001</td>
<td>3200.</td>
<td>0.092</td>
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<tr>
<td>1400.</td>
<td>-0.006</td>
<td>3300.</td>
<td>0.143</td>
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<td>0.227</td>
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<tr>
<td>1600.</td>
<td>-0.033</td>
<td>3500.</td>
<td>0.381</td>
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<tr>
<td>1700.</td>
<td>-0.052</td>
<td>3600.</td>
<td>0.671</td>
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<tr>
<td>1800.</td>
<td>-0.061</td>
<td>3700.</td>
<td>1.264</td>
</tr>
<tr>
<td>1900.</td>
<td>-0.076</td>
<td>3800.</td>
<td>2.649</td>
</tr>
</tbody>
</table>

Run # 2

B-FILTER calculation results

Terminating impedance for optimization (ZL):
ERZL = 1 RSL = 600. CSL = 0.000E+00 RPL = 0. CPPL = 0.000E+0

Terminating impedance ZL at a,b line!

Calculated and quantized coefficients:

XB = 0.12434 -0.20703 0.24080 -0.06671 -0.19477
0.18490 0.04671 -0.27867 0.27106 -0.13596

XBQ = 0.12451 -0.20312 0.24023 -0.06689 -0.19531
0.18359 0.04663 -0.27930 0.26953 -0.13672

2nd part of bytes B-Filter (0B): 00,4B,21,24,3A,5C,E1,13
1st part of bytes B-Filter (03): AC,BA,4C,23,2D,BA,31,9F
### TRANS HYBRID LOSS

<table>
<thead>
<tr>
<th>FREQ</th>
<th>loss</th>
<th>FREQ</th>
<th>loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Hz)</td>
<td>(dB)</td>
<td>(Hz)</td>
<td>(dB)</td>
</tr>
<tr>
<td>100.</td>
<td>26.747</td>
<td>1800.</td>
<td>33.657</td>
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<tr>
<td>200.</td>
<td>20.474</td>
<td>1900.</td>
<td>30.738</td>
</tr>
<tr>
<td>300.</td>
<td>26.448</td>
<td>2000.</td>
<td>29.176</td>
</tr>
<tr>
<td>400.</td>
<td>34.852</td>
<td>2100.</td>
<td>28.525</td>
</tr>
<tr>
<td>500.</td>
<td>37.946</td>
<td>2200.</td>
<td>28.141</td>
</tr>
<tr>
<td>600.</td>
<td>31.736</td>
<td>2300.</td>
<td>28.321</td>
</tr>
<tr>
<td>700.</td>
<td>29.294</td>
<td>2400.</td>
<td>28.877</td>
</tr>
<tr>
<td>800.</td>
<td>27.968</td>
<td>2500.</td>
<td>30.016</td>
</tr>
<tr>
<td>900.</td>
<td>27.463</td>
<td>2600.</td>
<td>31.356</td>
</tr>
<tr>
<td>1000.</td>
<td>27.519</td>
<td>2700.</td>
<td>32.514</td>
</tr>
<tr>
<td>1100.</td>
<td>28.381</td>
<td>2800.</td>
<td>32.774</td>
</tr>
<tr>
<td>1200.</td>
<td>30.012</td>
<td>2900.</td>
<td>32.179</td>
</tr>
<tr>
<td>1300.</td>
<td>31.863</td>
<td>3000.</td>
<td>31.047</td>
</tr>
<tr>
<td>1400.</td>
<td>36.126</td>
<td>3100.</td>
<td>30.917</td>
</tr>
<tr>
<td>1500.</td>
<td>41.026</td>
<td>3200.</td>
<td>30.506</td>
</tr>
<tr>
<td>1600.</td>
<td>47.533</td>
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<td>31.842</td>
</tr>
<tr>
<td>1700.</td>
<td>37.952</td>
<td>3400.</td>
<td>34.411</td>
</tr>
</tbody>
</table>

Additional B-filter delay (in seconds): .625E-04
Bytes for B-filter delay (18): 19,19,11,19

The coefficients for the SICOFI can now be extracted from the result file. In the appendix the transfer measurements of the analog line card for the USA-specification can be found.
4 Conclusion

This transformer SLIC fulfills the AT&T specifications in terms of return loss, echo return loss, the gain in transmit and the loss in receive direction. The frequency distortion in both directions fulfill the specification, too. Other specifications, like long lines with a terminating impedance of $600 \, \Omega + 2.16 \, \mu F$ or other levels have not been tested.

5 Appendix

In the appendix you will find

– parts list
– plots of transfer measurements:
  a) return loss
  b) echo return loss
  c) level in transmit and receive direction
  d) frequency distortion in transmit and receive direction.

Parts List

$\begin{align*}
 R_1 & = 150 \, k\Omega \\
 R_2 & = 200 \, k\Omega \\
 R_3 & = 15 \, k\Omega \\
 R_4 & = 24 \, k\Omega \\
 R_5 & = 20 \, k\Omega \\
 R_6 & = 75 \, k\Omega \\
 R_7 & = 10 \, k\Omega \\
 R_8 & = 220 \, \Omega \\
 C_1 & = 1 \, \mu F \\
 C_2 & = 1 \, \mu F \\
 C_3 & = 330 \, nF \\
 Z_0 & = 243 \, \Omega \\
 \text{OP1} & = \text{LM356} \\
 \text{OP2} & = \text{LM356} \\
 \end{align*}$

Transformer
Figure 2

Figure 3
Figure 4

Figure 5
Figure 6

Figure 7
SICOFI® Layout Recommendations for Analog Line-Card Applications

<table>
<thead>
<tr>
<th>Contents</th>
<th>Page</th>
</tr>
</thead>
<tbody>
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<td>724</td>
</tr>
<tr>
<td>2 Power Supply</td>
<td>724</td>
</tr>
<tr>
<td>3 SICOFI® Decoupling</td>
<td>724</td>
</tr>
<tr>
<td>4 SICOFI® Analog and Digital Ground Pins</td>
<td>724</td>
</tr>
<tr>
<td>5 Separation of Digital and Analog Lines</td>
<td>725</td>
</tr>
<tr>
<td>6 Pairing Voice Leads</td>
<td>725</td>
</tr>
<tr>
<td>7 Structured Form</td>
<td>725</td>
</tr>
<tr>
<td>8 Crosstalk</td>
<td>725</td>
</tr>
<tr>
<td>9 Connector Pins</td>
<td>725</td>
</tr>
<tr>
<td>10 Analog and Digital Ground Separation</td>
<td>725</td>
</tr>
<tr>
<td>11 Voltage Difference between AGND and DGND</td>
<td>725</td>
</tr>
<tr>
<td>12 High Voltage</td>
<td>726</td>
</tr>
<tr>
<td>13 Ground Plane</td>
<td>726</td>
</tr>
<tr>
<td>14 Resistance of Ground Leads</td>
<td>726</td>
</tr>
<tr>
<td>15 Ground Loop</td>
<td>726</td>
</tr>
<tr>
<td>16 Separation of Pathsf</td>
<td>726</td>
</tr>
<tr>
<td>17 Leads with Transients</td>
<td>726</td>
</tr>
<tr>
<td>18 Plug-in Boards Connector</td>
<td>727</td>
</tr>
</tbody>
</table>
1 Introduction

The most important steps in designing a low noise Line Card are to insure that the layout of the circuit components and of the electrical paths guarantees a minimum of cross-coupling between analog and digital signals, and to provide well bypassed and clean power supplies, solid ground plane and minimal lead lengths between components.

This paper is a general guide line for the layout of an Analog Line Card. In most cases two printed circuit layers are sufficient but with more layers it is possible to separate the different channels, to have a better ground plane and to obtain a smaller printed circuit board.

2 Power Supply

All leads of the power sources should be bypassed to ground on each printed circuit board. At least one electrolytic capacitor is recommended (at least 10 µF) at the point where all power traces from the components join prior to interfacing with the power connector.

3 SICOFI® Decoupling

It is recommended to connect a bypass filter close to each SICOFI composed of an electrolytic capacitor (10 µF) in parallel to a ceramic capacitor (e.g. 100 nF) between the power supplies (+ 5 V and – 5 V) and ground. Thus spikes due to digital switching and high frequency components would be filtered out.

The optimum value for the ceramic capacitor is determined by trying and changing the value and observing the noise in each channel.

4 SICOFI® Analog and Digital Ground Pins

The best configuration to minimize the noise is to connect the digital ground pin and the analog ground pin directly under the SICOFI to the analog ground of the printed board.

Definitions:  
AGND = Analog Ground  
DGND = Digital Ground
5  **Separation of Digital and Analog Lines**

The layout of the traces should be such that the analog signals are separated from the digital clock and data leads as far as possible.

6  **Pairing Voice Leads**

Analog voice circuit leads should be paired on their layouts so that no interfering circuit paths should be permitted to run parallel to them and/or between them.

7  **Structured Form**

Arrange the layout for each line trunk or channel circuit on the board in identical form.

8  **Crosstalk**

Line circuits mounted extremely close to line circuits of adjacent channel increase the possibility of interchannel crosstalk.

9  **Connector Pins**

Avoid the assignment of adjacent connector pins to analog signals and digital signals or power.

10  **Analog and Digital Ground Separation**

The optimal grounding configuration except for the SICOFI parts is to maintain separate digital and analog grounds on the circuit boards, and to carry these grounds back to the power supply with a low impedance connection. This keeps the grounds separate over the entire system except at the power supply.

The SICOFI ground pins and the SLIC ground should be connected to AGND (see figure 1).

11  **Voltage Difference between AGND and DGND**

The voltage difference between analog ground leads (AGND) and digital ground leads (DGND) should be kept low.

One method of preventing any substantial voltage difference between leads is to connect two diodes back to back in opposite directions across these two ground leads on each board.
12 High Voltage

No digital or high voltage level (e.g. ringing supply) should run below or in parallel with analog voice frequency connections. If the analog lines are on the top of the printed circuit board, then AGND or power supply leads should be below them on the other side of the board to prevent analog coupling.

13 Ground Plane

The SICOFL should be separated from traces at the bottom of the printed circuit board by a ground plane directly under the device on the component side.

14 Resistance of Ground Leads

Both ground and power supply leads should have as little resistance and inductance as possible.

This can be accomplished by using a ground plane whenever possible. If traces have to be used for ground connections, a minimum width should be maintained for these leads (e.g. 2 mm) and extra large through holes be used when passing the ground connections through the printed circuit board.

15 Ground Loop

Make sure that no ground loops exist on the printed circuit board:
This would be a perfect antenna for all kind of noises.

16 Separation of Paths

Ground separation traces between sensitive leads can be used to avoid cross coupling.

17 Leads with Transients

Relay operation, ringing voltage, surges can produce transients. Leads carrying such signals should be routed well away from both analog and digital circuits on the line card and in backplanes.
18 Plug-in Boards Connector

For plug-in boards, it is recommended to use a connector with different pin lengths. This should help to connect the interface in a distinct order if the board is plugged in under power condition. The correct order is:

- Super extra long ground pins (allow to discharge the electrostatic charges)
- Extra long pins for power supplies
- Long pins for the clock signals
- Normal pins for the rest of the signals.

Figure 1
Using SICOFL®-2 (PEB 2260) in IOM®-2 Mode

<table>
<thead>
<tr>
<th>Contents</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1  Introduction</td>
<td>729</td>
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<tr>
<td>2  Menu Trackfile Software</td>
<td>729</td>
</tr>
<tr>
<td>3  General Aspects</td>
<td>729</td>
</tr>
</tbody>
</table>
1 Introduction

The SICOFI®-2 can work in two different serial interface modes

→ SLD
→ IOM-2

In this application note necessary programming steps for the SICOFI-2 in an IOM-2 environment are shown. They are documented and explained in a trackfile print out that is used on the SIPB 5000 Userboard System.

So the mnemonics refer directly to the modular architecture of the userboard concept. In order to verify this application note the following hardware equipment is used with a PC:

- Mainboard SIPB 5000
- Line-Card Module SIPB 5121
- SICOFI-2 Board SIPB 5135
- PCM4 Adaptor SIPB 5311a

2 Menu Trackfile Software

In this application note, the SICOFI-2 is connected to two HARRIS-SLICs HC 5502. Basically the SICOFI-2 will be

- identified
- initialized
- programmed.

The used coefficients for filter programming have been derived from the "SICOFI-Application Note HARRIS-SLIC HC 5502".

For any other hardware environment just use the register handling of the SICOFI-2 and modify it for your own application.

3 General Aspects

Using the IOM-2 interface with a data clock of 4.096 MHz (DCL) and an 8-kHz frame signal, eight IOM channels per 125 μs frame on each IOM-line will be offered. These IOM channels can be individually addressed by the SICOFI-2 by its time slots capability. A specific time slot (IOM channel) is selected by pin-strapping at TS1/TS2 pins at the SICOFI-2. This is carried out by external hardware and the switch S1 on the SICOFI-2 Board.
Selected IOM®-2 and TS1/TS2 Pins in Relation Switch S1

Table 1

<table>
<thead>
<tr>
<th>IOM-2 Channel</th>
<th>TS1</th>
<th>TS2</th>
<th>Position S1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>N</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>P</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>P</td>
<td>N</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>P</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>N</td>
<td>0</td>
<td>7</td>
</tr>
<tr>
<td>6</td>
<td>P</td>
<td>P</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td>N</td>
<td>P</td>
<td>9</td>
</tr>
</tbody>
</table>

P = + 5 V, 0 = 0 V, N = – 5 V

Any IOM-channel can be splitted into 4 bytes:
- 2 data channels (8 bits each)
- 1 MONITOR channel (8 bits)
- C/I field (signaling, 6 bits)
- handshake bits MR, MX (2 bits) for MONITOR handshaking.

A basic demand in IOM-2 realizations is, that any connected circuit has to have its own address. For the SICOFI-2 the value 81h has been specified.

Before any data can be transmitted to the SICOFI-2 via IOM-2 interface (e.g. SOP/COP commands) the specific address has to be sent in order to activate the device.

Additionally any IOM-2 device can identify itself on request. This is done by sending an identify request string, consisting of bytes 80h, 00h. The SICOFI-2 responds with bytes 80h, 80h.

**Note:** SICOFI-2 Version 1.x has a minor error that can be temporarily solved by programming a work-around.

Problem: A Write sequence to the SICOFI-2 blocks the next three commands. They will be just ignored.

Work-around: Any Write command is followed by a Read command. The Read command enables correct acception of new commands.

Therefore all programming sequences to the SICOFI-2 end with a SOP-Read command in this application note. As reaction, the SICOFI-2 sends the contents of CR1 back. For versions higher 1.x, the additional SOP-Read command can be omitted.
C ********************************************
C *        SICOFI2                        *
C *         with                       *
C *      HARRIS HC 5502                     *
C ********************************************

C Hardware: Line Card SIPB 5121
C     SICOFI2 BOARD SIPB 5135
C     PCM4 Adaptor SIPB 5311
C
C configuration:
C     Line Card: via software
C     ICOFI 2: S1 in position 5
C     PCM4 Adaptor: J1 is open

C ********************************************
C SICOFI2 set up in channel 3 of IOM2
C
C     S1 in position 5
C
C ********************************************
C please run the trackfile
C     LC_IOM2.TRK
C first to configure the Line Card

C ********************************************
C ********************************************
C selecting EPIC to monitor handshake
C in channel 3
C     /LINECA/EPIC/MCHSTR/MFSAR 1C

C ********************************************
C in case of channel 0 MFSAR = 04          *
C     S1 position 2                      *
C in case of channel 1 MFSAR = 0C          *
C     S1 position 3                      *
C in case of channel 2 MFSAR = 14          *
C     S1 position 4                      *
C in case of channel 4 MFSAR = 24          *
C     S1 position 6                      *
C in case of channel 5 MFSAR = 2C          *
C     S1 position 7                      *
C in case of channel 6 MFSAR = 34          *
C     S1 position 8                      *
C in case of channel 7 MFSAR = 3C          *
C     S1 position 9                      *
C ********************************************
C channel 3 B1 to PCM timeslot 1
W /LINECA/EPIC/MARSCR/MADR 81
W /LINECA/EPIC/MARSCR/MAAR B0
W /LINECA/EPIC/MARSCR/MACR 71
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 81
W /LINECA/EPIC/MARSCR/MACR 60
C
C PCM timeslot 1 to channel 3 B1
W /LINECA/EPIC/MARSCR/MADR 01
W /LINECA/EPIC/MARSCR/MAAR 31
W /LINECA/EPIC/MARSCR/MACR 71
C
C channel 3 B2 to PCM timeslot 2
W /LINECA/EPIC/MARSCR/MADR 82
W /LINECA/EPIC/MARSCR/MAAR B1
W /LINECA/EPIC/MARSCR/MACR 71
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 82
W /LINECA/EPIC/MARSCR/MACR 60
C
C PCM timeslot 2 to channel 3 B2
W /LINECA/EPIC/MARSCR/MADR 02
W /LINECA/EPIC/MARSCR/MAAR 30
W /LINECA/EPIC/MARSCR/MACR 71
C
C sicofi identification:
C write to SICOFI2 80h, 00h
W /LINECA/EPIC/MCHSTR/MFFIFO 80
W /LINECA/EPIC/MCHSTR/MFFIFO 00
C EPIC enable receive + transmit
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C EPIC received data
R /LINECA/EPIC/MCHSTR/STAR 26
C first byte from SICOFI2
R /LINECA/EPIC/MCHSTR/MFFIFO 80
R /LINECA/EPIC/MCHSTR/STAR 26
C second byte from SICOFI2
R /LINECA/EPIC/MCHSTR/MFFIFO 80
R /LINECA/EPIC/MCHSTR/STAR 27
C reset FIFO
W /LINECA/EPIC/MCHSTR/CMDR 01
R /LINECA/EPIC/MCHSTR/STAR 25
C
C initialization of sicofi:
C CR4, CR3, CR2, CR1
C 00h, 00h, 00h, 00h
C for both channels of SICOFI2
C
C SICOFI2 address = 81h
W /LINECA/EPIC/MCHSTR/MFFIFO 81
W /LINECA/EPIC/MCHSTR/MFFIFO C2
W /LINECA/EPIC/MCHSTR/MFFIFO 21
W /LINECA/EPIC/MCHSTR/MFFIFO 04
W /LINECA/EPIC/MCHSTR/MFFIFO 90
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO 47
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the X-filter
C
C GX - filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 30
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 20
W /LINECA/EPIC/MCHSTR/MFFIFO 92
W /LINECA/EPIC/MCHSTR/MFFIFO 80
W /LINECA/EPIC/MCHSTR/MFFIFO 80
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO 47
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the GX-
C filter
C
C GR - filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 32
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO A0
W /LINECA/EPIC/MCHSTR/MFFIFO 11
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO 47
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the GR-
C filter
C
B - filter part 1 programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 03
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO C4
W /LINECA/EPIC/MCHSTR/MFFIFO 12
W /LINECA/EPIC/MCHSTR/MFFIFO 23
W /LINECA/EPIC/MCHSTR/MFFIFO 32
W /LINECA/EPIC/MCHSTR/MFFIFO 72
W /LINECA/EPIC/MCHSTR/MFFIFO B9
W /LINECA/EPIC/MCHSTR/MFFIFO B2
W /LINECA/EPIC/MCHSTR/MFFIFO BA
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO 47
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C part 1
C
C B - filter part 2 programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 0B
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 97
W /LINECA/EPIC/MCHSTR/MFFIFO FD
W /LINECA/EPIC/MCHSTR/MFFIFO C8
W /LINECA/EPIC/MCHSTR/MFFIFO DD
W /LINECA/EPIC/MCHSTR/MFFIFO 4C
W /LINECA/EPIC/MCHSTR/MFFIFO C2
W /LINECA/EPIC/MCHSTR/MFFIFO BC
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO 47
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C part 2
C
C B-filter delay programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 18
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 19
W /LINECA/EPIC/MCHSTR/MFFIFO 19
W /LINECA/EPIC/MCHSTR/MFFIFO 11
W /LINECA/EPIC/MCHSTR/MFFIFO 19
C read back CR1 and power up:
W /LINECA/EPIC/MCHSTR/MFFIFO 67
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C delay
C
C
C SICOFI2 CHANNEL B
C programming the filter
C
C Z-filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 93
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 20
W /LINECA/EPIC/MCHSTR/MFFIFO BA
W /LINECA/EPIC/MCHSTR/MFFIFO EA
W /LINECA/EPIC/MCHSTR/MFFIFO 25
W /LINECA/EPIC/MCHSTR/MFFIFO 23
W /LINECA/EPIC/MCHSTR/MFFIFO 41
W /LINECA/EPIC/MCHSTR/MFFIFO C1
W /LINECA/EPIC/MCHSTR/MFFIFO BB
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the Z-filter
C
C R - filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO AB
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO D0
W /LINECA/EPIC/MCHSTR/MFFIFO C8
W /LINECA/EPIC/MCHSTR/MFFIFO 84
W /LINECA/EPIC/MCHSTR/MFFIFO DC
W /LINECA/EPIC/MCHSTR/MFFIFO B1
W /LINECA/EPIC/MCHSTR/MFFIFO 93
W /LINECA/EPIC/MCHSTR/MFFIFO 02
W /LINECA/EPIC/MCHSTR/MFFIFO 1D
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the R-filter
C
C X-filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO A3
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 50
W /LINECA/EPIC/MCHSTR/MFFIFO C8
W /LINECA/EPIC/MCHSTR/MFFIFO B5
W /LINECA/EPIC/MCHSTR/MFFIFO 4A
W /LINECA/EPIC/MCHSTR/MFFIFO C2
W /LINECA/EPIC/MCHSTR/MFFIFO 21
W /LINECA/EPIC/MCHSTR/MFFIFO 04
W /LINECA/EPIC/MCHSTR/MFFIFO 90
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the X-filter
C
C GX - filters programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO B0
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 20
W /LINECA/EPIC/MCHSTR/MFFIFO 92
W /LINECA/EPIC/MCHSTR/MFFIFO 80
W /LINECA/EPIC/MCHSTR/MFFIFO 80
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the GX-
C filters
C
C GR - filter programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 32
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO A0
W /LINECA/EPIC/MCHSTR/MFFIFO 11
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the GR-
C filters
C
C B - filter part 1 programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 83
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO C4
W /LINECA/EPIC/MCHSTR/MFFIFO 12
W /LINECA/EPIC/MCHSTR/MFFIFO 23
W /LINECA/EPIC/MCHSTR/MFFIFO 32
W /LINECA/EPIC/MCHSTR/MFFIFO 72
W /LINECA/EPIC/MCHSTR/MFFIFO B9
W /LINECA/EPIC/MCHSTR/MFFIFO B2
W /LINECA/EPIC/MCHSTR/MFFIFO BA
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C part 1
C
C B - filter part 2 programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 8B
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 97
W /LINECA/EPIC/MCHSTR/MFFIFO FD
W /LINECA/EPIC/MCHSTR/MFFIFO C8
W /LINECA/EPIC/MCHSTR/MFFIFO DD
W /LINECA/EPIC/MCHSTR/MFFIFO 4C
W /LINECA/EPIC/MCHSTR/MFFIFO C2
W /LINECA/EPIC/MCHSTR/MFFIFO BC
C read back CR1 and power down:
W /LINECA/EPIC/MCHSTR/MFFIFO C7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMDR 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C part 2
C
C B - filter delay programming
W /LINECA/EPIC/MCHSTR/MFFIFO 81
C COP command:
W /LINECA/EPIC/MCHSTR/MFFIFO 98
C coefficients:
W /LINECA/EPIC/MCHSTR/MFFIFO 19
W /LINECA/EPIC/MCHSTR/MFFIFO 19
W /LINECA/EPIC/MCHSTR/MFFIFO 19
W /LINECA/EPIC/MCHSTR/MFFIFO 11
W /LINECA/EPIC/MCHSTR/MFFIFO 19
C read back CR1 and power up:
W /LINECA/EPIC/MCHSTR/MFFIFO E7
R /LINECA/EPIC/MCHSTR/STAR 24
C send the bytes to SICOFI & read out
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
C byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C SICOFI address
R /LINECA/EPIC/MCHSTR/MFFIFO 81
C new byte in FIFO
R /LINECA/EPIC/MCHSTR/STAR 26
C CR1:
R /LINECA/EPIC/MCHSTR/MFFIFO 00
R /LINECA/EPIC/MCHSTR/STAR 27
W /LINECA/EPIC/MCHSTR/CMRD 01
C FIFO is empty
R /LINECA/EPIC/MCHSTR/STAR 25
C end of programming the B-filter
C delay
C
C SICOFI2 is programmed and power up
C of both channels
C
C ************************************
C       activation of HARRIS-SLIC
C
C ***/RC = 1 ,/PD = 1
C
C ************************************
C
C ADR, C3A, CI2, CI1, C2, C1, 1, 1
C 1/0, X, X, X,/RC,/PD, 1, 1
C
C SICOFI2 channel A
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 38
W /LINECA/EPIC/MARSCR/MACR 48
C
C SICOFI2 channel B
W /LINECA/EPIC/MARSCR/MADR 8F
W /LINECA/EPIC/MARSCR/MAAR 38
W /LINECA/EPIC/MARSCR/MACR 48
C
C end of activation
C
C ************************************
C
C read the signaling information
C
C /GKD, /SHD
C from the HARRIS-SLIC
C
C ************************************
C
C switch on the LAST-LOOK-LOGIC
C
W /LINECA/EPIC/MARSCR/CMRD 40
C
C CI2B, CI1B, I1B, CI2A, CI1A, I1A, 1, 1
C /GKD,/GKD,/SHD,/GKD,/GKD,/GKD,/SHD, 1, 1
CHANNEL B, CHANNEL A, 1, 1

SLIC AT SICOFL2 CHANNEL B+A

MADR = FF A= on hook B= on hook
MADR = FB A=off hook B= on hook
MADR = DF A= on hook B=off hook
MADR = DB A=off hook B=off hook

W /LINECA/EPIC/MARSCR/MAAR B8
W /LINECA/EPIC/MARSCR/MACR C8
R /LINECA/EPIC/MARSCR/MADR D8

Both terminals are off-hook and no ground key

END OF TRACKFILE
DAML Simulation Using the SIPB 5000 Userboard System

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1 Introduction

This application note describes the simulation of a Digital Added Main Line (DAML) using components of the Siemens ISDN PC User Board system SIPB 5000.

In practice during the transition period from a pure analog telephone network to the future Integrated Services Digital Network (ISDN) the DAML provides a cost-effective provisional extension (doubling) of traffic capability of existing installations.

DAML is a concept of integrating digital transmission into an existing analog communication system with the aim of increasing its performance. It provides telephony facility for two independent analog subscribers on a single local wire pair. The transmission principle uses echo cancellation and message recovery according to American National Standards Institute (ANSI) T1E1 specification for the U interface (2B1Q line code).

This application note is not only to show the simplicity of insertion of this feature but also the high quality of the extra gained transmission channel. In addition this example is a good introduction to digital communication and to the flexibility in application of the SIPB system components.

For simulation a subscriber loop is reproduced using a TE and a NTS station. The necessary hardware is listed in section 2. Special information on setting up and running the test equipment are given in section 3.

As from versatility reasons several features of the ISDN components are left for software programming, the respective initializing procedure is performed by track files which are to be found in section 5. A PC AT serves for the interface to the user. Using the Siemens Menu Software which enables access down to the register level of the employed components gives deep insight into the operational procedure of such a set-up.
2 Required Hardware

Figure 1 shows the set-up of a subscriber loop between a NTS and a TE, where a DAML is to be simulated. The hardware required at the terminals differs slightly according to the peculiar configuration:

NTS-Configuration:

1 ITAC® Module SIPB 5140
1 Audio Interface Module V2.0 SIPB 5130
1 Layer-2 Module SIPB 5120-2
1 IEC-Q Reference Module LT SIPB 2091
1 SICOFI®-2 Board SIPB 5135
2 Analog Telephone Sets
2 SLICs (HARRIS HC 5502)
1 Adapter cable

TE-Configuration:

1 Audio Interface Module V2.0 SIPB 5130
1 Layer-2 Module SIPB 5120-2
1 IEC-Q Reference Module NT SIPB 2091
1 SICOFI®-2 Board SIPB 5135
2 Analog Telephone Sets
2 SLICs (HARRIS HC 5502)
1 Adapter Cable

As the SICOFI-2 Board has been developed originally for connection to the Line Card Module, and the Audio Interface Module at its Service Access Connector (SAC) shows a differing pinning, a peculiar Adapter Cable has to be used. The particular design depends on whether the RESET of the SICOFI-2 will be used or not (including an inverter stage or not). A schematic of these Adapter Cables is shown in figure 2.
Figure 1
Set-Up for Simulating a DAML
Top: RESET not connected to the SICOFI-2 Board, bottom: RESET connected to the SICOFI-2 Board

**Figure 2**

Wiring of the SICOFI-2 Adapter Cable
3 Operational Information

The modules of the NTS and TE configurations each are plugged to the Add-on Module Connectors (AMC) of a SIPB 5000 Mainboard, which in turn are inserted into an expansion slot of an IBM AT or compatible (For safety reasons please refer to the respective instructions of the User Manual of the computer manufacturer for internal installation procedures).

Before insertion into the PC, the modules are configured to the particular mode:

**NTS:**
- Layer-2 Module: all DIP switches to OFF position
- Audio Interface Module: Switches S1 … 4 to OFF position, no jumpers set

**TE:**
- Layer-2 Module: all DIP switches to OFF position
- Audio Interface Module: Switches S1, S2, S4 to OFF position, Switch S3 to ON position, no jumpers set

The IEC-Q Reference Boards are connected externally to that SAC which corresponds to the AMC the Layer-2 Modules are plugged to. Similarly the SICOFI-2 Boards bearing two SLICs each are connected to the SAC corresponding to the Audio Interface Modules using the peculiar Adapter Cable (refer to figure 1).

Telephone sets and SLICs, and IEC-Q Reference Boards are interconnected using single wire pairs (a/b lines and U interface respectively).

The configuration of IEC-Q Reference Boards depends on the particular mode:

**LT:**
- DIP switches 1 … 3 to OFF position
- DIP switches 4 … 7 to ON position
- Jumpers J1, J2 set, Jumper J5 open
- Jumpers J3, J4 set to position a-b

**TE:**
- DIP switch S1 to OFF position
- DIP switches 2 … 7 to ON position
- Jumpers J1, J2 set

At the SICOFI-2 Board the rotary switch S1 is put to position 0 (DIP switch S2 don't care).
4 Glossary

AMC     Add-on module connector
DAML    Digital added main line
IEC-Q   ISDN echo cancellation circuit conforming to 2B1Q transmission mode
ISDN    Integrated services digital network
ITAC    ISDN terminal adapter circuit
LT      Line termination
NT      Network termination
NTS     Network termination on S bus
SAC     Service access connector
SICOFI  Signal processing codec filter
SICOFI-2 Dual channel codec filter
SIPB    Siemens ISDN PC User Board (system)
SLIC    Subscriber line circuit
TE      Terminal equipment
2B1Q    Transmission mode requiring 120-kHz bandwidth
5 Track Files

Note: The filter coefficients of the SICOFI are calculated to meet the specifications of the Deutsche Bundespost.

5.1 Track File DAMLCOT.TRK for COT Side

C ****************************************
C this track file supports DAML applica-
C tions with the SICOFI2 board SIPB 5135
C and fits to the track file D A M L
C (RT = Remote Terminal)
C
C
C note:
C - please use audio module Version 2.0
C - please use firmware Version V2.0
C - please use a adaptor cable for SICOFI2
C   board SIPB 5135
C
C - start with this track file!
C ****************************************
C
C reset and deactivation the IECQ
W /LI_NTS/ICCB/SERIAL/CIXR 47
R /LI_NTS/ICCB/SERIAL/ISTA 04
R /LI_NTS/ICCB/SERIAL/CIRR 06
R /LI_NTS/ICCB/SERIAL/ISTA 00
W /LI_NTS/ICCB/SERIAL/CIXR 40
R /LI_NTS/ICCB/SERIAL/ISTA 04
R /LI_NTS/ICCB/SERIAL/CIRR 3E
R /LI_NTS/ICCB/SERIAL/ISTA 00
C
C S T O P - S T O P - S T O P
C now go to DAML RT side
C FOR reset and deactivation of RT
C
C
C activation of U interface
W /LI_NTS/ICCB/SERIAL/CIXR 60
R /LI_NTS/ICCB/SERIAL/ISTA 04
R /LI_NTS/ICCB/SERIAL/CIRR 22
C
C W A I T - W A I T - W A I T
C several seconds, max. 15sec,
C for adaption of echo cancellor
C and equalizer
C
R /LI_NTS/ICCB/SERIAL/ISTA 04
R /LI_NTS/ICCB/SERIAL/CIRR 1E
R /LI_NTS/ICCB/SERIAL/CIRR 1C
R /LI_NTS/ICCB/SERIAL/CIRR 1C
C
C STOP - STOP - STOP
C go back to RT side
C for ACTIVATION INDICATION (AI)
C
R /LI_NTS/ICCB/SERIAL/ISTA 04
R /LI_NTS/ICCB/SERIAL/CIRR 32
R /LI_NTS/ICCB/SERIAL/ISTA 00
R /LI_NTS/ICCB/SERIAL/CIRR 30
R /LI_NTS/ICCB/SERIAL/CIRR 30
R /LI_NTS/ICCB/SERIAL/CIRR 30
R /LI_NTS/ICCB/SERIAL/ISTA 00
C
C switch the proper port of ICC
W /LI_NTS/ICCB/SERIAL/SPCR 45
D
C programming of SICOFI2
C the configuration register CR3-CR1
D
B 05
B 00
B 00
B 00
B 85
B 00
B 00
B 00
X /LI_NTS/ICCB/BUS/CONTR
C
C the Z-filters
D
B 13
B 20
B BA
B EA
B 25
B 23
B 41
B C1
B BB
B 93
B 20
B BA
B EA
B 25
B 23
B 41
B C1
B BB
X /LI_NTS/ICCB/BUS/CONTR
C
C the R-filters
D
B  2B
B  D0
B  C8
B  84
B  DC
B  B1
B  93
B  02
B  1D
B  AB
B  D0
B  C8
B  84
B  DC
B  B1
B  93
B  02
B  1D
X /LI_NTS/ICCB/BUS/CONTR
D
C
C the X-filters
D
B  23
B  50
B  C8
B  B5
B  4A
B  C2
B  21
B  04
B  90
B  A3
B  50
B  C8
B  B5
B  4A
B  C2
B  21
B  04
B  90
X /LI_NTS/ICCB/BUS/CONTR
C
C the B-filters part 1
D
B  0B
B  00
B  97
B  FD
B  C8
B  DD
B 4C
B C2
B BC
B 8B
B 00
B 97
B FD
B C8
B DD
B 4C
B C2
B BC
X /LI_NTS/ICCB/BUS/CONTR
C
C the B-filters part 2
D
B 03
B C4
B 12
B 23
B 32
B 72
B B9
B B2
B BA
B 83
B C4
B 12
B 23
B 32
B 72
B B9
B B2
B BA
X /LI_NTS/ICCB/BUS/CONTR
C
C the B-filters delay
D
B 18
B 19
B 19
B 11
B 19
B 19
B 98
B 19
B 19
B 11
B 19
X /LI_NTS/ICCB/BUS/CONTR
C
C the GX filters
D
B 30
B 20
B 92
B 80
B 80
B B0
B 20
B 92
B 80
B 80
X /LI_NTS/ICCB/BUS/CONTR
C
C the GR-filters
D
B 3A
B A0
B 11
B BA
B A0
B 11
X /LI_NTS/ICCB/BUS/CONTR
C
C switch on all filters
D
B 25
B 00
B 00
B FC
B A5
B 00
B 00
B FC
X /LI_NTS/ICCB/BUS/CONTR
C
C activation of the HARRIS-SLIC
W /LI_NTS/ICCB/ SERIAL/SSCX 33
C
C now you can talk
C
C *****************************************************
C END of TRACK FILE
C *****************************************************
5.2 Track File DAMLRT.TRK for RT Side

C ****************************************
C this track file supports DAML applications with the SICOFI2 board SIPB 5135
C and fits to the track file DAML (COT = Central Office Terminal)
C
C note:
C - please use audio module Version 2.0
C - please use firmware Version V2.0
C - please use an adaptor cable for SICOFI2 board SIPB 5135
C
C - start with DAML (COT)!
C ****************************************
C
C reset and deactivate the IECQ
W /LI_TE/ICCB/SERIAL/SCPR 80
W /LI_TE/ICCB/SERIAL/CIXR 47
W /LI_TE/ICCB/SERIAL/SCPR 00
R /LI_TE/ICCB/SERIAL/ISTA 04
R /LI_TE/ICCB/SERIAL/CIRR 1E
R /LI_TE/ICCB/SERIAL/ISTA 04
R /LI_TE/ICCB/SERIAL/CIRR 02
R /LI_TE/ICCB/SERIAL/ISTA 00
W /LI_TE/ICCB/SERIAL/CIXR 7C
R /LI_TE/ICCB/SERIAL/ISTA 04
R /LI_TE/ICCB/SERIAL/CRIR 3E
R /LI_TE/ICCB/SERIAL/ISTA 00
C
C STOP - STOP - STOP
C go back to DAML COT side
C for activation the U interface
C
R /LI_TE/ICCB/SERIAL/ISTA 04
R /LI_TE/ICCB/SERIAL/CIRR 22
R /LI_TE/ICCB/SERIAL/ISTA 00
R /LI_TE/ICCB/SERIAL/CIRR 20
R /LI_TE/ICCB/SERIAL/ISTA 00
C
C ACTIVATION INDICATION (AI)
C
W /LI_TE/ICCB/SERIAL/CIXR 70
R /LI_TE/ICCB/SERIAL/ISTA 04
R /LI_TE/ICCB/SERIAL/CIRR 32
R /LI_TE/ICCB/SERIAL/CIRR 30
R /LI_TE/ICCB/SERIAL/CIRR 30
R /LI_TE/ICCB/SERIAL/ISTA 00
C
C now the U interface is transparent
C
C
C switch the proper port in ICC
W /LI_TE/ICCB/SERIAL/SPCR 45
W /LI_TE/ICCB/SERIAL/SSCX 00
C
C programming of SICOFI2
C the configuration register CR3-CR1
D
B 05
B 00
B 00
B 00
B 85
B 00
B 00
B 00
X /LI_TE/ICCB/BUS/CONTR
C
C the Z-filters
D
B 13
B 20
B BA
B EA
B 25
B 23
B 41
B C1
B BB
B 93
B 20
B BA
B EA
B 25
B 23
B 41
B C1
B BB
X /LI_TE/ICCB/BUS/CONTR
C
C the R-filters
D
B 2B
B D0
B C8
B 84
B DC
B B1
B 93
B 02
B 1D
C the X-filters

C the B-filters part 1
C the B-filters part 2

C the B-filters delay

C the GX filters
X /LI_TE/ICCB/BUS/CONTR
C
C the GR-filters
D
B 3A
B A0
B 11
B BA
B A0
B 11
X /LI_TE/ICCB/BUS/CONTR
C
C switch on all filters
D
B 25
B 00
B 00
B FC
B A5
B 00
B 00
B FC
X /LI_TE/ICCB/BUS/CONTR
C
C activation of the HARRIS-SLIC
W /LI_TE/ICCB/ SERIAL/SSCX 33
C
C now you can talk
C
C*****************************************************************************
C END of TRACK FILE
C*****************************************************************************