ICs for Communications

ISDN Communication Controller
ICC
PEB 2070
PEF 2070

User's Manual 01.94
Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25 \, ^\circ C$ and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about “Processing Guidelines” and “Quality Assurance” for ICs, see our “Product Overview”.

Edition 01.94

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# Table of Contents

## 1 Features
- 1.1 Pin Configuration ............................................. 8
- 1.2 Pin Definitions and Functions .................................. 9
- 1.3 Logic Symbol .................................................. 13
- 1.4 Functional Block Diagram ....................................... 14
- 1.5 System Integration ............................................. 15
- 1.5.1 ISDN Applications ............................................ 15
- 1.5.2 Other Applications ........................................... 19
- 1.5.3 Microprocessor Environment .................................. 20

## 2 Functional Description
- 2.1 General Functions and Device Architecture ...................... 21
- 2.2 Serial Interface Modes ......................................... 22
  - 2.2.1 IOM®-1 Mode (IMS = 0, DIM2 = 0) .......................... 23
  - 2.2.2 IOM®-2 Mode (IMS = 1) ..................................... 25
  - 2.2.3 HDLC Controller Mode (IMS = 0, DIM2 = 1) ............... 26
- 2.3 Interfaces ...................................................... 26
  - 2.3.1 mP Interface ................................................ 27
  - 2.3.2 ISDN Oriented Modular (IOM®) Interface .................. 28
  - 2.3.3 SSI (Serial Port A) ......................................... 36
  - 2.3.4 SLD ......................................................... 37
- 2.4 Individual Functions ........................................... 38
  - 2.4.1 Layer-2 Functions for HDLC ................................ 38
  - 2.4.1.1 Message Transfer Modes ................................ 39
  - 2.4.1.2 Protocol Operations (auto mode) ......................... 41
  - 2.4.1.3 Reception of Frames .................................... 42
  - 2.4.1.4 Transmission of Frames .................................. 47
  - 2.4.2 B-Channel Switching (IOM®-1) .............................. 50
  - 2.4.3 Access to B / IC Channels .................................. 52
  - 2.4.4 C/I Channel Handling ....................................... 57
  - 2.4.5 MONITOR Channel Handling ................................ 57
  - 2.4.6 Terminal Specific Functions ................................. 62
  - 2.4.7 Test Functions ............................................. 63
  - 2.4.8 Documentation of the Auto Mode ............................ 64

## 3 Operational Description
- 3.1 Microprocessor Interface Operation ............................ 91
- 3.2 Reset ............................................................ 91
- 3.3 Initialization .................................................. 93
- 3.4 IOM® Interface Connections .................................... 95
- 3.5 Processing ..................................................... 100
  - 3.5.1 Interrupt Structure .......................................... 100
  - 3.5.2 Data Transfer ............................................... 103
  - 3.5.2.1 HDLC Frame Reception ................................ 107
  - 3.5.2.2 HDLC Frame Transmission ............................... 109
<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Detailed Register Description</td>
<td>112</td>
</tr>
<tr>
<td>4.1</td>
<td>HDLC Operation and Status Registers</td>
<td>117</td>
</tr>
<tr>
<td>4.1.1</td>
<td>Receive FIFO RFIFO Read Address 00-1FH</td>
<td>117</td>
</tr>
<tr>
<td>4.1.2</td>
<td>Transmit FIFO XFIFO Write Address 00-1FH</td>
<td>117</td>
</tr>
<tr>
<td>4.1.3</td>
<td>Interrupt Status Register ISTA Read Address 20H</td>
<td>117</td>
</tr>
<tr>
<td>4.1.4</td>
<td>Mask Register MASK Write Address 20H</td>
<td>119</td>
</tr>
<tr>
<td>4.1.5</td>
<td>Status Register STAR Read Address 2H</td>
<td>119</td>
</tr>
<tr>
<td>4.1.6</td>
<td>Command Register CMDR Write Address 2H</td>
<td>120</td>
</tr>
<tr>
<td>4.1.7</td>
<td>Mode Register MODE Read/Write Address 22H</td>
<td>121</td>
</tr>
<tr>
<td>4.1.8</td>
<td>Timer Register TIMR Read/Write Address 23H</td>
<td>124</td>
</tr>
<tr>
<td>4.1.9</td>
<td>Extended Interrupt Register EXIR Read Address 24H</td>
<td>126</td>
</tr>
<tr>
<td>4.1.10</td>
<td>Transmit Address 1 XAD1 Write Address 24H</td>
<td>127</td>
</tr>
<tr>
<td>4.1.11</td>
<td>Receive Frame Byte Count Low RBCL Read Address 25H</td>
<td>128</td>
</tr>
<tr>
<td>4.1.12</td>
<td>Transmit Address 1 XAD2 Write Address 25H</td>
<td>128</td>
</tr>
<tr>
<td>4.1.13</td>
<td>Received SAPI Register SAPR Read Address 26H</td>
<td>129</td>
</tr>
<tr>
<td>4.1.14</td>
<td>SAPI1 Register SAP1 Write Address 26H</td>
<td>129</td>
</tr>
<tr>
<td>4.1.15</td>
<td>Receive Status Register RSTA Read Address 27H</td>
<td>130</td>
</tr>
<tr>
<td>4.1.16</td>
<td>SAP12 Register SAP2 Write Address 27H</td>
<td>131</td>
</tr>
<tr>
<td>4.1.17</td>
<td>TE1 Register 1 TE1 Write Address 28H</td>
<td>132</td>
</tr>
<tr>
<td>4.1.18</td>
<td>Receive HDLC Control Register RHCR Read Address 29H</td>
<td>132</td>
</tr>
<tr>
<td>4.1.19</td>
<td>TE12 Register TE12 Write Address 29H</td>
<td>134</td>
</tr>
<tr>
<td>4.1.20</td>
<td>Receive Frame Byte Count High RBCH Read Address 30H</td>
<td>134</td>
</tr>
<tr>
<td>4.1.21</td>
<td>Status Register 2 STAR2 Read Address 2BH</td>
<td>135</td>
</tr>
<tr>
<td>4.2</td>
<td>Special Purpose Registers: IOM-1Mode</td>
<td>135</td>
</tr>
<tr>
<td>4.2.1</td>
<td>Serial Port Control Register SPCR Read/Write Address 30H</td>
<td>135</td>
</tr>
<tr>
<td>4.2.2</td>
<td>Command/Indication Receive Register CIRR Read Address 31H</td>
<td>137</td>
</tr>
<tr>
<td>4.2.3</td>
<td>Command/Indication Transmit Register CIXR Write Address 31H</td>
<td>138</td>
</tr>
<tr>
<td>4.2.4</td>
<td>MONITOR Receive Register MOR Read Address 32H</td>
<td>139</td>
</tr>
<tr>
<td>4.2.5</td>
<td>MONITOR Transmit Register MOX Write Address 32H</td>
<td>139</td>
</tr>
<tr>
<td>4.2.6</td>
<td>SIP Signaling Code Receive SCR Read Address 33H</td>
<td>139</td>
</tr>
<tr>
<td>4.2.7</td>
<td>SIP Signaling Code Transmit SSCX Write Address 33H</td>
<td>139</td>
</tr>
<tr>
<td>4.2.8</td>
<td>SIP Feature Control Read SFCR Read Address 34H</td>
<td>140</td>
</tr>
<tr>
<td>4.2.9</td>
<td>SIP Feature Control Write SFCW Write Address 34H</td>
<td>140</td>
</tr>
<tr>
<td>4.2.10</td>
<td>Channel Register 1 C1R Read/Write Address 35H</td>
<td>140</td>
</tr>
<tr>
<td>4.2.11</td>
<td>Channel Register 2 C2R Read/Write Address 36H</td>
<td>140</td>
</tr>
<tr>
<td>4.2.12</td>
<td>B1 Channel Register B1CR Read Address 37H</td>
<td>141</td>
</tr>
<tr>
<td>4.2.13</td>
<td>Synchronous Transfer Control Register STCR Write Address 37H</td>
<td>141</td>
</tr>
<tr>
<td>4.2.14</td>
<td>B2 Channel Register B2CR Read Address 38H</td>
<td>142</td>
</tr>
<tr>
<td>4.2.15</td>
<td>Additional Feature Register 1 ADF1 Write Address 38H</td>
<td>142</td>
</tr>
<tr>
<td>4.2.16</td>
<td>Additional Feature Register 2 ADF2 Read/Write Address 39H</td>
<td>143</td>
</tr>
</tbody>
</table>
### Table of Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.3</td>
<td>144</td>
</tr>
<tr>
<td>4.3.1</td>
<td>144</td>
</tr>
<tr>
<td>4.3.2</td>
<td>146</td>
</tr>
<tr>
<td>4.3.3</td>
<td>146</td>
</tr>
<tr>
<td>4.3.4</td>
<td>147</td>
</tr>
<tr>
<td>4.3.5</td>
<td>148</td>
</tr>
<tr>
<td>4.3.6</td>
<td>148</td>
</tr>
<tr>
<td>4.3.7</td>
<td>148</td>
</tr>
<tr>
<td>4.3.8</td>
<td>149</td>
</tr>
<tr>
<td>4.3.9</td>
<td>149</td>
</tr>
<tr>
<td>5</td>
<td>156</td>
</tr>
<tr>
<td>6</td>
<td>168</td>
</tr>
</tbody>
</table>

Figure 24a until figure 26d are CCITT recommendations for comparison.
Introduction

The transmission and protocol functions in an ISDN basis access can be all be implemented using the CMOS circuits of the ISDN Oriented Modular (IOM®) chip set. While three chips, the S Bus interface Circuit SBC (PEB 2080), the ISDN Echo Cancellation circuit IEC (PEB 2090) and the ISDN Burst Controller IBC (PEB 2095) perform the transmission functions in different applications (S and U interface), the ISDN Communication Controller ICC (PEB 2070) acts as the D-channel-link-access protocol controller.

The IOM® architecture makes possible a wide range of configurations for the Basic Access, using the basic devices. These configurations essentially differ in the implementation of the layer-1 OSI functions, while the layer-2 functions are provided by the ICC for all configurations.

In addition to that, the PEB 2070 provides the interface to B-channel sources in the terminal and to a peripheral board controller (PEB 2050, 51, 52 etc.) at the exchange.

The HDLC packets of the ISDN D channel are handled by the ICC which transfers them to the associated microcontroller. The ICC has on-chip buffer memories (64 bytes per direction) for the temporary storage of data packets. Because of the overlapping I/O operations the maximum length of the D-channel packets is not limited. In one of its operating modes the device offers high level support of layer-2 functions of the LAPD protocol.

Aside from ISDN applications, the ICC can be used as a general purpose communication controller in all applications calling for LAPD, LAPB or other HDLC/SDLC based protocols.
ISDN Communication Controller (ICC)

Preliminary Data

1 Features

- Support of LAPD protocol
- Different types of operating modes for increased flexibility
- FIFO buffer (2 x 64 bytes) for efficient transfer of data packets
- Serial interfaces: IOM\textsuperscript{-}1, SLD, SSI
  \hspace{1cm} IOM\textsuperscript{-}2
- General purpose HDLC communication interface
- Implementation of IOM-1/IOM-2 MONITOR and C/I channel protocol to control layer 1 and peripheral devices
- D-channel access with contention resolution mechanism
- \(\mu\)P access to B channel and intercommunication channels
- B-channels switching
- Watchdog timer
- Test loops
- Advanced CMOS technology
- Low power consumption:
  - active : 17 mW (IOM-2)
  - : 8 mW (IOM-1)
  - standby : 3 mW

<table>
<thead>
<tr>
<th>Type</th>
<th>Ordering Code</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>PEB 2070-N</td>
<td>Q67100-H6213</td>
<td>P-LCC-28-R (SMD)</td>
</tr>
<tr>
<td>PEB 2070-P</td>
<td>Q67100-H6212</td>
<td>P-DIP-24</td>
</tr>
<tr>
<td>PEF 2070-N</td>
<td>H67100-H6246</td>
<td>P-LCC-28-R (SMD)</td>
</tr>
</tbody>
</table>

Semiconductor Group 7 01.94
1.1 Pin Configuration

(top view)
## Features

### 1.1 Pin Definitions and Functions

<table>
<thead>
<tr>
<th>Pin No. P-DIP</th>
<th>Pin No. P-LCC</th>
<th>Symbol</th>
<th>Input (I) Output (O)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>25</td>
<td>AD0/D0</td>
<td>I/O</td>
<td>Multiplexed Bus Mode: Address/Data bus. Transfers addresses from the µP system to the ICC and data between the µP system and the ICC.</td>
</tr>
<tr>
<td>22</td>
<td>26</td>
<td>AD1/D1</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>27</td>
<td>AD2/D2</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>28</td>
<td>AD3/D3</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>AD4/D4</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>AD5/D5</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>AD6/D6</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>AD7/D7</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>21</td>
<td>CS</td>
<td>I</td>
<td>Chip Select. A “Low” on this line selects the ICC for read/write operation.</td>
</tr>
<tr>
<td>–</td>
<td>23</td>
<td>R/W</td>
<td>I</td>
<td>Read/Write. When “High”, identifies a valid µP access as a read operation. When “Low”, identifies a valid µP access as a write operation (Motorola bus mode). Write. This signal indicates a write operation (Siemens/Intel bus mode).</td>
</tr>
<tr>
<td>19</td>
<td>23</td>
<td>WR</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>–</td>
<td>24</td>
<td>DS</td>
<td>I</td>
<td>Data Strobe. The rising edge marks the end of a valid read or write operation (Motorola bus mode). Read. This signal indicates a read operation (Siemens/Intel bus mode).</td>
</tr>
<tr>
<td>20</td>
<td>24</td>
<td>RD</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>18</td>
<td>INT</td>
<td>OD</td>
<td>Interrupt Request. The signal is activated when the ICC request an interrupt. It is an open drain output.</td>
</tr>
<tr>
<td>16</td>
<td>20</td>
<td>ALE</td>
<td>I</td>
<td>AddressLatchEnable. A high on this line indicates an address on the external address bus (Multiplexed bus typ only).</td>
</tr>
</tbody>
</table>
## Pin Definitions and Functions (cont’d)

<table>
<thead>
<tr>
<th>Pin No. P-DIP</th>
<th>Pin No. P-LCC</th>
<th>Symbol</th>
<th>Input (I)</th>
<th>Output (O)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>8</td>
<td>SCA</td>
<td>O</td>
<td></td>
<td><strong>Serial Clock Port A</strong>, IOM-1 timing mode. A 128-kHz data clock signal for serial port A (SSI).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Frame Sync Delayed</strong>, IOM-1 timing mode 1. An 8-kHz synchronization signal, delayed by 1/8 of a frame, for IOM-1 is supplied. In this mode a minimal round-trip delay for B1 and B2 channels is guaranteed.</td>
</tr>
<tr>
<td>7</td>
<td>8</td>
<td>FSD</td>
<td>O</td>
<td></td>
<td><strong>Serial Data Strobe 2</strong>, IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SCA/FSD/SDS2 takes on the function of SDS2 until a write access to SPCR is made.</td>
</tr>
<tr>
<td>7</td>
<td>8</td>
<td>SDS2</td>
<td>O</td>
<td></td>
<td><strong>Reset</strong>. A “High” on this input forces the ICC into reset state. The minimum pulse length is four clock periods. If the terminal specific functions are enabled, the ICC may also supply a reset signal.</td>
</tr>
<tr>
<td>8</td>
<td>9</td>
<td>RES</td>
<td>I/O</td>
<td></td>
<td><strong>Frame Sync</strong>. Input synchronization signal. IOM-2 mode: Indicates the beginning of IOM frame. Indicates the beginning of IOM and, if TSF = 0, frame (timing mode 0). Indicates the beginning of SLD frame (timing mode 1). HDLC-mode: Strobe signal of programmable polarity.</td>
</tr>
</tbody>
</table>

**Semiconductor Group**  10
## Pin Definitions and Functions (cont’d)

<table>
<thead>
<tr>
<th>Pin No. P-DIP</th>
<th>Pin No. P-LCC</th>
<th>Symbol</th>
<th>Input (I) Output (O)</th>
<th>Function</th>
</tr>
</thead>
</table>
| 11            | 14            | DCL    | I                    | Data Clock.  
IOM modes: Clock of the frequency equal to twice the data on the IOM interface.  
HDLC mode: Clock of frequency equal to the data on serial port B. |
| 19            | A0            | I      | Address bit 0 (Non-multiplexed bus type). |
| 5             | A1            | I      | Address bit 1 (Non-multiplexed bus type). |
| 6             | A2            | I      | Address bit 2 (Non-multiplexed bus type)  
**Serial Data Port Receive.**  
Serial data is received on this pin at standard TTL or CMOS level. An integrated pull-up circuit enables connection of an open-drain/open collector driver without an external pull-up resistor. SDAR is used only if IOM-1 mode is selected. |
| 11            | A3            | I      | Address bit 3 (Non-multiplexed bus type). |
| 12            | A4            | I      | Address bit 4 (Non-multiplexed bus type). |
| 10            | A5            | I      | Address bit 5 (Non-multiplexed bus type).  
**SLD Interface Port, IOM-1 mode.** This line transmits and receives serial data at standard TTL or CMOS levels.  
**External Awake** (terminal specific function). If a falling edge on this input is detected, the ICC generates an interrupt and, if enabled, a reset pulse. |
| 10            | SIP           | I/O    |                      |
| 10            | EAW           | I      |                      |
### Pin Definitions and Functions (cont’d)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>SDAX</td>
<td>Serial Data Port A transmit, IOM-1 mode. Transmit data is shifted out via this pin at standard TTL or CMOS levels.</td>
</tr>
<tr>
<td>6</td>
<td>SDS1</td>
<td>Serial Data Strobe 1, IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SDAX/SDS1 takes on the function of SDS1 until a write access to SPCR is made.</td>
</tr>
<tr>
<td>12</td>
<td>$V_{ss}$</td>
<td>Ground (0 V)</td>
</tr>
<tr>
<td>18</td>
<td>$V_{dd}$</td>
<td>Power supply (5 V ± 5%)</td>
</tr>
<tr>
<td>14</td>
<td>IDP0</td>
<td>IOM Data Port 0</td>
</tr>
<tr>
<td>13</td>
<td>IDP1</td>
<td>IOM Data Port 1</td>
</tr>
</tbody>
</table>
1.2 Logic Symbol

- **+5 V**, **0 V**, **RESET**, **V_{DD}**, **V_{SS}**, **RES**
- **SDAX/SDS1**, **SDAR**, **SSI (Serial Port A)**
- **SLD**, **SIP/EAW**
- **Clock/Frame Synchronization**, **DCL**, **FSC**
- **SCA/FSD/SDS2**
- **AD0 - 7 (D0 - 7)**, **(A0 - 5)**, **CS**, **WR (R/W)**, **RD (DS)**, **INT**, **ALE**
- **μP**
- **IOM® (Serial Port B)**, **IDP0**, **IDP1**

**Features**

*ITL00895*
1.3 Functional Block Diagram
1.4 System Integration

1.4.1 ISDN Applications

The reference model for the ISDN basic access according to CCITT I series recommendations consists of

- an exchange and trunk line termination in the central office (ET, LT)
- a remote network termination in the user area (NT)
- a two-wire loop (U interface) between NT and LT
- a four-wire link (S interface) which connects subscriber terminals and the NT in the user area as depicted in figure 1.

Figure 1
ISDN Subscriber Basic Access Architecture

The NT equipment serves as a converter between the U interface at the exchange and the S interface at the subscriber premises. The NT may consist of either an NT1 only or an NT1 together with an NT2 connected via the T interface which is physically identical to the S interface. The NT1 is a direct transformation between layer 1 of S and layer 1 of U. NT2 may include higher level functions like multiplexing and switching as in a PABX.
In terms of **channels** the ISDN access consists of:
- a number of 64 kbit/s bearer channels \((n \times B)\)
  - e.g. \(n = 2\) for basic rate ISDN access
  - \(n = 30\) or \(23\) for primary rate ISDN access;
- and a signaling channel \((D)\), either 16 (basic rate) or 64 (primary rate) kbit/s (figure 2).

**Figure 2**
ISDN Basic Access Channel Structure
The B channels are used for end-to-end circuit switched digital connections between communicating stations.

The D channel is used to carry signaling and data via protocols defined by the CCITT. These protocols cover the network services layers of the open system interconnection model (Layers 1-3). At layer 2, the data link layer, an HDLC type protocol is employed, the link access procedure on the D channel LAPD (CCITT Rec. Q. 920/1).

The ISDN Communication Controller PEB 2070 can be used in all ISDN applications involving establishment and maintenance of the data link connection in either the D channel or B channel. It also provides the interface to layer-1 functions controlled via the IOM which links the ICC to any transceiver or peripheral device. Depending on the interface mode, the ICC supports three serial interfaces and offers switching functions and \( \mu \)P access to voice/ data channels.

The applications comprise:
- Use as a signaling controller for the D channel
- Access to the D channel for data transmission
- Source/ sink for secured B-channel data

and the target equipment include:
- ISDN terminal
- ISDN PABX (NT2) and Central Office (ET) line card
- ISDN packet switches
- “Intelligent” NT1.

Terminal Applications

The concept of the ISDN basic access is based on two circuit-switched 64 kbit/s B channels and a message oriented 64 kbit/s D channel for packetized data, signaling and telemetry information.

Figure 3 shows an example of an integrated multifunctional ISDN terminal using the ICC. The transceiver provides the layer-1 connection to the transmission line, either an S or U interface, and is connected to the ICC and other, peripheral modules via the IOM-2 interface.

The D channel, containing signaling data and packet switched data, is processed by the ICC LAPD controller and routed via a parallel \( \mu \)P interface to the terminal processor. The high level support of the LAPD protocol which is implemented by the ICC allows the use of a low cost processor in cost sensitive applications.

The IOM-2 interface is used to connect diverse voice/data application modules:
- sources/ sinks for the D channel
- sources/ sinks for the B1 and B2 channels.
Different D-channel services (for different SAPI’s) can be simply implemented by connecting an additional ICC in parallel to the first one, for instance for transmitting p-packets in the D channel.

Up to eight ICCs may thus be connected to the D and C/I (Command/Indication) channels via the TIC bus. The ICCs handle contention autonomously.

Data transfer between the terminal controller and the different modules are done with the help of the IOM-2 MONITOR channel protocol. Each voice/data module can be accessed by an individual address. The same protocol enables the control of terminal modules that do not have an associated microcontroller (such as the Audio Ringing Codec Filter ARCOFI® : PSB 2160) and the programming of intercommunication inside the terminal. Two intercommunication channels IC1 and IC2 allow a 2 x 64 kbit/s transfer rate between voice/data modules.

In the example above (figure 3), one ICC is used for data packets in the D channel. A voice processor is connected to a programmable digital signal processing codec filter via IC1 and a data encryption module to a data device via IC2. B1 is used for voice communication, B2 for data communication.

The ICC ensures full upward compatibility with IOM-1 devices. It provides the additional strobe, clock and data lines for connecting standard combos or data devices via IOM, or serial SLD and SSI interfaces. The strobe signals and the switching of B channels is programmable.
Line Card Application

An example of the use of the ICC on an **ISDN LT + ET line card** (decentralized architecture) is shown in **figure 4**.

The transceivers (ISDN Cancellation Circuit IEC: PEB 2090) are connected to an Extended PCM Interface Controller (EPIC® PEB 2055) via an IOM interface.

This interface carries the control and data for up to eight subscribers using time division multiplexing. The ICCs are connected in parallel on IOM, one ICC per subscriber.

The EPIC performs dynamic B- and D-channel assignment on the PCM highways. Since this component supports four IOM interfaces, up to 32 subscribers may be accommodated.

1.4.2 Other Applications

If programmed in non-ISDN mode, the ICC serial port B operates as an HDLC communication link without IOM frame structure. This allows the use of the ICC as a general purpose communication controller. The valid HDLC data is marked by a strobe signal on serial port B. Examples of the use of the ICC are: X.25 packet controllers, terminal adaptors, and packet transmission e.g. in primary rate/DMI systems.

![Figure 4
ISDN Line Card Implementation](image-url)
1.4.3 Microprocessor Environment

The ICC is especially suitable for cost-sensitive applications with single-chip microcontrollers (e.g. SAB 8048 / 8031 / 8051). However, due to its programmable micro interface and non-critical bus timing, it fits perfectly into almost any 8-bit microprocessor system environment. The microcontroller interface can be selected to be either of the Motorola type (with control signals CS, R/W, DS) of the Siemens/Intel non-multiplexed bus type (with control signals CS, WR, RD) or of the Siemens/Intel multiplexed address/data bus type (CS, WR, RD, ALE).

**Figure 5**
Example of ICC Microcontroller Environment
2 Functional Description

2.1 General Functions and Device Architecture

Figure 6
Architecture of the ICC
The functional block diagram in **figure 6** shows the ICC to consist of:

- serial interface logic for the IOM and the SLD and SSI interfaces, with B-channel switching capabilities
- logic necessary to handle the D-channel messages (layer 2)

The latter consists of an HDLC receiver and an HDLC transmitter together with 64-byte deep FIFO’s for efficient transfer of the messages to/from the user’s CPU.

In a special HDLC controller operating mode, the auto mode, the ICC processes protocol handshakes (I and S frames) of the LAPD (Link Access Procedure on the D channel) autonomously.

Control and MONITOR functions as well as data transfers between the user’s CPU and the D and B channel are performed by the 8-bit parallel \( \mu \)P interface logic.

The IOM interface allows interaction between layer-1 and layer-2 functions. It implements D-channel collision resolution for connecting other layer-2 devices to the IOM interface, and the C/I and MONITOR channel protocols (IOM-1/IOM-2) to control peripheral devices. This function is called TIC-Bus-Access-Procedure.

The timing unit is responsible for the system clock and frame synchronization.

### 2.2 Serial Interface Modes

The PEB 2070 can be used in different modes of operation:

- **IOM-1 Mode**
- **IOM-2 Mode**
- **HDLC Controller Mode**.

These modes are selected via bit IMS (Interface Mode Select) in ADF2 register and bits DIM2-0 (Digital Interface Mode) in MODE register. **See table 1.**

<table>
<thead>
<tr>
<th>IMS</th>
<th>DIM2</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>IOM-1 Mode</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>HDLC Mode</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>IOM-2 Mode</td>
</tr>
</tbody>
</table>
2.2.1 IOM®-1 Mode (IMS = 0, DIM2 = 0)
Serial port B is used as the IOM-1 interface, which connects the ICC to layer-1 component. The HDLC controller is always connected to the D channel of the IOM-1 interface.
Two additional serial interfaces are available in this mode, the Synchronous Serial Interface SSI (Serial Port A) and the Subscriber Line Datalink (SLD) interface.
The SSI is used especially in ISDN terminal applications for the connection of B-channel sources/sinks. It is available if timing mode 0 (Bit SPM = 0, SPCR register) is programmed.
The SLD is used:
- in ISDN terminal applications for the connection of SLD compatible B-channel devices
- in line card applications for the connection of a peripheral line board controller (e.g. PEB 2050).
The connections of the serial interfaces in both terminal and exchange applications are shown in figure 7.
The SSI interface is only available in timing mode 0 (SPM = 0). Timing mode 1 (SPM = 1) is only applicable in exchange applications figure 7b and is used to minimize the B channel round-trip delay time for the SLD interface. Refer to section 2.3.2.
Figure 7
ICC Interfaces in IOM®-1 Mode
The characteristics of the IOM interface are determined by bits DIM1, 0 as shown in table 2.

Table 2
IOM®-1 Interface Mode Characteristics

<table>
<thead>
<tr>
<th>DIM1</th>
<th>DIM0</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>MONITOR channel upstream is used for TIC bus access.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>MONITOR channel upstream is used for TIC bus access. Bit 3 of MONITOR channel downstream is evaluated to control D-channel transmission.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>MONITOR channel is used for TIC bus access and for data transfer.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>MONITOR channel is used for TIC bus access, for data transfer and for D-channel access control.</td>
</tr>
</tbody>
</table>

2.2.2 IOM®-2 Mode (IMS = 1)

Serial port B is operated as an IOM-2 interface for the connection of layer-1 devices, and as a general purpose backplane bus in terminal equipment. The auxiliary serial SSI and SLD interfaces are not available in this case.

The functions carried out by the IOM are determined by bits SPCR:SPM (terminal mode/non-terminal mode) and DIM2-0, as shown in table 3.

Table 3
IOM®-2 Interface Mode Characteristics

<table>
<thead>
<tr>
<th>HDLC in D channel:</th>
<th>DIM2</th>
<th>DIM1</th>
<th>DIM0</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Last octet of IOM channel 2 is used for TIC bus access. Applicable in terminal mode (SPM = 0).</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Last octet of IOM channel 2 is used for TIC bus access, bit 5 of last octet is evaluated to control D-channel transmission. Applicable in terminal mode (SPM = 0).</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>No TIC bus access and no S bus D-channel access control. Applicable in terminal and non-terminal mode.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Bit 5 of last octet is evaluated to control D-channel transmission. Applicable in terminal mode (SPM = 0).</td>
</tr>
<tr>
<td>HDLC in B or IC channel:</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>No transmission/reception in D channel. HDLC channel selected by ADF2:D1C2-0.</td>
</tr>
</tbody>
</table>

HDLC in B or IC channel:

<table>
<thead>
<tr>
<th>HDLC in B or IC channel:</th>
<th>DIM2</th>
<th>DIM1</th>
<th>DIM0</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>No transmission/reception in D channel. HDLC channel selected by ADF2:D1C2-0.</td>
</tr>
</tbody>
</table>
Note: In IOM-2 terminal mode (SPM = 0, 12-byte IOM-2 frame), all DIM2 – 0 combinations are meaningful. When IOM-2 non-terminal mode is programmed (SPM = 1), the only meaningful combination is “10”.

2.2.3 HDLC Controller Mode (IMS = 0, DIM2 = 1)
In this case serial port B has no fixed frame structure, but is used as a serial HDLC port. The valid HDLC data is marked by a strobe signal input via pin FSC. The data rate is determined by the clock input DLC (maximum 4096 Mbit/s). The characteristic of the serial port B are determined by bits DIM1, 0 as shown in table 4.

Table 4
HDLC Mode Characteristics

<table>
<thead>
<tr>
<th>DIM1</th>
<th>DIM0</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>reserved</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>FSC strobe active low</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>FSC strobe active high</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>FSC strobe ignored</td>
</tr>
</tbody>
</table>

2.3 Interfaces
The ICC serves three different user-oriented interface types:
– parallel processor interface to higher layer functions
– IOM interface: between layer 1 and 2, and as a universal backplane for terminals
– SSI and SLD interfaces for B-channel sources and destinations (in IOM-1 mode only).
2.3.1 \(\mu\)P Interface

The ICC is programmed via an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 13 (18) lines and is directly compatible with multiplexed and non-multiplexed microcontroller interfaces (Siemens/Intel or Motorola type buses). The microprocessor interface signals are summarized in Table 5.

Table 5
Interface of the ICC

<table>
<thead>
<tr>
<th>Pin No. P-DIP</th>
<th>Pin No. P-LCC</th>
<th>Symbol</th>
<th>Input (I) Output (O)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>25</td>
<td>AD0/D0</td>
<td>I/O</td>
<td>Multiplexed Bus Mode: Address/ Data bus. Transfers addresses from the (\mu)P system to the ICC and data between the (\mu)P system and the ICC.</td>
</tr>
<tr>
<td>22</td>
<td>26</td>
<td>AD1/D1</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>27</td>
<td>AD2/D2</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>28</td>
<td>AD3/D3</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>AD4/D4</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>AD5/D5</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>AD6/D6</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>AD7/D7</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>21</td>
<td>CS</td>
<td>I</td>
<td>Chip Select. A 0 “low” on this line selects the ICC for read/write operation.</td>
</tr>
<tr>
<td>–</td>
<td>23</td>
<td>R/W</td>
<td>I</td>
<td>Read/Write. At 1 “high”, identifies a valid (\mu)P access as a read operation. At 0, identifies a valid (\mu)P access as a write operation (Motorola bus mode).</td>
</tr>
<tr>
<td>19</td>
<td>23</td>
<td>WR</td>
<td>I</td>
<td>Write. This signal indicates a write operation (Siemens/Intel bus mode).</td>
</tr>
<tr>
<td>–</td>
<td>24</td>
<td>DS</td>
<td>I</td>
<td>Data Strobe. The rising edge marks the end of a valid read or write operation (Motorola bus mode).</td>
</tr>
<tr>
<td>20</td>
<td>24</td>
<td>RD</td>
<td>I</td>
<td>Read. This signal indicates a read operation (Siemens/Intel bus mode).</td>
</tr>
</tbody>
</table>

Multiplexed Bus Mode: Address/Data bus. Transfers addresses from the \(\mu\)P system to the ICC and data between the \(\mu\)P system and the ICC.

Non Multiplexed Bus Mode: Data bus. Transfers data between the \(\mu\)P system and the ICC.
Interface of the ICC (cont’d)

<table>
<thead>
<tr>
<th>Pin No. P-DIP</th>
<th>Pin No. P-LCC</th>
<th>Symbol</th>
<th>Input (I) Output (O)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>18</td>
<td>INT</td>
<td>OD</td>
<td>Interrupt Request. The signal is activated when the ICC requests an interrupt. It is an open drain output.</td>
</tr>
<tr>
<td>16</td>
<td>20</td>
<td>ALE</td>
<td>I</td>
<td>Address Latch Enable. A high on this line indicates an address on the external address bus (Multiplexed bus typ only).</td>
</tr>
<tr>
<td>19</td>
<td>A0</td>
<td>I</td>
<td>Address bit 0 (Non-multiplexed bus type).</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>A1</td>
<td>I</td>
<td>Address bit 1 (Non-multiplexed bus type).</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>A2</td>
<td>I</td>
<td>Address bit 2 (Non-multiplexed bus type).</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>A3</td>
<td>I</td>
<td>Address bit 3 (Non-multiplexed bus type).</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>A4</td>
<td>I</td>
<td>Address bit 4 (Non-multiplexed bus type).</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>A5</td>
<td>I</td>
<td>Address bit 5 (Non-multiplexed bus type).</td>
<td></td>
</tr>
</tbody>
</table>

2.3.2 ISDN Oriented Modular (IOM®) Interface

IOM®-1

This interface consists of one data line per direction (IOM Data Ports 0 and 1: IDP0,1). Three additional signals define the data clock (DCL) and the frame synchronization (FSC/FSD) at this interface. The data clock has a frequency of 512 kHz (twice the data rate) and the frame sync clock has a repetition rate of 8 kHz.

Via this interface four octets are transmitted per 125 μs frame (figure 8):
- The first two octets constitute the two 64 kbit/s B channels.
- The third octet is the MONITOR channel. It is used for the exchange of data using the IOM-1 MONITOR channel protocol which involves the E bit as a validation bit. In addition, it carries a bit which enables/inhibits the transmission of HDLC frames (IDP0) and it serves to arbitrate the access to the last octet. (IDP1).
- The fourth octet is called the Telecom IC (TIC) bus because of the offered busing capability. It is constituted of the 16 kbit/s D channel (2 bits), a four-bit Command/Indication channel and the T and E bits. The C/I channel serves to control and MONITOR layer-1 functions (e.g. activation/deactivation of a transmission line...). The T bit is a transparent 8-kbit/s channel which can be accessed from the ICC, and the E bit is used in MONITOR byte transfer.
Figure 8
IOM®-1 Frame Structure

**TIC Bus and Arbitration via MONITOR Channel**

The arbitration mechanism implemented in the MONITOR channel allows the access of more than one (up to eight) ICC to the last octet of IOM (TIC). This capability is useful for the modular implementation of different ISDN services (different Service Access Points) e.g. in ISDN voice/data terminals. The IDP1 pins are connected together in a wired-or configuration, as shown in figure 9.
The arbitration mechanism is described in the following.

An access request to the TIC bus may either be generated by software (μP access to the C/I channel) or by the ICC itself (transmission of an HDLC frame). A software access request to the bus is effected by setting the BAC bit (CIXR/CIX0 register) to “1”.

Figure 9
IOM® Bus (TIC Bus) Configuration
In the case of an access request, the ICC checks the bus accessed-bit (bit 3 of IDP1 MONITOR octet) for the status “bus free”, which is indicated by a logical “1”. If the bus is free, the ICC transmits its individual TIC bus address programmed in STCR register. The TIC bus is occupied by the device which is able to send its address error-free. If more than one device attempt to seize the bus simultaneously, the one with the lowest address value wins.

**MONITOR Channel Structure on IDP1**

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

- **TIC Bus Address TBA2-0**
- Bus accessed = “1” (no TIC bus access) if
- BAC = 0 (CIXR/CIX0 register) and
- no HDLC transmission is in progress

When the TIC bus is seized by the ICC, the bus is identified to other devices as occupied via the IDP1 MONITOR channel bus accessed bit state “0” until the access request is withdrawn. After a successful bus access, the ICC is automatically set into a lower priority class, that is, a new bus access cannot be performed until the status “bus free” is indicated in two successive frames.

If none of the devices connected to the IOM interface request access to the D and C/I channels, the TIC bus address 7 will be present. The device with this address will therefore have access, by default, to the D and C/I channels.

**Note:** Bit BAC (CIXR/CIX0 register) should be reset by the µP when access to the C/I channel is no more requested, to grant other devices access to these channels.
MONITOR Channel

The MONITOR channel protocol for data transfer is described in section 2.4.5.

When the ICC is used in connection with an S interface layer-1 transceiver, an indication must be given to the ICC whether the D channel is available for transmission (TE applications with short passive or extended bus configuration).

This indication is assumed to be given in bit 3 “Stop/Go” (S/G) of the MONITOR input channel on IDP0. When a HDLC frame is to be transmitted in the D channel, the ICC automatically starts, proceeds with, or stops frame transmission according to the S/G bit value:

S/G = 1 : stop
S/G = 0 : go

MONITOR Channel Structure IDP0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>S/G</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IOM®-1 Timing

In IOM-1 mode, the ICC may be operated either in timing mode 0 or timing mode 1. The selection is via bit SPM in SPCR register.

Timing mode 0 (SPM = 0) is used in terminal applications. Timing mode 1 (SPM = 1) is only meaningful in exchange applications when the SLD is used. Programming timing mode 1 minimizes the B-channel round-trip delay time on the SLD interface.

In timing mode 0 the IOM frame begin is marked by a rising edge on the FSC input. It simultaneously marks the beginning of the SLD frame.

In timing mode 1 the IOM frame begins is marked by a rising edge on FSD output. The FSD output is delayed by the ICC by 1/8 th of a frame with respect to FSC (figure 10).
Figure 10
Interface Timing in IOM®-1 Mode

Note: The up-arrows show the position, where register contents are transferred to the sender, the down-arrows show the position, where the receiver transfers data to the registers.
IOM®-2

The IOM-2 is a generalization and enhancement of the IOM-1. While the basic frame structure is very similar, IOM-2 offers further capacity for the transfer of maintenance information. In terminal applications, the IOM-2 constitutes a powerful backplane bus offering intercommunication and sophisticated control capabilities for peripheral modules.

The channel structure of the IOM-2 is depicted below.

Channel Structure of the IOM®-2

<table>
<thead>
<tr>
<th>B1</th>
<th>B2</th>
<th>MONITOR</th>
<th>D</th>
<th>C/I</th>
<th>MR</th>
<th>MX</th>
</tr>
</thead>
</table>

- The first two octets constitute the two 64 kbit/s B channels.
- The third octet is the MONITOR channel. It is used for the exchange of data between the ICC and the other attached device(s) using the IOM-2 MONITOR channel protocol.
- The fourth octet (control channel) contains
  - two bits for the 16 kbit/s D channel
  - a four-bit Command/Indication channel
  - two bits MR and MX for supporting the MONITOR channel protocol.

In the case of an IOM-2 interface the frame structure depends on whether TE- or non-TE mode is selected, via bit SPM in SPCR register.

Non-TE Timing Mode (SPM = 1)

In this case the frame is a multiplex of eight IOM-2 channels (figure 11), each channel has the same structure.

Thus the data rate per subscriber connection (corresponding to one channel) is 256 kbit/s, whereas the bit rate is 2048 kbit/s. The IOM-2 interface signals are:

| IDP0,1 | 2048 kbit/s |
| DCL | 4096 kHz input |
| FSC | 8 kHz input |
The ICC is assigned to one of the eight channels (0 to 7) via register programming. This mode is used in ISDN exchange/line card applications.

**TE Timing Mode (SPM = 0)**

The frame is composed of three channels (figure 11):

- Channel 0 contains 144 kbit/s (for 2B + D) plus MONITOR and command/indication channels for layer-1 devices.

- Channel 1 contains two 64-kbit/s intercommunication channels plus MONITOR and command/indication channels for other IOM-2 devices.

- Channel 2 is used for enabling/inhibiting the transmission of HDLC frames. This bit is typically generated by an S-bus transceiver (stop/go: bit 5, or 3rd MSB of the last octet on IDP0). On IDP1, bits 2 to 5 of the last octet are used for TIC bus access arbitration.

As in the IOM-1 case (figure 9), up to eight ICCs can access the TIC bus (D and C/I channels). The bus arbitration mechanism is identical to that described previously, except that it involves bits 2 to 5 in channel 2.
Functional Description

2.3.3 SSI (Serial Port A)

The SSI (Serial Synchronous Interface) is available in IOM-1 interface mode. Timing mode 0 (SPM = 0) has to be programmed.

The serial port SSI has a data rate of 128 kbit/s. It offers a full duplex link for B channels in ISDN voice/data terminals. Examples: serial synchronous transceiver devices (USART’s, HSCX SAB 82525, ITAC PSB 2110, …), and CODEC filters.

The port consists of one data line in each direction (SDAX and SDAR) and the 128-kHz clock output (SCA). The beginning of B2 is marked by a rising edge on FSC, see figure 12.

The µC system has access to B-channel data via the ICC registers BCR1/2 and BCX1/2.

The µC access must be synchronized to the serial transmission by means of the Synchronous Transfer Interrupt (STCR see chapter 4).

---

**Figure 12**

**Definition of the IOM®-2 Channels in Terminal Timing Mode**

The IOM-2 signals are:

- **IDP0,1**: 768 kbit/s
- **DCL**: 1536 kHz input
- **FSC**: 8 kHz input.

In addition, to support standard combos/data devices the following signals are generated as outputs:

- **SDS1/2**: 8 kHz programmable data strobe signals for selecting one or both B/IC channel(s).
2.3.4 SLD
The SLD is available in IOM-1 interface mode.

Figure 13
SSI (a) and SLD (b) Interface Lines
The standard SLD interface is a three-wire interface with a 512-kHz clock input (DCL), an 8-kHz frame direction signal input (FSC), and a serial ping-pong data lead (SIP) with an effective full duplex data rate of 256 kbit/s.

The frame is composed of four octets per direction. Octets 1 and 2 contain the two B channels, octet 3 is a feature control byte, and octet 4 is a signaling byte (figure 13).

The SLD interface can be used in:
- **Terminal applications** as a full duplex time-multiplexed (ping-pong) connection to B-channel sources/destinations. CODEC filters, such as the SICOFI® (PEB 2060) or the ARCOFI® (PSB 2160) as well as other SLD compatible voice/data modules may be connected directly to the ICC as depicted in figure 13a. Terminal specific functions have to be deselected (TSF = 0), so that pin SIP/EAW takes on its proper function as SLD data line. Moreover, in TE applications timing mode 0 has to be programmed.
- **Digital exchange applications** as a full duplex time-multiplexed connection to convey the B channels between the layer-1 devices and a Peripheral Board Controller (e.g. PBC PEB 2050 or PIC PEB 2052), which performs time-slot assignment on the PCM highways, forming a system interface to a switching network (figure 13b).

Timing mode 1 (SPM = 1) can be programmed in order to minimize the B-channel round-trip delay.

The µC system has access to B-channel data, the feature control byte and the signaling byte via the ICC registers:

- C1R, C2R → B1/B2
- CF CR and SFCX → FC
- SSCR and SSCX → SIG

The µP access to C1R, C2R, SFCR, SFCX, SSCR and SSCX must be synchronized to the serial transmission by means of the Synchronous Transfer Interrupt (STCR) and the BVS-bit (STAR).

### 2.4 Individual Functions

#### 2.4.1 Layer-2 Functions for HDLC

The HDLC controller in the ICC is responsible for the data link layer using HDLC/SDLC based protocols.

The ICC can be made to support that data link layer to a degree that best suits system requirements. When programmed in auto mode, it handles elements of procedure of an acknowledged, balanced class of HDLC protocol autonomously (window size equal to “1”). Multiple links may be handled simultaneously due to the address recognition capabilities, as explained in section 2.4.1.1.

The ICC supports point-to-point protocols such as LAPB (Link Access Procedure Balanced) used in X.25 networking.

For ISDN, one particularly important protocol is the **Link Access Procedure for the D channel** (LAPD).
LAPD, layer 2 of the ISDN D-channel protocol (CCITT I.441) includes functions for:

- Provision of one or more data link connections on a D channel (multiple LAP). Discrimination between the data link connections is performed by means of a data link connection identifier (DLCI = SAPI + TEI)
- HDLC-framing
- Application of a balanced class of procedure in point-multipoint configuration.

The simplified block diagram in figure 6 shows the functional blocks of the ICC which support the LAPD protocol.

The HDLC transceiver in the ICC performs the framing functions used in HDLC/SDLC based communication: flag generation/recognition, bit stuffing, CRC check and address recognition.

The FIFO structure with two 64-byte pools for transmit and receive directions and an intelligent FIFO controller permit flexible transfer of protocol data units to and from the µC system.

2.4.1.1 Message Transfer Modes

The HDLC controller can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be programmed in a flexible way, to satisfy different system requirements.

In the auto mode the ICC handles elements of procedure of the LAPD (S and I frames) according to CCITT I.441 fully autonomously.

For the address recognition the ICC contains four programmable registers for individual SAPI and TEI values SAP1-2 and TEI1-2, plus two fixed values for “group” SAPI and TEI, SAPG and TEIG.

There are 5 different operating modes which can be set via the MODE register:

**Auto mode** (MDS2, MDS1 = 00)

Characteristics:

- Full address recognition (1 or 2 bytes).
- Normal (mod 8) or extended (mod 128) control field format
- Automatic processing of numbered frames of an HDLC procedure (see 2.4.1.2).

If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FC8 (group address) as well as with two individually programmable values in SAP1 and SAP2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R) dependent on the setting of the CRI bit in SAP1, and will be excluded from the address comparison.

Similarly, the low address byte is compared with the fixed value FFH (group TEI) and two compare values programmed in special registers (TEI1, TEI2). A valid address will be recognized in case the high and low byte of the address field match one of the compare values. The ICC can be called (addressed) with the following address combinations:
– SAP1/TEI1
– SAP1/FF\textsubscript{H}
– SAP2/TEI2
– SAP2/FF\textsubscript{H}
– FE\textsubscript{H}(FC\textsubscript{H})/TEI1
– FE\textsubscript{H}(FC\textsubscript{H})/TEI2
– FE\textsubscript{H}(FC\textsubscript{H})/FF\textsubscript{H}

Only the logical connection identified through the address combination SAP1, TEI1 will be processed in the auto mode, all others are handled as in the non-auto mode. The logical connection handled in the auto mode must have a window size 1 between transmitted and acknowledged frames. HDLC frames with address fields that do not match with any of the address combinations, are ignored by the ICC.

In case of a 1-byte address, TEI1 and TEI2 will be used as compare registers. According to the X.25 LAPB protocol, the value in TEI1 will be interpreted as COMMAND and the value in TEI2 as RESPONSE.

The control field is stored in RHCR register and the I field in RFIFO. Additional information is available in RSTA.

**Non-Auto Mode** (MDS2, MDS1 = 01)

Characteristics: Full address recognition (1 or 2 bytes)
Arbitrary window sizes

All frames with valid addresses (address recognition identical to auto mode) are accepted and the bytes following the address are transferred to the \( \mu \)P via RHCR and RFIFO. Additional information is available in RSTA.

**Transparent Mode 1** (MDS2, MDS1, MDS0 = 101).

Characteristics: TEI recognition

A comparison is performed only on the second byte after the opening flag, with TEI1, TEI2 and group TEI (FF\textsubscript{H}). In case of a match, the first address byte is stored in SAPR, the (first byte of the) control field RHCR, and the rest of the frame in the RFIFO. Additional information is available in RSTA.
**Transparent Mode 2** (MDS2, MDS1, MDS0 = 110).
Characteristics: non address recognition.
Every received frame is stored in RFIFO (first byte after opening flag to CRC field). Additional information can be read from RSTA.

**Transparent Mode 3** (MDS2, MDS1, MDS0 = 111)
Characteristics: SAPI recognition
A comparison is performed on the first byte after the opening flag with SAP1, SAP2 and group SAPI (FE/FCH). In the case of a match, all the following bytes are stored in RFIFO. Additional information can be read from RSTA.

**2.4.1.2 Protocol Operations (auto mode)**
In addition to address recognition all S and I frames are processed in hardware in the auto mode. The following functions are performed:

- update of transmit and receive counter
- evaluation of transmit and receive counter
- processing of S commands
- flow control with RR/RNR
- response generation
- recognition of protocol errors
- transmission of S commands, if an acknowledgment is not received
- continuous status query of remote station after RNR has been received
- programmable timer/repeater functions.

The processing of frames in auto mode is described in detail in section 2.4.8.
2.4.1.3 Reception of Frames

A 2x32-byte FIFO buffer (receive pools) is provided in the receive direction.

The control of the data transfer between the CPU and the ICC is handled via interrupts.

There are two different interrupt indications concerned with the reception of data:

– RPF (Receive Pool Full) interrupt, indicating that a 32-byte block of data can be read from the RFIFO and the received message is not yet complete.

– RME (Receive Message End) interrupt, indicating that the reception of one message is completed, i.e. either
  - one message ≤ 32 bytes, or
  - the last part of a message ≥ 32 bytes
  is stored in the RFIFO.

Depending on the message transfer mode the address and control fields of received frames are processed and stored in the receive FIFO or in special registers as depicted in figure 14.

The organization of the RFIFO is such that, in the case of short (≤ 32 bytes), successive messages, up to two messages with all additional information can be stored. The contents of the RFIFO would be, for example, as shown in figure 15.

---

**Figure 14**
Contents of RFIFO (short message)
**Figure 15**
**Receive Data Flow**

**Note 1**  Only if a 2-byte address field is defined (MDS0 = 1 in MODE register).

**Note 2**  Comparison with Group TEI (FF) is only made if a 2-byte address field is defined (MDS0 = 1 in MODE register).

**Note 3**  In the case of an extended, modulo 128 control field format (MCS = 1 in SAP2 register) the control field is stored in RHCR in compressed form (I frames).

**Note 4**  In the case of extended control field, only the first byte is stored in RHCR, the second in RFIFO.

---

**Table: Receive Data Flow**

<table>
<thead>
<tr>
<th>Flag</th>
<th>Address High</th>
<th>Address Low</th>
<th>Control</th>
<th>Information</th>
<th>CRC</th>
<th>Flag</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SAP1,SAP2</td>
<td>TE1,TE12</td>
<td>RHCR</td>
<td>RFIFO</td>
<td>RSTA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FE,FC</td>
<td>FF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Note 1) Checked automatically by ICC

(Note 2) Compared with register or fixed value

(Note 3) Stored into register or RFIFO

(Note 4)
When 32 bytes of a message longer than that are stored in RFIFO, the CPU is prompted to read out the data by an RPF interrupt. The CPU must handle this interrupt before more than 32 additional bytes are received, which would cause a “data overflow” (figure 16). This corresponds to a maximum CPU reaction time of 16 ms (data rate 16 kbit/s).

After a remaining block of less than or equal to 16 bytes has been stored, it is possible to store the first 16 bytes of a new message (see figure 16b).

The internal memory is now full. The arrival of additional bytes will result in “data overflow” and a third new message in “frame overflow”.

The generated interrupts are inserted together with all additional information into a wait line to be individually passed to the CPU.

After an RPF or RME interrupt has been processed, i.e. the received data has been read from the RFIFO, this must be explicitly acknowledged by the CPU issuing a RMC (Receive Message Complete) command.

The ICC can then release the associated FIFO pool for new data. If there is an additional interrupt in the wait line it will be generated after the RMC acknowledgment.
Figure 16
Contents of RIFIFO (long message)

Information about the received frame is available for the µP when the RME interrupt is generated, as shown in table 6.
### Functional Description

#### Table 6
Receive Information at RME Interrupt

<table>
<thead>
<tr>
<th>Information</th>
<th>Register</th>
<th>Bit</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>First byte after flag (SAPI of LAPD address field)</td>
<td>SAPR</td>
<td>–</td>
<td>Transparent mode 1</td>
</tr>
<tr>
<td>Control field</td>
<td>RHCR</td>
<td>–</td>
<td>Auto mode, I (modulo 8) and U frames</td>
</tr>
<tr>
<td>Compressed control field</td>
<td>RHCR</td>
<td>–</td>
<td>Auto mode, I frames (modulo 128)</td>
</tr>
<tr>
<td>2(^{nd}) byte after flag</td>
<td>RHCR</td>
<td>–</td>
<td>Non-auto mode, 1-byte address field</td>
</tr>
<tr>
<td>3(^{rd}) byte after flag</td>
<td>RHCR</td>
<td>–</td>
<td>Non-auto mode, 2-byte address field</td>
</tr>
<tr>
<td>Type of frame (Command/Response)</td>
<td>STAR</td>
<td>C/R</td>
<td>Auto mode, 2-byte address field</td>
</tr>
<tr>
<td>Recognition of SAPI</td>
<td>STAR</td>
<td>SA1-0</td>
<td>Non-auto mode, 2-byte address field</td>
</tr>
<tr>
<td>Recognition of TEI</td>
<td>STAR</td>
<td>TA</td>
<td>All expect Transparent mode 2,3</td>
</tr>
<tr>
<td>Result of CRC check (correct/incorrect)</td>
<td>STAR</td>
<td>CRC</td>
<td>ALL</td>
</tr>
<tr>
<td>Data available in RFIFO (yes/no)</td>
<td>STAR</td>
<td>RDA</td>
<td>ALL</td>
</tr>
<tr>
<td>Abort condition detected (yes/no)</td>
<td>STAR</td>
<td>RAB</td>
<td>ALL</td>
</tr>
<tr>
<td>Data overflow during reception of a frame (yes/no)</td>
<td>STAR</td>
<td>RDO</td>
<td>ALL</td>
</tr>
<tr>
<td>Number of bytes received in RFIFO</td>
<td>RBCL</td>
<td>RBC4-0</td>
<td>ALL</td>
</tr>
<tr>
<td>Message length</td>
<td>RBCL</td>
<td>RBC11-50V</td>
<td>ALL</td>
</tr>
</tbody>
</table>
2.4.1.4 Transmission of Frames

A 2x32 byte FIFO buffer (transmit pools) is provided in the transmit direction.

If the transmit pool is ready (which is true after an XPR interrupt or if the XFW bit in STAR is set), the CPU can write a data block of up to 32 bytes to the transmit FIFO. After this, data transmission can be initiated by command.

Two different frame types can be transmitted:
- Transparent frames (command: XTF), or
- I frames (command: XIF)

as shown in figure 17.

![Figure 17: Transmit Data Flow](image-url)

**Description of Symbols:**
- ![ ] → Generated automatically by ICC
- ![ ] → Written initially by CPU (into register)
- ![ ] → Loaded (repeatedly) by CPU upon ICC request (XPR interrupt)
For transparent frames, the whole frame including address and control field must be written to the XFIFO.

The transmission of I frames is possible only if the ICC is operating in the auto mode. The address and control field is autonomously generated by the ICC and appended to the frame, only the data in the information field must be written to the XFIFO.

If a 2-byte address field has been selected, the ICC takes the contents of the XAD 1 register to build the high byte of the address field, and the contents of the XAD 2 register to build the low byte of the address field.

Additionally the C/R bit (bit 1 of the high byte address, as defined by LAPD protocol) is set to “1” or “0” dependent on whether the frame is a command or a response.

In the case of a 1-byte address, the ICC takes either the XAD 1 or XAD 2 register to differentiate between command or response frame (as defined by X.25 LAP B).

The control field is also generated by the ICC including the receive and send sequence number and the poll/final (P/F) bit. For this purpose, the ICC internally manages send and receive sequence number counters.

In the auto mode, S frames are sent autonomously by the ICC. The transmission of U frames, however, must be done by the CPU. U frames must be sent as transparent frames (XTF), i.e. address and control field must be defined by the CPU.

Once the data transmission has been initiated by command (XTF or XIF), the data transfer between CPU and ICC is controlled by interrupts.

The ICC repeatedly requests another data packet or block by means of an XPR interrupt, every time no more than 32 bytes are stored in the XFIFO.

The processor can then write further data to the XFIFO and enable the continuation of frame transmission by issuing an XIF/XTF command.

If the data block which has been written last to the XFIFO completes the current frame, this must be indicated additionally by setting the XME (Transmit Message End) command bit. The ICC then terminates the frame properly by appending the CRC and closing flag.

If the CPU fails to respond to an XPR interrupt within the given reaction time, a data underrun condition occurs (XFIFO holds no further valid data). In this case, the ICC automatically aborts the current frame by sending seven consecutive “ones” (ABORT sequence).

The CPU is informed about this via an XDU (Transmit Data Underrun) interrupt.

It is also possible to abort a message by software by issuing an XRES (Transmitter RESet) command, which causes an XPR interrupt.

After an end of message indication from the CPU (XME command), the termination of the transmission operation is indicated differently, depending on the selected message transfer mode and the transmitted frame type.

If the ICC is operating in the auto mode, the window size (= number of outstanding unacknowledged frames) is limited to 1; therefore an acknowledgment is expected for every I frame sent with an XIF command. The acknowledgment may be provided either by a received S or I frame with corresponding receive sequence number (see figure 14).
If no acknowledgment is received within a certain time (programmable), the ICC requests an acknowledgment by sending an S frame with the poll bit set (P = 1) (RR or RNR). If no response is received again, this process is repeated in total CNT times (retry count, programmable via TIMR register).

The termination of the transmission operation may be indicated either with:

- XPR interrupt, if a positive acknowledgment has been received,
- XMR interrupt, if a negative acknowledgment has been received, i.e. the transmitted message must be repeated (XMR = Transmit Message Repeat),
- TIN interrupt, if no acknowledgment has been received at all after CNT times the expiration of the time period $t_1$ (TIN = Timer INterrupt, XPR interrupt is issued additionally).

**Note:** Prerequisite for sending I frames in the auto mode (XIF) is that the internal operational mode of the timer has been selected in the MODE register (TMD bit = 1).

The transparent transmission of frames (XTF command) is possible in all message transfer modes. The successful termination of a transparent transmission is indicated by the XPR interrupt.

In the case where an IOM interface mode is programmed (see section 2.2), a transmission may be aborted from the outside by setting the stop/go bit to 1, provided DIM1 - 0 are programmed appropriately, see tables 2 and 3. An example of this is the occurrence of an S bus D-channel collision. - If this happens before the first FIFO pool has been completely transmitted and released, the ICC will retransmit the frame automatically as soon as transmission is enabled again. Thus no µP interaction is required.

On the other hand, if a transmission is inhibited by the stop/go bit after the first pool has already been released (and XPR generated), the ICC aborts the frame and requests the processor to repeat the frame with an XMR interrupt.
2.4.2 B-Channel Switching (IOM®-1)

The ICC contains two serial interfaces, SLD and SSI, which can serve as interfaces to B-channel sources/destinations. Both channels B1 and B2 can be switched independently of one another to the IOM interface (figure 18).

The following possibilities are provided:

- Switching from/to SSI
- Switching from/to SLD
- IOM looping
- SLD looping

The microcontroller can select the B-channel switching in the SPCR register. In figure 19 all possible selections of the B-channel routes and access to B-channel data via the microprocessor interface are illustrated. This access from the microcontroller is possible by writing or reading the C1R/C2R register or reading the B1CR/B2CR register (cf. Synchronous Transfer, paragraph 2.4.3).

Figure 18
**Figure 19**

- B1 = FF_H
- B2 = Undefined Value

**Diagram Notes:**
- **FF_H**
- **μP Access**
- **B-Channel Route**
- **IOM Loop**

---

**Legend:**
- SSI: Switching
- SLD: Loop
- IOM: IOM®
- **μP:** Access
- **B-Channel Route**
2.4.3 Access to B / IC Channels

IOM®-1 mode (IMS = 0)

The B1 and/or B2 channel is accessed by reading the B1CR/B2CR or by reading and writing the C1R/C2R registers. The µP access can be synchronized to the serial interface by means of a Synchronous Transfer programmed in the STCR register.

The read/write access possibilities are shown in table 7.

Table 7

<table>
<thead>
<tr>
<th>C_C1</th>
<th>C_C0</th>
<th>C_R Read</th>
<th>Write</th>
<th>B_CR Read</th>
<th>Application(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>SLD</td>
<td>SLD</td>
<td>IOM</td>
<td>B_not switched, SLD looping</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>SLD</td>
<td>–</td>
<td>IOM</td>
<td>B_switched to/from SLD</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>SSI</td>
<td>–</td>
<td>IOM</td>
<td>B_switched to/from SSI</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>IOM</td>
<td>IOM</td>
<td>–</td>
<td>IOM looping</td>
</tr>
</tbody>
</table>

The Synchronous Transfer Interrupt (SIN, ISTA register) can be programmed to occur at either the beginning of a 125 µs frame or at its center, depending on the channel(s) to be accessed and the current configuration, see figure 20a.
Figure 20a

(a) C_C1, C_C0 = 00
SLD Loop

FSC

BVS

IDP1

SLD

μP Access

μP

OUT

IN

SIN (STO)

ITSO2864
Figure 20b

(b) C_C1, C_C0 = 01
SLD - IOM Connection

µP Access

FSC
BVS
IDP0
SIP
IDP1

SIN (STO)
Figure 20c

(c) C.C1, C.C0 = 10
SSI - IOM® Connection
IOM\textsuperscript{®}-2 mode (IMS = 1)

The B1, B2 and/or IC1, IC2 channels are accessed by reading the B1CR/B2CR or by reading and writing the C1R/C2R registers. The \( \mu \)P access can be synchronized to the IOM interface by means of a Synchronous Transfer programmed in the STCR register.

The read/write access possibilities are shown in table 8.

Table 8

<table>
<thead>
<tr>
<th>C_C1</th>
<th>C_C0</th>
<th>C_R Read</th>
<th>C_R Write</th>
<th>B_CR Read</th>
<th>Output to IOM2</th>
<th>Application(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>IC_</td>
<td>–</td>
<td>B_</td>
<td>–</td>
<td>B_monitoring, IC_monitoring</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>IC_</td>
<td>IC_</td>
<td>B_</td>
<td>IC_</td>
<td>B_monitoring, IC_looping from/to IOM</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>–</td>
<td>B_</td>
<td>B_</td>
<td>B_</td>
<td>B_access from/to IOM; transmission of a constant value in B_channel to IOM.</td>
</tr>
<tr>
<td>1</td>
<td>B_</td>
<td>1</td>
<td>B_</td>
<td>–</td>
<td>B_</td>
<td>B_looping from IOM; transmission of a variable pattern in B_channel to IOM.</td>
</tr>
</tbody>
</table>

The general sequence of operations to access the B/IC channels is:

- (set configuration, register SPCR)
- Program Synchronous Interrupt (ST0)
- Read Register (B_CR, C_R)
- (Write register)
- Acknowledge SIN (SC0)

**Note:** The data transfer itself works independent of the Synchronous Transfer Interrupt. In case of a SOV e.g. transfer is still possible.
2.4.4 C/I Channel Handling

The Command/Indication channel carries real-time status information between the ICC and another device connected to the IOM.

1) One C/I channel conveys the commands and indications between a layer-1 device and a layer-2 device. This channel is available in all timing modes (IOM-1 or IOM-2). It can be accessed from the microcontroller e.g. to control the layer-1 activation/deactivation procedures. Access is arbitrated via the TIC bus access protocol:

   – in IOM-1 mode, this arbitration is done in the MONITOR channel
   – in IOM-2 TE timing mode (SPM = 0), this arbitration is done in C/I channel 2 (see figure 11).

This C/I channel is access via register CIRR/CIR0 (in receive direction layer 1-to-layer 2) and register CIXR/CIX0 (in transmit direction, layer 2-to-layer 1). The code is four bits long.

In the receive direction, the code from layer 1 is continuously monitored, with an interrupt being generated anytime a change occurs. A new code must be found in two consecutive IOM frames to be considered valid and to trigger a C/I code change interrupt status (double last look criterion).

In the transmit direction, the code written in CIXR/CIX0 is continuously transmitted in the channel.

2) A second C/I channel (called C/I1) can be used to convey real time status information between the ICC and various non-layer 1 peripheral devices. The channel consists of six bits in each direction. It is available only in the IOM-2 terminal timing mode (see figure 11).

The C/I1 channel is accessed via registers CIR1 and CIX1. A change in the received C/I1 code is indicated by an interrupt status without double last look criterion.

2.4.5 MONITOR Channel Handling

IOM®-1

The MONITOR channel protocol can be used to exchange one byte of information at a time between the ICC and another device (e.g. layer-1 transceiver).

The procedure is as follows:

MONITOR Transmit Channel (MOX) register is loaded with the value to be sent in the outgoing MONITOR channel. (Bytes of the form FxH are not allowed for this purpose because of the TIC bus collision resolution procedure).
The receiving device interprets the incoming MONITOR value as a control/information byte, FXH excluded. If no response is expected, the procedure is complete. If the receiving device shall react by transmitting information to the ICC, it should set the E bit to 0 and send the response in the MONITOR channel of the following frame. The ICC

- latches the value in the MONITOR channel of the frame immediately following a frame with “E = 0” into MOR register.

- generates a MONITOR Status interrupt MOS (EXIR register) to indicate that the MOR register has been loaded. See figure 21.

**Figure 21**

**IOM®-2**

In this case, the MONITOR channel protocol is a handshake protocol used for high speed information exchange between the ICC and other devices, in MONITOR channel 0 or 1 (see figure 11). In the non-TE mode, only one MONITOR channel is available (“MONITOR channel 0”).

The MONITOR channel protocol is necessary (see figure 22):

- For programming and controlling devices attached to the IOM. Examples of such devices are: layer-1 transceivers (using MONITOR channel 0), and peripheral V/D modules that do not have a parallel microcontroller interface (MONITOR channel 1), such as the Audio Ringing Codec Filter PSB 2160.

- For data exchange between two microcontroller systems attached to two different devices on one IOM-2 backplane. Use of the MONITOR channel avoids the necessity of a dedicated serial communication path between the two systems. This greatly simplifies the system design of terminal equipment (figure 22).
The MONITOR channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the MONITOR Channel Receive (MR0 or 1) and MONITOR Channel Transmit (MX0 or 1) bits. For example: data is placed onto the MONITOR channel and the MX bit is activated. This data will be transmitted repeatedly once per 8-kHz frame until the transfer is acknowledged via the MR bit.

The microprocessor may either enforce a “1” (idle) in MR, MX by setting the control bit MRC1,0 or MXC1,0 to “0” (MONITOR Control Register MOCR), or enable the control of these bits internally by the ICC according to the MONITOR channel protocol. Thus, before a data exchange can begin, the control bit MRC(1,0), or MXC(1,0) should be set to “1” by the microprocessor.

The MONITOR channel protocol is illustrated in figure 23. Since the protocol is identical in MONITOR channel 0 and MONITOR channel 1 (available in TE mode only), the index 0 or 1 has been left out in the illustration.

The relevant status bits are:
- MONITOR Channel Data Received MDR (MDR0, MDR1)
- MONITOR Channel End of Reception MER (MER0, MER1) for the reception of MONITOR data, and
- MONITOR Channel Data Acknowledged MDA (MDA0, MDA1)
- MONITOR Channel Data Abort MAB (MAB0, MAB1) for the transmission of MONITOR data (Register: MOSR).
In addition, the status bit:
MONITOR Channel Active MAC (MAC0, MAC1)
indicates whether a transmission is in progress (Register: STAR).

Before starting a transmission, the microprocessor should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by an “0” in the MONITOR Channel Active MAC status bit.

After having written the MONITOR Data Transmit (MOX) register, the microprocessor sets the MONITOR Transmit Control bit MXC to 1. This enables the MX bit to go active (0), indicating the presence of valid MONITOR data (contents of MOX) in the corresponding frame.
As a result, the receiving device stores the MONITOR byte in its MONITOR Receive MOR register and generates a MDR interrupt status.

Alerted by the MDR interrupt, the microprocessor reads the MONITOR Receive (MOR) register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR control bit MRC to “1” to enable the receiver to store succeeding MONITOR channel bytes and acknowledge them according to the MONITOR channel protocol. In addition, it enables other MONITOR channel interrupts by setting MONITOR Interrupt Enable to “1”.

As a result, the first MONITOR byte is acknowledged by the receiving device setting the MR bit to “0”. This causes a MONITOR Data Acknowledge MDA interrupt status at the transmitter.

A new MONITOR data byte can now be written by the microprocessor in MOX. The MX bit is still in the active (0) state. The transmitter indicates a new byte in the MONITOR channel by returning the MX bit active after sending it once in the inactive state. As a result, the receiver stores the MONITOR byte in MOR and generates anew a MDR interrupt status. When the microprocessor has read the MOR register, the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate a MDA interrupt status.

This “MDA interrupt - write data - MDR interrupt - read data - MDA interrupt” handshake is repeated as long as the transmitter has data to send. Note that the MONITOR channel protocol imposes no maximum reaction times to the microprocessor.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microprocessor sets the MONITOR Transmit Control bit MXC to 0. This enforces an inactive (“1”) state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a MONITOR Channel End of Reception MER interrupt status is generated by the receiver when the MX is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to 0, which in turn enforces an inactive state in the MR bit. This marks the end of the transmission, making the MONITOR Channel Active MAC bit return to “0”.

During a transmission process, it is possible for the receiver to ask a transmission to be aborted by sending an inactive MR bit value in two consecutive frames. This is effected by the microprocessor writing the MR control bit MRC to 0. An aborted transmission is indicated by a MONITOR Channel Data Abort MAB interrupt status at the transmitter.
2.4.6 Terminal Specific Functions

In addition to the standard functions supporting the ISDN basic access, the ICC contains optional functions, useful in various terminal configurations.

The terminal specific function are enabled by setting bit TSF (STCR register) to “1”. This has two effects:

- The SIP/EAW line is defined as External Awake input (and not as SLD line);
- Second, the interrupts SAW and WOV (EXIR register) are enabled:
  - SAW (Subscriber Awake) generated by a falling edge on the EAW line
  - WOV (Watchdog Timer Overflow) generated by the watchdog timer. This occurs when the processor fails to write two consecutive bit patterns in ADF1:

<table>
<thead>
<tr>
<th>ADF1</th>
<th>WTC1</th>
<th>WTC2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0x0</td>
<td>0x0</td>
</tr>
</tbody>
</table>

Watchdog Timer Control 1,0.

The WTC1 and WTC2 bits have to be successively written in the following manner within 128 ms:

<table>
<thead>
<tr>
<th></th>
<th>WTC1</th>
<th>WTC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

As a result the watchdog timer is reset and restarted. Otherwise a WOV is generated.

Deactivating the terminal specific functions is only possible with a hardware reset.

Having enable the terminal specific functions via TSF = 1, the user can make the ICC generate a reset signal by programming the Reset Source Select RSS bit (CIX0 register), as follows:

0 —— A reset signal is generated as a result of
  - a falling edge on the EAW line (subscriber awake)
  - a C/I code change (exchange awake).

A falling edge on the EAW line also forces the IDP1 line of the IOM interface to zero.

**Note:** This should normally induce the attached layer-1 device to leave the power down state and supply clocking to ICC via DCL and FSC.

A corresponding interrupt status (CIC or SAW) is also generated.
1. A reset signal is generated as a result of the expiration of the watchdog timer (indicated by the WOV interrupt status).

   **Note:** That the watchdog timer is not running when the ICC is in the power-down state (IOM not clocked).

**Note:** Bit RSS has a significance only if terminal specific functions are activated (TSF = 1).

The RSS bit should be set to “1” by the user when the ICC is in power-up to prevent an edge on the EAW line or a change in the C/I code from generating a reset pulse.

Switching RSS from 0 to 1 or from 1 to 0 resets the watchdog timer.

The reset pulse generated by the ICC (output via RES pin) has a pulse width of 5 ms and is an active high signal.

### 2.4.7 Test Functions

The ICC provides the following test and diagnostic functions:

- digital loop via TLP (Test Loop, SPCR register) command bit: IDP1 is internally connected with IDP0, external input on IDP0 is ignored: this is used in system tests, to test layer-2 functionality independent of layer 1;

- special loops programmed via C2C1-0 and C1C1-0 bits (register SPCR, cf. 2.4.3).
2.4.8 Documentation of the Auto Mode

The Auto Mode of the ICC and ISAC-S is only applicable for the states 7 and 8 of the LAPD protocol. All other states (1 to 6) have to be performed in Non-Auto Mode (NAM). Therefore this documentation gives an overview of how the device reacts in the states 7 and 8, which reactions require software programming and which are done by the hardware itself, when interrupts and status register contents are set or change. The necessary software actions are also detailed in terms of command or mode register access.

The description is based on the SDL-Diagrams of the ETSI TS 46-20 dated 1989.

The diagrams are only annotated by documentary signs or texts (mostly register descriptions) and can therefore easily be interpreted by anyone familiar with the SDL description of LAPD. All deviations that occur are specially marked and the impossible actions, path etc. are crossed out.

To get acquainted with this documentation, first read through the legend-description and the additional general considerations, then start with the diagrams, referring to the legend and the register description in the Technical Manual if necessary.

We hope you will profit from this documentation and use our software-saving auto mode.

Legend of the Auto Mode Documentation

a. Symbols within a path

There are 3 symbols within a path

a.1 In the auto mode the device processes all subsequent state transitions branchings etc. up to the next symbol.

a.2 In the auto mode the device does not process the state transitions, branchings, etc. Within the path appropriate directions are given with which the software can accomplish the required action.

a.3 A path cannot be implemented and no software or hardware action can change this. These path are either optional or only applicable for window-size > 1.
b. Symbols at a path
   There is 1 symbol at a path

b.1 marks the beginning of a path, for which a.3 applies

c Symbols at an internal or external message box.
   There are 2 symbols at a message box.

c.1 This symbol means, that the action described in the box is not possible. Either the action specified is not done at all (box crossed out) or an additional action is taken (written into the box).
   Note: The impossibility to perform the optional T203 timer-procedure is not explicitly mentioned; the corresponding actions are only crossed out.

c.2 This symbol means, that within a software-path, by taking the prescribed register actions the contents of the box will be done automatically.

d. Text within boxes
   Text within boxes can be grouped in one of two classes.

d.1 The text denotes an interrupt which is always associated with the event (but can also be associated with other events). (See ISTA and EXIR register description in the Technical Manual for an interrupt description)

d.2 The text describes a register access

   either a register read access to discriminate this state from others or to reach a branching condition.

   or a register write access to give a command.

   The text is placed in the box that describes the functions for which the register access is needed.
e. Text at the side of boxes

e.1  
Box  
Text  

The text describes an interrupt associated with the contents of the box. The interrupt is always associated with the box contents, if the interrupt name is not followed by a “/”, it is associated only under appropriate conditions if a “/” is behind it.

e.1  
Box  
Text  

The text describes a possible or mandatory change of a bit in a status-register associated with the contents of the box.

(The attached texts can also be placed on the left side.)

f. Text above and below boxes

f.1  
Text  
box  

Text describes a mandatory action to performed on the contents of the box.

f.2  
Box  
Text  

Text describes a mandatory action to be taken as a result of the contents of the box. Action here means register access.

g. Shaded boxes

Box  

The box describes an impossible state or action for the device.
Additional General Considerations when Using the Auto Mode

a) Switching from Auto Mode to Non-Auto Mode.

As mentioned in the introduction the Auto Mode is only applicable in the states 7 and 8 of the LAPD. Therefore whenever these states have to be left (which is indicated by a “Mode:NAM” text) there are several actions to be taken that could not all be detailed in the SDL-diagrams:

a.1) write Non Auto Mode and TMD = 0 into the mode register.

a.2) write the timer register with an arbitrary value to stop it. The timer T200 as specified in the LAPD-Protocol is implemented in the hardware only in the states 7 and 8; in all other states this or any other timer-procedure has to be done by the software with the possible use of the timer in external timer mode.

a.3) read the WFA bit of the STAR2 register and store it in a software variable. The information in this bit may be necessary for later decisions. When switching from Auto Mode to Non-Auto Mode XPR interrupts may be lost.

a.4) In the Non-Auto Mode the software has to decode I, U and S-frames because I and S frames are only handled autonomously in the Auto Mode.

a.5) The RSC and PCE interrupts, the contents of the STAR2 register and the RRNR bit in the STAR register are only meaningful within the Auto Mode.

a.6) leave some time before RHR or XRES is written to reset the counters, as a currently sent frame may not be finished yet.

b) What has to be written to the XFIFO?

In the legend description when the software has to write contents of a frame to the XFIFO only “XFIFO” is shown in the corresponding box. We shall given here a general rule of what has to be written to the XFIFO:

a) For sending an I frame with CMDR:XIF, only the information field content, i.e. no SAPI, TEI, control field should be written to the XFIFO.

b) For sending an U frame or any other frame with CMDR:XTF, the SAPI, TEI and the control field has to be written to the XFIFO.

c) The interrupts XPR and XMR.

The occurrence of an XPR interrupt in Auto Mode after an XIF command indicates that the I frame sent was acknowledged and the next I frame can be sent, if STAR2:TREC indicates state 7 and STAR:RRNR indicates Peer Rec not busy. If Peer Rec is busy after an XPR, the software should wait for the next RSC interrupt before sending the next I-frame. If the XPR happens to be in the Timer Recovery state, the software has to poll the STAR2 register until the state Multiple Frame Established is reached or a TIN interrupt is issued which requires Auto Mode to be left (One of these two conditions will occur before the time T200xN200). In Non-Auto Mode or after an XTF command the XPR just indicates, that the frame was sent successfully.
The occurrence of an XMR interrupt in Auto Mode after an XIF command indicates that the I frame sent was either rejected by the Peer Entity or that a collision occurred on the S interface. In both cases the I frame has to be retransmitted (after an eventual waiting for the RSC interrupt if the Peer Rec was busy; after an XMR the device will always be in the state 7). In Non-Auto Mode or after an XTF command the XMR indicates that a collision occurred on the S interface and the frame has to be retransmitted.

d) The resetting of the RC variable:

The RC variable is reset in the ICC and ISAC-S when leaving the state Timer Recovery. The SLD diagrams indicate a reset in the state Multiple Frame Established when T200 expires. There is no difference to the outside world between these implementations however our implementation is clearer.

e) The timer T203 procedure:

We do not fully support the optional timer T203 procedure, but we can still find out whether or not S frames are sent on the link in the Auto Mode. By polling the STAR2:SDET bit and (re)starting a software timer whenever a one is read we can build a quasi T203 procedure which handles approximately the same task. When T203 expires one is supposed to go into the Timer Recovery State with RC = 0. This is possible for the ICC and ISAC-S by just writing the STI bit in the CMDR register (Auto Mode and Internal Timer Mode assumed).

f) The congestion procedure as defined in the 1 TR 6 of the “Deutsche Bundespost”.

In the 1 TR 6a variable N2x4 is defined for the maximum number of Peer Busy requests. The 1 TR is in this respect not compatible with the Q921 of CCITT or the ETSI 46–20 but it is, nevertheless, sensible to avoid getting into a hangup situation. With the ICC and ISAC-S this procedure can be implemented:

After receiving an RSC interrupt with RRNR set one starts a software – timer. The timer is reset and stopped if one either receives another RSC interrupt with a reset RRNR, if one receives a TIN interrupt or if other conditions occur that result in a reestablishment of the link. The timer expires after N2x4xT200 and in this case the 1 TR 6 recommends a reestablishment of the link.

g) Dealing with error conditions: The SLD diagrams do not give a very detailed description of how to deal with errors. Therefore we prepared a special Application Note:

“How to deal with an error condition of the LAPD-Protocol with your ICC or ISAC-S”
Note: The regeneration of this signal does not affect the sequence integrity of the I queue.

Figure 24a
Figure 24b
Note: These signals are generated outside of this SDL representation, and may be generated by the connection management entity.

Figure 24d
Functional Description

Figure 24f

Semiconductor Group 74
Figure 24h

Figure 24i

Note 1: Processing of acknowledge pending is described figure 24i.

Note 2: This SDL representation does not include the optional procedure in Appendix I.
Figure 24j
Semiconductor Group

Functional Description

Figure 25a
Figure 25b
Figure 25c
Note: These signals are generated outside of this SDL representation, and may be generated by the connection management entity.
Figure 25e
Figure 25g

Note 1: Processing of acknowledge pending is described on figure 25i.
Note 2: This SDL representation does not include the optional procedure in Appendix I.
Note 1: The relevant states are as follows
4 TEI-assigned
5 Awaiting-establishement
6 Awaiting-release
7 Multiple-frame-established
8 Timer-recovery

Note 2: The data link layer returns to the state it was in prior to the events shown.

ITD02384
Note 1: The relevant states are as follows
7 Multiple-frame-established
8 Timer-recovery
Figure 26c
Note: The generation of the correct number of signals in order to cause the required retransmission of I frames does not alter their sequence integrity.
3 Operational Description

3.1 Microprocessor Interface Operation

The ICC microcontroller interface can be selected to be either of the

(1) – Motorola type with control signals CS, R/W, DS

(2) – Siemens/Intel non-multiplexed bus type with control signals CS, WR, DS

(3) – or of the Siemens/Intel multiplexed address/data bus type with control signals CS, WR, RD, ALE

The selection is performed via pin ALE as follows:

ALE tied to VDD \( \rightarrow \) (1)
ALE tied to VSS \( \rightarrow \) (2)
Edge on ALE \( \rightarrow \) (3).

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects interface type (3). A return to one of the other interface types is possible only if a hardware reset is issued.

3.2 Reset

After a hardware reset (pin RES), the ICC is in an idle state, and its registers are loaded with specified values. A subset of ICC registers with defined reset values is listed in table 9.

During the reset pulse pins SDAX/SDS1 and SCA/FSD/SDS2 are “low”, all other pins are in high impedance state.

1) Note: These μp-interface-modes only make sense for a 28 pin package, as the address pins are needed. The multifunctional pins SDAR and SIP are automatically interpreted as A2 and A5 resp. and should therefore not be used for SSI or SLD interface or terminal specific functions.
### Table 9
State of ICC Registers after Hardware Reset

<table>
<thead>
<tr>
<th>Register</th>
<th>Value after Reset (hex)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISTA</td>
<td>00</td>
<td>no interrupts</td>
</tr>
<tr>
<td>MASK</td>
<td>00</td>
<td>all interrupts enabled</td>
</tr>
<tr>
<td>EXIR</td>
<td>00</td>
<td>no interrupts</td>
</tr>
</tbody>
</table>
| STAR     | 48 (4A)                 | - XFIFO is ready to be written to  
- RFIFO is ready to receive at least 16 octets of a new message |
| CMDR     | 00                      | no command |
| MODE     | 00                      | - auto mode  
- 1-octet address field  
- external timer mode  
- receiver inactive  
- IOM-1 interface, MONITOR channel used for TIC bus access only |
| RBCL     | 00                      | - no frame bytes received |
| RBCH     | XXX000002               | - no frame bytes received |
| SPCR     | 00                      | - IDP1 pin = “High”  
- SIP pin “High impedance”  
- Timing mode 0  
- IOM interface test loop deactivated  
- SLD B channel loop selected  
- SDAX/SDS1, SCA/FSD/SDS2 pins = “Low” |
| CIRR/CIR0| 7C                      | - another device occupies the D and C/I channels  
- received C/I code = “1111”  
- no C/I code change |
| CIXR/CIX0| BF                      | - TIC bus is not requested for transmitting a C/I code  
- transmitted C/I code = “1111”  
- T, E = logical “1” |
| STCR     | 00                      | - terminal specific functions disabled  
- TIC bus address = “0000”  
- no synchronous transfer |
| ADF1     | 00                      | - inter-frame time fill = continuous “1” |
| ADF2     | 00                      | - IOM-1 interface mode selected  
- SDS1/2 low |
3.3 Initialization

During initialization a subset of registers have to be programmed to set the configuration parameters according to the application and desired features. They are listed in Table 10.

In Table 10 the ISDN applications are denoted using the following abbreviations:

- **TE** Terminal Equipment TE1, TA
e.g. ISDN feature telephone
  ISDN voice/data workstation
  Terminal Adaptor for non-ISDN terminals (TE2)
- **LT** Line Termination
- **NT** Intelligent Network Termination

### Table 10
Configuration Parameters for Initialization

<table>
<thead>
<tr>
<th>Register</th>
<th>Bit</th>
<th>Effect</th>
<th>Application</th>
<th>Restricted to</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADF 2</td>
<td>IMS</td>
<td>Program IOM-1 or IOM-2 interface mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>D2C2-0</td>
<td>Polarity of SDS2/1 (and/or selection of HDLC channel)</td>
<td></td>
<td>IOM-2</td>
</tr>
<tr>
<td></td>
<td>D1C2-0</td>
<td>IOM output driver tri-state/open drain</td>
<td></td>
<td>IOM-2</td>
</tr>
<tr>
<td></td>
<td>ODS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPCR (note)</td>
<td>SPU</td>
<td>Pull IDP1 low (to request clocking from layer-1 device).</td>
<td>TE</td>
<td>IOM</td>
</tr>
<tr>
<td></td>
<td>SAC</td>
<td>SLD port inactive/active</td>
<td></td>
<td>IOM-1</td>
</tr>
</tbody>
</table>
|          | SPM | 0 Timing mode 0  
1 Timing mode 1 | TE/NT  
LT only | IOM-1 |
|          | TLP | 0 Terminal timing mode  
1 Non-terminal timing mode | TE  
LT | IOM-2 |
|          | C2C1-0 | Serial port B-test loop | | |
|          | C1C1-0 | B-channel switching  
or B/IC channel connect | | IOM-1 |
|          | | | | IOM-2 |
Configuration Parameters for Initialization (cont’d)

<table>
<thead>
<tr>
<th>Register</th>
<th>Bit</th>
<th>Effect</th>
<th>Application</th>
<th>Restricted to</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODE</td>
<td>DIM2-0</td>
<td>IOM interface configuration for D + C/I channel arbitration Stop/Go bit monitoring for HDLC transmission yes/no HDLC interface characteristics</td>
<td>Serial HDLC communication</td>
<td>IOM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADF1</td>
<td>IDC</td>
<td>IOM Data Port IDP1,0 direction control</td>
<td></td>
<td>IOM-2</td>
</tr>
<tr>
<td></td>
<td>CSEL2-0</td>
<td>IOM channel select (Time slot)</td>
<td>non-TE</td>
<td>IOM-2</td>
</tr>
<tr>
<td>CIXR/CIX0</td>
<td>RSS</td>
<td>Hardware reset generated by either subscriber/exchange awake or watchdog timer</td>
<td>TE specific functions (TSF = 1)</td>
<td>IOM</td>
</tr>
<tr>
<td>STCR</td>
<td>TSF</td>
<td>Terminal specific function enable/SLD interface enable</td>
<td></td>
<td>IOM</td>
</tr>
<tr>
<td></td>
<td>TBA2-0</td>
<td>TIC bus address</td>
<td></td>
<td>IOM</td>
</tr>
<tr>
<td>MODE</td>
<td>MDS2-0</td>
<td>HDLC message transfer mode 2 octet/(1 octet) address</td>
<td></td>
<td>Auto mode only</td>
</tr>
<tr>
<td></td>
<td>TMD</td>
<td>Timer mode external/internal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIMR</td>
<td>CNT</td>
<td>N1 and T1 in internal timer mode (TMD = 1) T2 in external timer mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VALUE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XAD1</td>
<td></td>
<td>SAPI, TEI</td>
<td></td>
<td>Auto mode only</td>
</tr>
<tr>
<td>XAD2</td>
<td></td>
<td>Transmit frame address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SAPI1/2</td>
<td></td>
<td>Receive SAPI, TEI address values for internal address recognition</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEI1/2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** After a hardware reset the pins SDAX/SDS1 and SCA/FSD/SDS2 are both “low” and have the functions of SDS1 and SDS2 in terminal timing mode (since SPM = 0), respectively, until the SPCR is written to for the first time. From that moment on, the function taken on by these pins depends on the state of IOM Mode Select bit IMS (ADF2 register).
3.4 IOM® Interface Connections

IOM®-1

In IOM-1 interface mode

– pin IDP0 carries B channel, MONITOR, D and C/I data from layer 1 to layer 2
– pin IDP1 carries B channel, MONITOR, D and C/I data from layer 2 to layer 1.

IDP1 is an open drain output. The B channels can be set inactive (FFH) by setting the B channel connect bits C1C1-0 and C2C1-0 in SPCR register to 0 (SLD loop), which is the state after a hardware reset.

The MONITOR channel is inactive (FFH) if:

– no MONITOR channel transfer is programmed
– and the TIC bus (i.e. the fourth octet of IOM frame: D and C/I channels) is not accessed.

IOM®-2

Because of the enhanced communication capabilities offered by the IOM-2, e.g. for the control of peripheral devices via the MONITOR channel, the direction of IDP0 and IDP1 is programmable.

The type of the IOM output is selectable via bit ODS (ADF2) register. Thus, the driver is of the open drain type if ODS = 0, and of the push-pull type when ODS = 1.

Non-Terminal Mode (SPM = 1)

Outside the programmed 4-byte subscriber channel (bits CSEL2-0, ADF1 register), both IDP1 and IDP0 are inactive.

Inside the programmed 4-byte subscriber channel:

– IDP1 carries the 2B+D channels as output toward the subscriber and the MONITOR and C/I channel as output to the layer 1
– IDP1 is inactive during B1 and B2
– IDP0 carries the 2B + D channels coming from the subscriber line, and the MONITOR and C/I channels from layer 1.

If IDC (IOM Direction Control, ADF1 register) is set to “1”, IDP0 sends the MONITOR, D and C/I channels normally carried by IDP1, i.e. normally destined to the subscriber. This feature can be used for test purposes, e.g. to send the D channel towards the system instead of the subscriber. See figure 27.
Operational Description

Figure 27
IOM® Data Ports 0, 1 in Non-Terminal Mode (SPM = 1)

Terminal Mode (SPM = 0)

In this case the IOM has the 12-byte frame structure consisting of channels 0, 1, and 2 (see figure 11):

- IDP0 carries the 2B + D channels from the subscriber line, and the MONITOR 0 and C/I 0 channels coming from layer 1;
- IDP1 carries the MONITOR 0 and C/I 0 channels to the layer 1.

Channel 1 of the IOM interface is used for internal communication in terminal applications. Two cases have to be distinguished, according to whether the ICC is operated as a master device (communication with slave devices via MONITOR 1 and C/I 1), or as a slave device (communication with one master via MONITOR 1 and C/I 1).
Figure 28a
IOM® Data Ports 0, 1 in Terminal Mode (SPM = 0)
Figure 28b
IOM® Data Ports 0, 1 in Terminal Mode (SPM = 0)
If IDC is set to “0” (Master Mode):
- IDP0 carries the MONITOR 1 and C/I 1 channels as output to peripheral (voice/data) devices;
- IPD0 carries the IC channels as output to other devices, if programmed (CxC1-0 = 01 in register SPCR).

If IDC is set to “1” (Slave mode):
- IDP1 carries the MONITOR 1 and C/I 1 channels as output to a master device;
- IPD0 carries the IC channels as output to other devices, if programmed (CxC1-0 = 01 in register SPCR).

If required (cf. DIM2-0, MODE register), bit 5 of the last byte in channel 2 on IDP0 is used to indicate the D-channel state (Stop/Go bit) on and bits 2 to 5 of the last byte are used for TIC bus access arbitration.

**Figure 28** shows the connections in a multifunctional terminal with the ICC as a master (**figure 28a**) or a slave device (**figure 28b**).
3.5 Processing

3.5.1 Interrupt Structure
Since the ICC provides only one interrupt request output (INT), the cause of an interrupt is determined by the microprocessor by reading the Interrupt Status Register ISTA. In this register, seven interrupt sources can be directly read. The LSB of ISTA points to eight non-critical interrupt sources which are indicated in the Extended Interrupt Register EXIR (Figure 29).

![Figure 29: ICC Interrupt Structure](image)

A read of the ISTA register clears all bits except EXI and CIC. CIC is cleared by reading CIRR/CIR0. A read of EXIR clears the EXI bit in ISTA as well as the EXIR register.

When all bits in ISTA are cleared, the interrupt line (INT) is deactivated.

Each interrupt source in ISTA register can be selectively masked by setting to “1” the corresponding bit in MASK. Masked interrupt status bits are not indicated when ISTA is read. Instead, they remain internally stored and pending, until the mask bit is reset to zero. Reading the ISTA while a mask bit is active has no effect on the pending interrupt.

In the event of an extended interrupt EXIR, EXI is set even when the corresponding mask bit in MASK is active, but no interrupt (INT) is generated. In the event of a C/I channel interrupt CIC is set, even when the corresponding mask bit in MASK is active, but no interrupt (INT) is generated.

Except for CIC and MOS all interrupt sources are directly determined by a read of ISTA and (possibly) EXIR.
Figure 30 shows the CIC and MOS interrupt logic.

CIC Interrupt Logic

A CIC interrupt may originate

- from a change in received C/I channel (0) code (CIC0)
- or (in the case of IOM-2 terminal mode only)
- from a change in received C/I channel 1 code (CIC 1).

The two corresponding status bits CIC0 and CIC1 are read in CIR0 register. CIC1 can be individually disabled by clearing the enable bit CI1E (ADF1 register). In this case the occurrence of a code change in CIR1 will not be displayed by CIC1 until the corresponding enable bit has been set to one.

Bits CIC0 and CIC1 are cleared by a read of CIR0.

An interrupt status is indicated every time a valid new code is loaded in CIR0 or CIR1. But in the case of a code change, the new code is not loaded until the previous contents have been read. When this is done and a second code change has already occurred, a new interrupt is immediately generated and the new code replaces the previous one in the register. The code registers are buffered with a FIFO size of two. Thus, if several consecutive codes are detected, only the first and the last code is obtained at the first and second register read, respectively.
Figure 30
(a) CIC Interrupt Structure
(b) MOS Interrupt Structure (IOM®-2 Mode)
MOS Interrupt Logic

The MOS interrupt logic shown in figure 30 is valid only in the case of IOM-2 interface mode. Further, only one MONITOR channel is handled in the case of IOM-2 non-terminal timing modes. In this case, MOR1 and MOX1 are unused.

The MONITOR Data Receive interrupt status MDR has two enable bits, MONITOR Receive interrupt Enable (MRE) and MR bit Control (MRC). The MONITOR channel End of Reception MER, MONITOR channel Data Acknowledged MDA and MONITOR channel Data Abort MAB interrupt status bits have a common enable bit MONITOR Interrupt Enable MIE.

MRE prevents the occurrence of MDR status, including when the first byte of a packet is received. When MRE is active (1) but MRC is inactive, the MDR interrupt status is generated only for the first byte of a receive packet. When both MRE and MRC are active, MDR is always generated and all received MONITOR bytes - marked by a 1-to-0 transition in MX bit - are stored. (Additionally, an active MRC enables the control of the MR handshake bit according to the MONITOR channel protocol.)

In IOM-1 mode the reception of a MONITOR byte is directly indicated by MOS interrupt status, and registers MOCR and MOSR are not used.

3.5.2 Data Transfer

The control of the data transfer phase is mainly done by commands from the µP to ICC via the Command Register (CMDR).

Table 11 gives a summary of possible interrupts from the HDLC controller and the appropriate reaction to these interrupts.

Table 12 lists the most important commands which are issued by a microprocessor by setting one or more bits in CMDR.

The powerful FIFO logic, which consists of a 2 x 32 byte receive and a 2 x 32 byte transmit FIFO, as well as an intelligent FIFO controller, builds a flexible interface to the upper protocol layers implemented in the microcontroller.

The extent of LAPD protocol support is dependent on the selected message transfer mode, see section 2.4.1.
## Table 11
Interrupts from ICC HDLC Controller

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Register</th>
<th>Meaning</th>
<th>Reaction</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Layer-2 Receive</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RPF</td>
<td>ISTA</td>
<td>Receive Pool Full. Request to read received octets of an uncompleted HDLC frame from RFIFO.</td>
<td>Read 32 octets from RFIFO and acknowledge with RMC.</td>
</tr>
<tr>
<td>RME</td>
<td>ISTA</td>
<td>Receive Message End. Request to read received octets of a complete HDLC frame (or the last part of a frame) from RFIFO.</td>
<td>Read RFIFO (number of octets given by RBCL4-0) and status information and acknowledge with RMC.</td>
</tr>
<tr>
<td>RFO</td>
<td>EXIR</td>
<td>Receive Frame Overflow. A complete frame has been lost because storage space in RFIFO was not available.</td>
<td>Error report for statistical purposes. Possible cause: deficiency in software.</td>
</tr>
<tr>
<td>PCE</td>
<td>EXIR</td>
<td>Protocol Error. S or I frame with incorrect N(R) or S frame with I field received (in auto mode only).</td>
<td>Link re-establishment. Indication to layer 3.</td>
</tr>
<tr>
<td><strong>Layer-2 Transmit</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XPR</td>
<td>ISTA</td>
<td>Transmit Pool Ready. Further octets of an HDLC frame can be written to XFIFO. If XIFC was issued (auto mode), indicates that the message was successfully acknowledged with S frame.</td>
<td>Write data bytes in the XFIFO if the frame currently being transmitted is not finished or a new frame is to be transmitted, and issue an XIF, XIFC, XTF or XTFC command.</td>
</tr>
<tr>
<td>XMR</td>
<td>EXIR</td>
<td>Transmit Message Repeat. Frame must be repeated because of a transmission error (all HDLC message transfer modes) or a received negative acknowledgement (auto mode only) from peer station.</td>
<td>Transmission of the frame must be repeated. No indication to layer 3.</td>
</tr>
<tr>
<td>XDU</td>
<td>EXIR</td>
<td>Transmit Data Underrun. Frame has been aborted because the XFIFO holds no further data and XME (XIFC or XTFC) was not issued.</td>
<td>Transmission of the frame must be repeated. Possible cause: excessively long software reaction times.</td>
</tr>
</tbody>
</table>
## Operational Description

**Layer-2 Transmit (cont’d)**

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Register</th>
<th>Meaning</th>
<th>Reaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSC</td>
<td>ISTA</td>
<td>Receive Status Change. A status change from peer station has been received (RR or RNR frame), auto mode only.</td>
<td>Stop sending new I frames.</td>
</tr>
<tr>
<td>TIN</td>
<td>ISTA</td>
<td>Timer Interrupt. External timer expired or, in auto mode, internal timer (T200) and repeat counter (N200) both expired.</td>
<td>Link re-established. Indication to layer 3. (Auto mode)</td>
</tr>
</tbody>
</table>
Table 12  
List of Commands

<table>
<thead>
<tr>
<th>Command Mnemonic</th>
<th>HEX</th>
<th>Bit 7 ... 0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMC</td>
<td>80</td>
<td>1000 0000</td>
<td><strong>Receive Message Complete.</strong> Acknowledges a block (RPF) or a frame (RME) stored in the RFIFO.</td>
</tr>
<tr>
<td>RRES</td>
<td>40</td>
<td>0100 0000</td>
<td><strong>Reset HDLC Receiver.</strong> The RFIFO is cleared. the transmit and receive counters (V(S), V(R)) are reset (auto mode).</td>
</tr>
<tr>
<td>RNR</td>
<td>20</td>
<td>0010 0000</td>
<td><strong>Receiver Not Ready (auto mode).</strong> An I or S frame will be acknowledged with RNR frame.</td>
</tr>
<tr>
<td>STI</td>
<td>10</td>
<td>0001 0000</td>
<td><strong>Start Timer.</strong></td>
</tr>
<tr>
<td>XTFC</td>
<td>0A</td>
<td>0000 1010</td>
<td><strong>Transmit Transparent Frame and Close.</strong> Enables the “transparent” transmission of the block entered last in the XFIFO. The frame is closed with a CRC and a flag.</td>
</tr>
<tr>
<td>XIFC</td>
<td>06</td>
<td>0000 0110</td>
<td><strong>Transmit I Frame and Close.</strong> Enables the “auto mode” transmission of the block entered last in the XFIFO. The frame is closed with a CRC and a flag.</td>
</tr>
<tr>
<td>XTF</td>
<td>08</td>
<td>0000 1000</td>
<td><strong>Transmit Transparent Frame.</strong> Enables the “transparent” transmission of the block entered last in the XFIFO without closing the frame.</td>
</tr>
<tr>
<td>XIF</td>
<td>04</td>
<td>0000 0100</td>
<td><strong>Transmit I Frame.</strong> Enables the “auto mode” transmission of the block entered last in the XFIFO without closing the frame.</td>
</tr>
<tr>
<td>XRES</td>
<td>01</td>
<td>0000 0001</td>
<td><strong>Reset HDLC Transmitter.</strong> The XFIFO is cleared.</td>
</tr>
</tbody>
</table>


3.5.2.1 HDLC Frame Reception

Assuming a normally running communication link (layer 1 activated, layer 2 link established), figure 31 illustrates the transfer of an I frame. The transmitter is shown on the left and the receiver on the right, with the interaction between the microcontroller system and the ICC in terms of interrupt and command stimuli.

When the frame (excluding the CRC field) is not longer than 32 bytes, the whole frame is transferred in one block. The reception of the frame is reported via the Receive Message End (RME) interrupt. The number of bytes stored in RFIFO can be read out from RBCL. The Receive Status Register (RSTA) includes information about the frame, such as frame aborted yes/no or CRC valid yes/no and, if complete or partial address recognition is selected, the identification of the frame address.

Depending on the HDLC message transfer mode, the address and control field of the frame can be read from auxiliary registers (SAPR and RHCR), as shown in figure 32.

---

**Figure 31**

Transmission of an I Frame in the D Channel (Subscriber to Exchange)

**Note 1** Only if a 2-byte address field is defined (MDS0 = 1 in MODE register).
### Note 2
Comparison with group TEI (FFH) is only made if a 2-byte address field is defined (MDS0 = 1 in MODE register).

### Note 3
In the case of an extended, modulo 128 control field format (MCS = 1 in SAP2 register) the control field is stored in RHCR in compressed form (I frames).

### Note 4
In the case of extended control field, only the first byte is stored in RHCR, the second in RFIFO.

---

**Figure 32**
**Receive Data Flow**

<table>
<thead>
<tr>
<th>Flag</th>
<th>Address High</th>
<th>Address Low</th>
<th>Control</th>
<th>Information</th>
<th>CRC</th>
<th>Flag</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Auto-Mode (U and I frames)</strong></td>
<td><strong>SAP1,SAP2, FE,FC</strong></td>
<td>TEI1,TEI2 FF</td>
<td>RCR</td>
<td>RFIFO</td>
<td>RSTA</td>
<td></td>
</tr>
<tr>
<td><strong>Non-Auto Mode</strong></td>
<td><strong>SAP1,SAP2, FE,FC</strong></td>
<td>TEI1,TEI2 FF</td>
<td>RCR</td>
<td>RFIFO</td>
<td>RSTA</td>
<td></td>
</tr>
<tr>
<td><strong>Transparent Mode 1</strong></td>
<td><strong>SAPR</strong></td>
<td>TEI1,TEI2 FF</td>
<td>SAPR</td>
<td>RFIFO</td>
<td>RSTA</td>
<td></td>
</tr>
<tr>
<td><strong>Transparent Mode 2</strong></td>
<td></td>
<td></td>
<td>RFIFO</td>
<td></td>
<td>RSTA</td>
<td></td>
</tr>
<tr>
<td><strong>Transparent Mode 3</strong></td>
<td><strong>SAP1,SAP2, FE,FC</strong></td>
<td></td>
<td>RFIFO</td>
<td></td>
<td>RSTA</td>
<td></td>
</tr>
</tbody>
</table>

**Description of Symbols:**
- Checked automatically by ICC
- Compared with register or fixed value
- Stored into register or RFIFO

[ITD02872]
A frame longer than 32 bytes is transferred to the microcontroller in blocks of 32 bytes plus one remainder of length 1 to 32 bytes. The reception of a 32-byte block is reported by a Receive Pool Full (RPF) interrupt and the data in RFIFO remains valid until this interrupt is acknowledged (RMC). This process is repeated until the reception of the remainder block is completed, as reported by RME (figure 31). If the second RFIFO pool has been filled or an end-of-frame is received while a previous RPF or RME interrupt is not yet acknowledged by RMC, the corresponding interrupt will be generated only when RMC has been issued. When RME has been indicated, bits 0-4 of the RBCL register represent the number of bytes stored in the RFIFO. Bits 7 to 5 of RBCL and bits 0 to 3 of RBCH indicate the total number of 32-byte blocks which were stored until the reception of the remainder block. When the total frame length exceeds 4095 bytes, bit OV (RBCH) is set but the counter is not blocked.

The contents of RBCL, RBCH and RSTA registers are valid only after the occurrence of the RME interrupt, and remain valid until the microprocessor issues an acknowledgment (RMC). The contents of RHCR and/or SAPR, also remain valid until acknowledgment.

If a frame could not be stored due to a full RFIFO, the microcontroller is informed of this via the Receive Frame Overflow interrupt (RFO).

### 3.5.2.2 HDLC Frame Transmission

After the XFIFO status has been checked by polling the Transmit FIFO Write Enable (XFW) bit or after a Transmit Pool Ready (XPR) interrupt, up to 32 bytes may be entered in XFIFO. Transmission of an HDLC frame is started when a transmit command (see table 12) is issued. The opening flag is generated automatically. In the case of an auto mode transmission (XIF or XIFC), the control field is also generated by the ICC, and the contents of register XAD1 (and, for LAPD, XAD2) are transmitted as the address, as shown in figure 33.
Figure 33
Transmit Data Flow

Description of Symbols:

- Generated automatically by ICC
- Written initially by CPU (into register)
- Loaded (repeatedly) by CPU upon ICC request (XPR interrupt)
The HDLC controller will request another data block by an XPR interrupt if there are no more than 32 bytes in XFIFO and the frame close command bit (Transmit Message End XME) has not been set. To this the microcontroller responds by writing another pool of data and re-issuing a transmit command for that pool. When XME is set, all remaining bytes in XFIFO are transmitted, the CRC field and the closing flag of the HDLC frame are appended and the controller generates a new XPR interrupt.

The microcontroller does not necessarily have to transfer a frame in blocks of 32 bytes. As a matter of fact, the sub-blocks issued by the microcontroller and separated by a transmit command, can be between 0 and 32 bytes long.

If the XFIFO runs out of data and the XME command bit has not been set, the frame will be terminated with an abort sequence (seven 1’s) followed by inter-frame time fill, and the microcontroller will be advised by a Transmit Data Underrun (XDU) interrupt. An HDLC frame may also be aborted by setting the Transmitter Reset (XRES) command bit.
4 Detailed Register Description

The parameterization of the ICC and the transfer of data and control information between the μP and ICC is performed through two register sets.

The register set in the address range 00-2 Bₜ pertains to the HDLC transceiver and LAPD controller. It includes the two FIFOs having an identical address range from 00-1 Fₜ.

The register set ranging from 30-3 Aₜ pertains to the control of layer-1 functions and of the IOM interface. Since the meaning of most register bits depends on the select IOM mode (IOM-1 or IOM-2), the description of this register set is divided into two sections:

- Special Purpose Registers: IOM-1 mode
- Special Purpose Registers: IOM-2 mode

The address map and a register summary are shown in the following tables:

Table 13
ICC Address Map 00-2BH

<table>
<thead>
<tr>
<th>Address (hex)</th>
<th>Read</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>00-1F</td>
<td>RFIFO</td>
<td>Receive FIFO</td>
</tr>
<tr>
<td>20</td>
<td>ISTA</td>
<td>Interrupt Status Register</td>
</tr>
<tr>
<td>21</td>
<td>STAR</td>
<td>Status Register</td>
</tr>
<tr>
<td>22</td>
<td>MODE</td>
<td>Mode Register</td>
</tr>
<tr>
<td>23</td>
<td>TIMR</td>
<td>Timer Register</td>
</tr>
<tr>
<td>24</td>
<td>EXIR</td>
<td>Extended Interrupt Register</td>
</tr>
<tr>
<td>25</td>
<td>RBCL</td>
<td>Receive Frame Byte Count Low</td>
</tr>
<tr>
<td>26</td>
<td>SAPR</td>
<td>Receive SAPI</td>
</tr>
<tr>
<td>27</td>
<td>RSTA</td>
<td>Receive Status Register</td>
</tr>
<tr>
<td>28</td>
<td>STAR2</td>
<td>Status Register 2</td>
</tr>
<tr>
<td>29</td>
<td>RHCR</td>
<td>Receive HDLC Control</td>
</tr>
<tr>
<td>2A</td>
<td>RBCH</td>
<td>Receive Frame Byte Count High</td>
</tr>
<tr>
<td>2B</td>
<td>STAR2</td>
<td>Status Register 2</td>
</tr>
</tbody>
</table>
### Table 14
**ICC Address Map 30-3A\(^H\)**

<table>
<thead>
<tr>
<th>Address (hex)</th>
<th>Read</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>Address</td>
<td>(hex)</td>
</tr>
<tr>
<td></td>
<td>Address</td>
<td>(hex)</td>
</tr>
<tr>
<td>30</td>
<td>SPCR</td>
<td>Serial Port Control Register</td>
</tr>
<tr>
<td>31</td>
<td>CIRR/</td>
<td>Command /Indication Receive</td>
</tr>
<tr>
<td></td>
<td>CIR0</td>
<td>(0)</td>
</tr>
<tr>
<td>32</td>
<td>MOR/</td>
<td>MONITOR Receive (0)</td>
</tr>
<tr>
<td></td>
<td>MOR0</td>
<td>MOX/</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MONITOR Transmit (0)</td>
</tr>
<tr>
<td>33</td>
<td>SSCR/</td>
<td>SIP Signaling Code Receive</td>
</tr>
<tr>
<td></td>
<td>CIR1</td>
<td>Command/Indication Receive 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CIX1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SIP Signaling Code Transmit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Command/Indication Transmit 1</td>
</tr>
<tr>
<td>34</td>
<td>SFCR/</td>
<td>SIP Feature Control Read/</td>
</tr>
<tr>
<td></td>
<td>MOR1</td>
<td>MONITOR Receive 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SFCW/</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MOX1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SIP Feature Control Write/</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MONITOR Transmit 1</td>
</tr>
<tr>
<td>35</td>
<td>C1R</td>
<td>Channel Register 1</td>
</tr>
<tr>
<td>36</td>
<td>C2R</td>
<td>Channel Register 2</td>
</tr>
<tr>
<td>37</td>
<td>B1CR</td>
<td>B1 Channel Register</td>
</tr>
<tr>
<td>38</td>
<td>B2CR</td>
<td>STCR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sync Transfer Control Register</td>
</tr>
<tr>
<td>39</td>
<td>ADF2</td>
<td>Additional Feature Register 2</td>
</tr>
<tr>
<td>3A</td>
<td>MOSR</td>
<td>MONITOR Status Register</td>
</tr>
<tr>
<td></td>
<td>MOCR</td>
<td>MONITOR Control Register</td>
</tr>
</tbody>
</table>
### Table 15
Register Summary: HDLC Operation and Status Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>20H</td>
<td>RME RPF RSC XPR TIN CIC SIN EXI ISTA R</td>
</tr>
<tr>
<td>20H</td>
<td>Mask W</td>
</tr>
<tr>
<td>21H</td>
<td>XFW XRN XRN MBR MAC1 BVS MAC0 STAR R</td>
</tr>
<tr>
<td>21H</td>
<td>CMD W</td>
</tr>
<tr>
<td>22H</td>
<td>MDS1 MDS0 TMD RAC DIM2 DIM1 DIM0 MOD R/W</td>
</tr>
<tr>
<td>23H</td>
<td>CONT VAL- TIMR R/W</td>
</tr>
<tr>
<td>24H</td>
<td>XMR XDU PCE RFO SOV MOS SAW WOV EXIR R</td>
</tr>
<tr>
<td>24H</td>
<td>XAD1 R</td>
</tr>
<tr>
<td>25H</td>
<td>RBC7 RBC6 RBC5 RBC4 RBC3 RBC2 RBC1 RBC0 RBCL R</td>
</tr>
<tr>
<td>25H</td>
<td>XAD2 W</td>
</tr>
<tr>
<td>26H</td>
<td>SAPR R</td>
</tr>
<tr>
<td>26H</td>
<td>SAP1 W</td>
</tr>
<tr>
<td>27H</td>
<td>RDA RDO CRC RAB SA1 SA0 C/R TA RSTA R</td>
</tr>
<tr>
<td>27H</td>
<td>SAP2 W</td>
</tr>
<tr>
<td>28H</td>
<td>TEI1 EA</td>
</tr>
<tr>
<td>29H</td>
<td>RHCR R</td>
</tr>
<tr>
<td>29H</td>
<td>TEI2 W</td>
</tr>
<tr>
<td>2AH</td>
<td>XAC VN1 VN0 OV RBC1 RBC1 RBC9 RBC8 RHCR R</td>
</tr>
<tr>
<td>2BH</td>
<td>0 0 0 0 WFA 0 TREC SDET STAR R</td>
</tr>
</tbody>
</table>
### Table 16
Register Summary: Special Purpose Register IOM®-1 Mode

**IOM®-1:**

<table>
<thead>
<tr>
<th>30H</th>
<th>SPU</th>
<th>SAC</th>
<th>SPM</th>
<th>TLP</th>
<th>C1C1</th>
<th>C1C0</th>
<th>C2C1</th>
<th>C2C0</th>
<th>SPCR</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>31H</td>
<td>0</td>
<td>BAS</td>
<td></td>
<td></td>
<td>CODR</td>
<td></td>
<td></td>
<td></td>
<td>CIC0</td>
<td>0</td>
</tr>
<tr>
<td>31H</td>
<td>RSS</td>
<td>BAC</td>
<td></td>
<td></td>
<td>CODX</td>
<td>TCX</td>
<td>ECX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32H</td>
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<td>32H</td>
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<td>36H</td>
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<td>38H</td>
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</tbody>
</table>

SIEMENS

Register Description

Semiconductor Group
# Register Description

## Table 17
Register Summary: Special Purpose Register IOM®-2 Mode

### IOM®-2:

<table>
<thead>
<tr>
<th>Address</th>
<th>SPU</th>
<th>0</th>
<th>SPM</th>
<th>TLP</th>
<th>C1C1</th>
<th>C1C0</th>
<th>C2C1</th>
<th>C2C0</th>
<th>SPCR</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>30H</td>
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</tr>
<tr>
<td>31H</td>
<td>0</td>
<td></td>
<td>BAS</td>
<td></td>
<td>CODR0</td>
<td>CIC0</td>
<td>CIC1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31H</td>
<td>RSS</td>
<td></td>
<td>BAC</td>
<td></td>
<td>CODX0</td>
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</tr>
</tbody>
</table>

**Legend:**
- **SPU**: Spurious Pulse Disable
- **SPM**: Spurious Pulse Mode
- **TLP**: Timing Line Pulse
- **C1C0/C1C1**: Selectable Clock Input
- **C2C0/C2C1**: Selectable Clock Output
- **SPCR**: Spurious Pulse Control Register
- **CIR0/CIR1**: Clock Input Register
- **CIX0/CIX1**: Clock Output Register
- **MOR0/MOR1**: Mode Register
- **MOX0/MOX1**: Mode Output Register
- **C1R**: Clock 1 Register
- **C2R**: Clock 2 Register
- **B1CR/B2CR**: Baseline 1/2 Control Register
- **STCR**: Strobe Control Register
- **WTC2**: Word Timing Control 2
- **CI1E/IDC**: Clock Input 1/Enable
- **CSEL**: Clock Select
- **BAC**: Baseline Adjust
- **ST1/ST0**: Strobe 1/0
- **SC1/SC0**: Select 1/0
- **STF**: Strobe Fallback
- **TBA2/TBA1/TBA0**: Timing Baseline 2/1/0
- **TSF**: Timing Source Fallback
- **TBA2/TBA1/TBA0**: Timing Baseline 2/1/0
- **TBA0**: Timing Baseline 0
- **ST1/ST0**: Strobe 1/0
- **SC1/SC0**: Select 1/0
- **C1C0/C1C1**: Selectable Clock Input
- **C2C0/C2C1**: Selectable Clock Output
- **STCR**: Strobe Control Register
- **ADF1**: Address Fallback 1
- **ADF2**: Address Fallback 2
- **MOS**: MOS bit
- **MOC**: MOS Output Control
- **MER1/MDA1/MAB1/MDR0/MER0/MDA0/MAB0**: Address Register
- **MRC1/MIE1/MXC1/MRE0/MRC0/MIE0/MXC0**: Output Control Register

*Semiconductor Group 116*
### 4.1 HDLC Operation and Status Registers

#### 4.1.1 Receive FIFO

**RFIFO Read Address 00-1FH**

A read access to any address within the range 00-1FH gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each read access. This allows for the use of efficient “moving string” type commands by the processor.

The RFIFO contains up to 32 bytes of received frame.

After an ISTA:RPF interrupt, exactly 32 bytes are available.

After an ISTA:RME interrupt, the number of bytes available can be obtained by reading the RBCL register.

#### 4.1.2 Transmit FIFO

**XFIFO Write Address 00-1FH**

A write access to any address within the range 00-1FH gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each write access. This allows for the use of efficient “move string” type commands by the processor.

Up to 32 bytes of transmit data can be written into the XFIFO following an ISTA:XPR interrupt.

#### 4.1.3 Interrupt Status Register

**ISTA Read Address 20H**

Value after reset: 00H

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>RME: Receive Message End</td>
</tr>
<tr>
<td>1</td>
<td>RPF: Receive Poll Full</td>
</tr>
<tr>
<td>2</td>
<td>SIC: Start of Information</td>
</tr>
<tr>
<td>3</td>
<td>CIC: Check Information</td>
</tr>
<tr>
<td>4</td>
<td>SIN: Start of Information Acknowledged</td>
</tr>
<tr>
<td>5</td>
<td>EXI: End of Information Acknowledged</td>
</tr>
<tr>
<td>6</td>
<td>TIN: Transmit Information</td>
</tr>
<tr>
<td>7</td>
<td>XPR: Transmit Poll Ready</td>
</tr>
</tbody>
</table>

**RME**

Receive Message End

One complete frame of length less than or equal to 32 bytes, or the last part of a frame of length greater than 32 bytes has been received. The contents are available in the RFIFO. The message length and additional information may be obtained from RBCH+RBCL and the RSTA register.

**RPF**

Receive Poll Full

A 32-byte block of a frame longer than 32 bytes has been received and is available in the RFIFO. The frame is not yet complete.
### Register Description

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
</table>
| **RSC** | Receive Status Change. Used in auto mode only.  
A status change in the receiver of the remote station – Receiver Ready/Receiver Not Ready - has been detected (RR or RNR S-frame). The actual status of the remote station can be read from the STAR register (RRNR bit). |
| **XPR** | Transmit Pool Ready  
A data block of up to 32 bytes can be written to the XFIFO.  
An XPR interrupt will be generated in the following cases:  
– after an XTF or XIF command, when one transmit pool is emptied and the frame is not yet complete  
– after an XTF together with an XME command is issued, when the whole transparent frame has been transmitted  
– after an XIF together with an XME command is issued, when the whole I frame has been transmitted and a positive acknowledgment from the remote station has been received, (auto mode). |
| **TIN** | Timer Interrupt  
The internal timer and repeat counter has expired (see TIMR register). |
| **CIC** | Channel Change  
A change in C/I channel 0 or C/I channel 1 (only in IOM-2 TE mode) has been recognized. The actual value can be read from CIR0 or CIR1. |
| **SIN** | Synchronous Transfer Interrupt  
When programmed (STCR register), this interrupt is generated to enable the processor to lock on to the IOM timing, for synchronous transfers. |
| **EXI** | Extended Interrupt  
This bit indicates that one of six non-critical interrupts has been generated. The exact interrupt cause can be read from EXIR. |

**Note:** A read of the ISTA register clears all bits except EXI and CISQ. EXI is cleared by the reading of EXIR register, CISQ is cleared by reading CIRR/CIR0.
4.1.4 Mask Register

Mask Register
Write
Address 20H

<table>
<thead>
<tr>
<th>Mask</th>
<th>Value after reset: 00H</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
</tr>
</tbody>
</table>

| RME | RPF | RSC | XPR | TIN | CIC | SIN | EXI |

Each interrupt source in the ISTA register can be selective masked by setting to “1” the corresponding bit in MASK. Masked interrupt status bits are not indicated when ISTA is read. Instead, they remain internally stored and pending, until the mask bit is reset to zero.

**Note:** In the event of an extended interrupt and of a C/I or S/Q channel change, EXI and CIC are set in ISTA even if the corresponding mask bits in MASK are active, but no interrupt (INT pin) is generated.

4.1.5 Status Register

Status Register
Read
Address 2H

<table>
<thead>
<tr>
<th>Status</th>
<th>Value after reset: 48H</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
</tr>
</tbody>
</table>

| XDOV | XFW | XRN0 | RRN | MBR | MAC | BVS | MAC0 |

**XDOV**
Transmit Data Overflow
More than 32 bytes have been written in one pool of the XFIFO, i.e. data has been overwritten.

**XFW**
Transmit FIFO Write Enable
Data can be written in the XFIFO. This bit may be polled instead of (or in addition to) using the XPR interrupt.

**XRN0**
Transmit RNR. Used in auto mode only
In auto mode, this bit indicates whether the ICC-B receiver is in the “ready” (0) or “not ready” (1) state. When “not ready”, the ICC-B sends an RNR S-frame autonomously to the remote station when an I frame or an S frame is received.

**RRN0**
Receive RNR. Used in auto mode only.
In the auto mode, this bit indicates whether the ICC-B has received an RR or an RNR frame, this being an indication of the current state of the remote station: receiver ready (0) or receiver not ready (1).
MBR  Message Buffer Ready
This bit signifies that temporary storage is available in the RFIFO to receive
at least the first 16 bytes of a new message.

MAC1  MONITOR Transmit Channel 1 Active (IOM-2 terminal mode only)
Data transmission is in progress in MONITOR channel 1.

BVS  B channel valid on SIP (IOM-1 mode only). B channel on SIP (SLD)
can be accessed.

MAC0  MONITOR Transmit Channel 0 Active. Used in IOM-2 mode only.
Data transmission is in progress in MONITOR channel 0.

4.1.6 Command Register

<table>
<thead>
<tr>
<th>CMDR</th>
<th>Write</th>
<th>Address 2H</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Note: The maximum time between writing to the CMDR register and the execution
of the command is 2.5 DCL clock cycles. During this time no further
commands should be written to the CMDR register to avoid any loss of
commands.

RMC  Receive Message Complete
Reaction to RPF (Receive Pool Full) or RME (Receive Message End)
interrupt. By setting this bit, the processor confirms that it has fetched the
data, and indicates that the corresponding space in the RFIFO may be
released.

RRES  Receiver Reset
HDLC receiver is reset, the RFIFO is cleared of any data.
In addition, in auto mode, the transmit and receive counters (V(S), V(R))
are reset.

RNR  Receiver Not Ready. Used in auto mode only.
Determines the state of the ICC-B HDLC receiver.
When RNR=“0”, a received I or S-frame is acknowledged by an RR
supervisory frame, otherwise by an RNR supervisory frame.

STI  Start Timer.
The ICC-B hardware timer is started when STI is set to one. In the internal
timer mode (TMD bit, MODE register) an S Command (RR, RNR) with poll bit
set is transmitted in addition. The timer may be stopped by a write of the
TIMR register.
XTF  Transmit Transparent Frame  
After having written up to 32 bytes in the XFIFO, the processor initiates the transmission of a transparent frame by setting this bit to “1”. The opening flag is automatically added to the message by the ICC-B.

XIF  Transmit I Frame. Used in auto mode only  
After having written up to 32 bytes in the XFIFO, the processor initiates the transmission of an I frame by setting this bit to “1”. The opening flag, the address and the control field are automatically added by the ICC-B.

XME  Transmit Message End  
By setting this bit to “1” the processor indicates that the data block written last in the XFIFO complete the corresponding frame. The ICC-B terminates the transmission by appending the CRC and the closing flag sequence to the data.

XRES  Transmitter Reset  
HDLC transmitter is reset and the XFIFO is cleared of any data. This command can be used by the processor to abort a frame currently in transmission.

Notes: ● After an XPR interrupt further data has been written in the XFIFO and the appropriate Transmit Command (XTF or XIF) has to be written in the CMDR register again to continue transmission, when the current frame is not yet complete (see also XPR in ISTA).
● During frame transmission, the 0-bit insertion according to the HDLC bit-stuffing mechanism is done automatically.

4.1.7 Mode Register  
Value after reset: 00H

<table>
<thead>
<tr>
<th>Mode Select (MDS2-0)</th>
<th>MDS</th>
<th>MDS</th>
<th>MDS</th>
<th>TMD</th>
<th>RAC</th>
<th>DIM2</th>
<th>DIM1</th>
<th>DIM0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
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<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Determine the message transfer mode of the HDLC controller, as follows:
**Register Description**

<table>
<thead>
<tr>
<th>MDS2 MDS1 MDS0</th>
<th>Mode</th>
<th>Number of Address Bytes</th>
<th>Address Comparison 1.Byte</th>
<th>Address Comparison 2.Byte</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>Auto mode</td>
<td>1</td>
<td>TEI1,TEI2</td>
<td>–</td>
<td>One-byte address compare. HDLC protocol handling for frames with address TEI1</td>
</tr>
<tr>
<td>0 0 1</td>
<td>Auto mode</td>
<td>2</td>
<td>SAP1,SAP2,SAPG</td>
<td>TEI1,TEI2,TEIG</td>
<td>Two-byte address compare. LAPD protocol handling for frames with address SAP1 + TEI1</td>
</tr>
<tr>
<td>0 1 0</td>
<td>Non-Auto mode</td>
<td>1</td>
<td>TEI1,TEI2</td>
<td>–</td>
<td>One-byte address compare.</td>
</tr>
<tr>
<td>0 1 1</td>
<td>Non-Auto mode</td>
<td>2</td>
<td>SAP1,SAP2,SAPG</td>
<td>TEI1,TEI2,TEIG</td>
<td>Two-byte address compare.</td>
</tr>
<tr>
<td>1 0 0</td>
<td>Reserved</td>
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</tr>
<tr>
<td>1 0 1</td>
<td>Transparent mode 1</td>
<td>&gt;1</td>
<td>–</td>
<td>TEI1,TEI2,TEIG</td>
<td>Low-byte address compare.</td>
</tr>
<tr>
<td>1 1 0</td>
<td>Transparent mode 2</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>No address compare. All frames accepted.</td>
</tr>
<tr>
<td>1 1 1</td>
<td>Transparent mode 3</td>
<td>&gt;1</td>
<td>SAP1,SAP2,SAPG</td>
<td>–</td>
<td>High-byte address compare.</td>
</tr>
</tbody>
</table>

**Note:**
SAP1, SAP2: two programmable address values for the first received address byte (in the case of an address field longer than 1 byte); SAPG = fixed value FC / FEH.

TEI1, TEI2: two programmable address values for the second (or the only, in the case of a one-byte address) received address byte; TEIG = fixed value FFH.

**TMD**
Sets the operating mode of the ICC-B timer. In the external mode (0) the timer is controlled by the processor. It is started by setting the STI bit in CMDR and it is stopped by a write of the TIMR register.

In the internal mode (1) the timer is used internally by the ICC-B for timeout and retry conditions (handling of LAPD/HDLC protocol in auto mode).
RAC  Receiver Active
The HDLC receiver is activated when this bit is set to “1”.

DIM2-0  Digital Interface Mode
These bits define the characteristics of the IOM Data Ports (IDP0, IDP1) according to following tables:

**IOM®-1 Modes (ADF2:IMS = 0)**

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>DIM2-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td>IOM frame structure</td>
<td>x</td>
</tr>
<tr>
<td>HDLC interface</td>
<td></td>
</tr>
<tr>
<td>MONITOR channel used for TIC bus access</td>
<td>x</td>
</tr>
<tr>
<td>MONITOR channel used for data transfer</td>
<td></td>
</tr>
<tr>
<td>MONITOR channel stop/go bit evaluated for D-channel access handling</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1) If the TIC bus access handling is not required, i.e. if only one layer-2 device occupies the D and C/I channel, the TIC bus address should be programmed to “111” e.g. STCR = 70H.

2) This function must be selected if the ICC controls an S layer-1 device (SBC PEB 2080) in a TE configuration.
### IOM®-2 Modes (ADF2:IMS = 1)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4-7</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOM -2 terminal mode</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>SPCR:SPM = 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOM -2 non-terminal mode</td>
<td></td>
<td></td>
<td>x</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>SPCR:SPM = 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Last octet of IOM channel 2 used for TIC bus access</td>
<td>x</td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stop/go bit evaluated for D-channel access handling¹)</td>
<td></td>
<td>x</td>
<td>x</td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** ¹) This function must be selected if the ICC controls an S layer-1 device (SBCX PEB 2081) in a TE configuration.

### 4.1.8 Timer Register

**TIMR**

Read/Write  Address 23H

Value after reset: undefined (previous value)

<table>
<thead>
<tr>
<th>CONT</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**CNT**

The meaning depends on the selected timer mode (TMD bit, MODE register).

* **Internal Timer Mode (TMD = 1)**

CNT indicates the maximum number of S commands “N1” which are transmitted autonomously by the ICC after expiration of time period T1 (retry, according to HDLC).
The internal timer procedure will be **started** in auto mode:

- after start of an I-frame transmission

or

- after an "RNR" S frame has been received.

After the last retry, a timer interrupt (TIN-bit in ISTA) is generated.

The timer procedure will be **stopped** when

- a TIN interrupt is generated. The time between the start of an I-frame transmission or reception of an "RNR" S frame and the generation of a TIN interrupt is equal to: \((\text{CNT} + 1) \times T1\).

- or the TIMR is written

- or a positive or negative acknowledgement has been received.

**Note:** The maximum value of CNT can be 6. If CNT is set to 7, the number of retries is unlimited.

**External Timer Mode (TMD = 0)**

CNT together with VALUE determine the time period \(T2\) after which a TIN interrupt will be generated:

\[
\text{CNT} \times 2.048 \text{ s} + T1
\]

with \(T1 = (\text{VALUE} + 1) \times 0.064 \text{ s} ,\)

in the normal case, and

\[
T2 = 16348 \times \text{CNT} \times \text{DCL} + T1
\]

with \(T1 = 512 \times (\text{VALUE} + 1) \times \text{DCL}\)

when \(TLP = 1\) (test loop activated, SPCR register).

DCL denotes the period of the DCL clock.

The timer can be started by setting the STI-bit in CMDR and will be stopped when a TIN interrupt is generated or the TIMR register is written.

**Note:** If CNT is set to 7, a TIN interrupt is indefinitely generated after every expiration of T1.

**VALUE**

Determines the time period \(T1\):

\[
T1 = (\text{VALUE} + 1) \times 0.064 \text{ s} \quad (\text{SPCR}:TLP = 0, \text{ normal mode})
\]

\[
T1 = 512 \times (\text{VALUE} + 1) \times \text{DCL} \quad (\text{SPCR}:TLP = 1, \text{ test mode}).
\]
4.1.9 Extended Interrupt Register

EXIR  Read  Address 24H

Value after reset: 00H.

<p>| | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>XMR</td>
<td>XDU</td>
<td>PCE</td>
<td>RFO</td>
<td>SOV</td>
<td>MOS</td>
<td>SAW</td>
<td>WOV</td>
</tr>
</tbody>
</table>

XMR  Transmit Message Repeat

The transmission of the last frame has to be repeated because:

– the ICC-B has received a negative acknowledgment to an I frame in auto mode (according to HDLC/LAPD)

– or a collision on the S bus has been detected after the 32nd data byte of a transmit frame.

XDU  Transmit Data Underrun

The current transmission of a frame is aborted by transmitting seven “1’s” because the XFIFO holds no further data. This interrupt occurs whenever the processor has failed to respond to an XPR interrupt (ISTA register) quickly enough, after having initiated a transmission and the message to be transmitted is not yet complete.

Note: When a XMR or an XDU interrupt is generated, it is not possible to send transparent frames or I frames until the interrupt has been acknowledged by reading EXIR.

PCE  Protocol Error. Used in auto mode only.

A protocol error has been detected in auto mode due to a received

– S or I frame with an incorrect sequence number N (R) or

– S frame containing an I field.

RFO  Receive Frame Overflow

The received data of a frame could not be stored, because the RFIFO is occupied. The whole message is lost.

This interrupt can be used for statistical purposes and indicates that the processor does not respond quickly enough to an RPF or RME interrupt (ISTA).

SOV  Synchronous Transfer Overflow

The synchronous transfer programmed in STCR has not been acknowledged in time via the SC0/SC1 bit.

MOS  MONITOR Status

A change in the MONITOR Status Register (MOSR) has occurred (IOM-2).

A new MONITOR channel byte is stored in MOR0 (IOM-1).
SAW  Subscriber Awake. Used only if terminal specific functions are enabled (STCR:TSF = 1).

Indicates that a falling edge on the EAW line has been detected, in case the terminal specific functions are enabled (TSF-bit in STCR).

WOV  Watchdog Timer Overflow. Used only if terminal specific functions are enabled (STCR:TSF = 1).

Signals the expiration of the watchdog timer, which means that the processor has failed to set the watchdog timer control bits WTC1 and WTC2 (ADF1 register) in the correct manner. A reset pulse has been generated by the ICC-B.

4.1.10  Transmit Address 1  XAD1  Write  Address 24H

<table>
<thead>
<tr>
<th>Command</th>
<th>Response</th>
<th>Transmitting End</th>
<th>CRI Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>subscriber</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>network</td>
<td>0</td>
</tr>
</tbody>
</table>

Used in auto mode only.

XAD1 contains a programmable address byte which is appended automatically to the frame by the ICC-B in auto mode. Depending on the selected address mode XAD1 is interpreted as follows:

* 2-Byte Address Field

XAD1 is the high byte (SAPI in the ISDN) of the 2-byte address field. Bit 1 is interpreted as the command/response bit “C/R”. It is automatically generated by the ICC-B following the rules of ISDN LAPD protocol and the CRI bit value in SAP1 register. Bit 1 has to be set to “0”.

* 1-Byte Address Field

According to the X.25 LAPB protocol, XAD1 is the address of a command frame.

**Note:** In standard ISDN applications only 2-byte address fields are used.
4.1.11 Receive Frame Byte Count Low  RBCL  Read  Address 25H

Value after reset: 00H

<table>
<thead>
<tr>
<th>RBC7</th>
<th>...</th>
<th>...</th>
<th>...</th>
<th>...</th>
<th>...</th>
<th>...</th>
<th>RBC0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

RBC7-0  Receive byte Count

Eight least significant bits of the total number of bytes in a received message. Bits RBC4-0 indicate the length of a data block currently available in the RFIFO, the other bits (together with RBCH) indicate the number of whole 32-byte blocks received.

If exactly 32 bytes are received RBCL holds the value 20H.

4.1.12 Transmit Address 1  XAD2  Write  Address 25H

<table>
<thead>
<tr>
<th>XAD2</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
</table>

Used in auto mode only.

XAD2 contains the second programmable address byte, whose function depends on the selected address mode:

* 2-Byte Address Field

XAD2 is the low byte (TEI in the ISDN) of the 2-byte address field.

* 1-Byte Address Field

According to the X.25 LAPB protocol, XAD2 is the address of a response frame.

Note: See note to XAD1 register description.
4.1.13 Received SAPI Register

SAPR Read Address 26H

| 7 | 0 |

When a transparent mode 1 is selected SAPR contains the value of the first address byte of a receive frame.

4.1.14 SAPI1 Register

SAPI1 Write Address 26H

| 7 | 0 |

SAPI1 value

Value of the first programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD protocol.

CRI Command/Response Interpretation

CRI defines the end of the ISDN user-network interface the ICC-B is used on, for the correct identification of “Command” and “Response” frames. Depending on the value of CRI the C/R-bit will be interpreted by the ICC-B, when receiving frames in auto mode, as follows:

<table>
<thead>
<tr>
<th>CRI Bit</th>
<th>Receiving End</th>
<th>Command</th>
<th>Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>subscriber</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>network</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

For transmitting frames in auto mode, the C/R-bit manipulation will also be done automatically, depending on the value of the CRI-bit (refer to XAD1 register description).

In message transfer modes with SAPI address recognition the first received address byte is compared with the programmable values in SAP1, SAP2 and the fixed group SAPI.

In 1-byte address mode, the CRI-bit is to be set to “0”.
4.1.15 Receive Status Register  

**Value after reset:** undefined

<p>| | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>RDA</td>
<td>RDO</td>
<td>CRC</td>
<td>RAB</td>
<td>SA1</td>
<td>SA0</td>
<td>C/R</td>
<td>TA</td>
</tr>
</tbody>
</table>

**RDA**  
Receive Data  
A “1” indicates that data is available in the RFIFO. After an RME-interrupt, a “0” in this bit means that data is available in the internal registers RHCR or SAPR only (e.g. S-frame). See also RHCR-register description table.

**RDO**  
Receive Data Overflow  
At least one byte of the frame has been lost, because it could not be stored in RFIFO (1).

**CRC**  
CRC Check  
The CRC is correct (1) or incorrect (0).

**RAB**  
Receive Message Aborted  
The receive message was aborted by the remote station (1), i.e. a sequence of 7 1’s was detected before a closing flag.

**SA1-0**  
SAPI Address Identification  
SA1-0 are significant in auto-mode and non-auto-mode with a two-byte address field, as well as in transparent mode 3. TA is significant in all modes except in transparent modes 2 and 3.

**TA**  
TEI Address Identification  
Two programmable SAPI values (SAP1, SAP2) plus a fixed group SAPI (SAPG of value FC/FEH), and two programmable TEI values (TEI1, TEI2) plus a fixed group TEI (TEIG of value FFH), are available for address comparison.
The result of the address comparison is given by SA1-0 and TA, as follows:

<table>
<thead>
<tr>
<th>Number of Address Bytes=1</th>
<th>1st Byte</th>
<th>2nd Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>x x 0</td>
<td>TEI2</td>
<td>-</td>
</tr>
<tr>
<td>x x 1</td>
<td>TEI1</td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Number of address Bytes=2</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>SAP2</td>
<td>TEIG</td>
</tr>
<tr>
<td>0 0 1</td>
<td>SAP2</td>
<td>TEI2</td>
</tr>
<tr>
<td>0 1 0</td>
<td>SAPG</td>
<td>TEIG</td>
</tr>
<tr>
<td>0 1 1</td>
<td>SAPG</td>
<td>TEI1 or TEI2</td>
</tr>
<tr>
<td>1 0 0</td>
<td>SAP1</td>
<td>TEIG</td>
</tr>
<tr>
<td>1 0 1</td>
<td>SAP1</td>
<td>TEI1</td>
</tr>
<tr>
<td>1 1 x</td>
<td>reserved</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
- If the SAPI values programmed to SAP1 and SAP2 are identical the reception of a frame with SAP2/TEI2 results in the indication SA1=1, SA0-0, TA=1.
- Normally RSTA should be read by the processor after an RME-interrupt in order to determine the status of the received frame. The contents of RSTA are valid only after an RME-interrupt, and remain so until the frame is acknowledged via the RMC-bit.

C/R Command/Response
The C/R-bit identifies a receive frame as either a command or a response, according to the LAPD-rules:

<table>
<thead>
<tr>
<th>Command</th>
<th>Response</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>Subscriber to network</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Network to subscriber</td>
</tr>
</tbody>
</table>

4.1.16 SAP12 Register
SAP2 Write Address 27H

<table>
<thead>
<tr>
<th>SAP12 value</th>
</tr>
</thead>
</table>

Value of the second programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD-protocol.
MCS  Modulo Count Select. Used in auto-mode only.
This bit determines the HDLC-control field format as follows:
0: One-byte control field (modulo 8)
1: Two-byte control field (modulo 128)

4.1.17  TEI1 Register 1  TEI1  Write  Address 28H

<table>
<thead>
<tr>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>E</td>
</tr>
</tbody>
</table>

EA  Address field Extension bit
This bit is set to “1” according to HDLC/LAPD.
In all message transfer modes except in transparent modes 2 and 3, TEI1 is used by the ICC-B for address recognition. In the case of a two-byte address field, it contains the value of the first programmable Terminal Endpoint Identifier according to the ISDN LAPD-protocol.

In the auto-mode with a two-byte address field, numbered frames with the address SAPI1-TEI1 are handled autonomously by the ICC-B according to the LAPD-protocol.

Note: If the value FFH is programmed in TEI1, received numbered frames with address SAPI1-TEI1 (SAPI1-TEIG) are not handled autonomously by the ICC-B.

In auto and non-auto-modes with one-byte address field, TEI1 is a command address, according to X.25 LAPB.

4.1.18  Receive HDLC Control Register  RHCR  Read  Address 29H

<table>
<thead>
<tr>
<th>7</th>
<th>0</th>
</tr>
</thead>
</table>

In all modes except transparent modes 2 and 3, this register contains the control field of a received HDLC-frame. In transparent modes 2 and 3, the register is not used.
### Contents of RHCR

<table>
<thead>
<tr>
<th>Mode</th>
<th>Modulo 8 (MCS=0)</th>
<th>Modulo 128 (MCS=1)</th>
<th>Contents of RFIFO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto-mode, 1-byte address (U/I frames) (Note 1)</td>
<td>Control field</td>
<td>U-frames only:</td>
<td>From 3&lt;sup&gt;rd&lt;/sup&gt; byte after flag (Note 4)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Control field</td>
<td></td>
</tr>
<tr>
<td>Auto-mode, 2-byte address (U/I frames) (Note 1)</td>
<td>Control field</td>
<td>U-frames only:</td>
<td>From 4&lt;sup&gt;th&lt;/sup&gt; byte after flag (Note 4)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Control field</td>
<td></td>
</tr>
<tr>
<td>Auto-mode, 1-byte address (I frames)</td>
<td></td>
<td>Control field</td>
<td>From 4&lt;sup&gt;th&lt;/sup&gt; byte after flag (Note 4)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>compressed form</td>
<td></td>
</tr>
<tr>
<td>Auto-mode, 2-byte address (I frames)</td>
<td></td>
<td>Control field</td>
<td>From 5&lt;sup&gt;th&lt;/sup&gt; byte after flag (Note 4)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>in compressed form</td>
<td></td>
</tr>
<tr>
<td>Non-auto-mode, 1-byte address</td>
<td>2&lt;sup&gt;nd&lt;/sup&gt; byte after flag</td>
<td>From 3&lt;sup&gt;rd&lt;/sup&gt; byte after flag</td>
<td></td>
</tr>
<tr>
<td>Non-auto-mode, 2-byte address</td>
<td>3&lt;sup&gt;rd&lt;/sup&gt; byte after flag</td>
<td>From 4&lt;sup&gt;th&lt;/sup&gt; byte after flag</td>
<td></td>
</tr>
<tr>
<td>Transparent mode 1</td>
<td>3&lt;sup&gt;rd&lt;/sup&gt; byte after flag</td>
<td>From 4&lt;sup&gt;th&lt;/sup&gt; byte after flag</td>
<td></td>
</tr>
<tr>
<td>Transparent mode 2</td>
<td>–</td>
<td>From 1&lt;sup&gt;st&lt;/sup&gt; byte after flag</td>
<td></td>
</tr>
<tr>
<td>Transparent mode 3</td>
<td>–</td>
<td>From 2&lt;sup&gt;nd&lt;/sup&gt; byte after flag</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1**  
S-frames are handled automatically and are not transferred to the microprocessor.

**Note 2**  
For U-frames (bit 0 of RHCR = 1) the control field is as in the modulo 8 case.

**Note 3**  
For I-frames (bit 0 of RHCR = 0) the compressed control field has the same format as in the modulo 8 case, but only the three LSB’s of the receive and transmit counters are visible:

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>N (R)</td>
<td>2-0</td>
<td>P</td>
<td>N (S)</td>
<td>2-0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 4**  
I-field.
4.1.19 TEI2 Register

<table>
<thead>
<tr>
<th>TEI2 Write</th>
<th>Address 29H</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
</tr>
</tbody>
</table>

**EA**  
Address field Extension bit  
This bit is to be set to “1” according to HDLC/LAPD.

In all message transfer modes except in transparent modes 2 and 3, TEI2 is used by the ICC-B for address recognition. In the case of a two-byte address field, it contains the value of the second programmable Terminal Endpoint Identifier according of the ISDN LAPD-protocol.

In auto and non-auto-modes with one-byte address field, TEI2 is a response address, according to X.25 LAPD.

4.1.20 Receive Frame Byte Count High

**RBCH**  
Read  
Address 30H

Value after reset: 0XXX00000₂.

<table>
<thead>
<tr>
<th>XAC</th>
<th>VN1</th>
<th>VN0</th>
<th>OV</th>
<th>RBC11</th>
<th>RBC10</th>
<th>RBC9</th>
<th>RBC8</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**XAC**  
Transmitter Active  
The HDLC-transmitter is active when XAC = 1. This bit may be polled. The XAC-bit is active when
– either an XTF/XIF-command is issued and the frame has not been completely transmitted
– or the transmission of an S-frame is internally initiated and not yet completed.

**VN1-0**  
Version Number of Chip  
0 ... A1 or A3 version  
1 ... B1 version  
2 ... B2 & B3 version  
3 ... Version 2.4

**OV**  
Overflow  
A “1” in this bit position indicates a message longer than 4095 bytes.

**RBC8-11**  
Receive Byte Count  
Four most significant bits of the total number of bytes in a received message.
Note: Normally RBCH and RBCL should be read by the processor after an RME-interrupt in order to determine the number of bytes to be read from the RFIFO, and the total message length. The contents of the registers are valid only after an RME-interrupt, and remain so until the frame is acknowledged via the RMC-bit.

4.1.21 Status Register 2

<table>
<thead>
<tr>
<th>Address 2BH</th>
<th>STAR2</th>
<th>Read</th>
</tr>
</thead>
</table>

| 7 | 0 |

0 0 0 0 WFA 0 TREC SDET

SDET S-frame detected: this bit is set to “1” by the first received correct I-frame or S-command with p = 1. It is reset by reading the STAR2 register.

TREC Timer recovery status:
0: The device is not in the Timer Recovery state.
1: The device is in the Timer Recovery state.

WFA Waiting for Acknowledge. This bit shows, if the last transmitted I-frame was acknowledged, i.e. $V(A) = V(S)$ (=>$WFA = 0$) or was not yet acknowledged, i.e. $V(A) < V(S)$ (=>$WFA = 1$).

4.2 Special Purpose Registers: IOM-1Mode

The following register description is only valid if IOM-1 Mode is selected (ADF2:IMS = 0). For IOM-2 Mode refer to chapter 4.3.

4.2.1 Serial Port Control Register

<table>
<thead>
<tr>
<th>Address 30H</th>
</tr>
</thead>
</table>

Value after reset: 00H

| 7 | 0 |

SPU SAC SPM TLP C1C1 C1C0 C2C1 C2C0

Important Note After a hardware reset the pins SDAX/SDS1 and SCA/FSD/SDS2 are both “low” and have the functions of SDS1 and SDS2 in terminal timing mode (since SPM = 0), respectively, until the SPCR is written to for the first time. From that moment, the function taken on by these pins depends on the state of the IOM Mode Select bit IMS (ADF2 register).
SPU  Software Power Up. Used in TE-mode only.

Setting this bit to 1 will pull the IDP1-line low. This will enforce the connected layer-1 device to deliver IOM-clocking.

After power down in TE-mode the SPU-bit has to be set to “1” and then cleared again.

After a subsequent CIC-interrupt (C/I-code change; ISTA) and reception of the C/I-code “PU” (Power Up indication in TE-mode) the reaction of the processor would be:
- to write an Activate Request command as C/I-code in the CIXR-register
- to reset the SPU-bit and wait for the following CIC-interrupt.

SAC  SIP-port activation; SIP-port is in high impedance state (SAC=0) or operating (SAC=1).

SPM  Serial Port Timing Mode; Depending on the interface mode, the following timing options are provided.

0  Timing mode 0; SIP (SLD) operates in master mode, SCA-supplies the 128-kHz data clock signal for port A (SSI).
    Typical applications: TE, NT-modes

1  Timing mode 1; SIP (SLD) operates in slave mode, FSD supplies a delayed frame synchronization signal for the IOM interface, serial port A (SSI) is not used.
    Typical applications: LT-T, LT-S-modes.

TLP  Test Loop

When set to 1 the IDP1 and IDP0 lines are internally connected together, and the times T1 and T2 are reduced (cf. TIMR).

C1C1, C1C0  Channel 1 Connect

Switching of B1 channel

<table>
<thead>
<tr>
<th>C1C1</th>
<th>C1C0</th>
<th>C1R</th>
<th>B1CR</th>
<th>Application(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>SIP</td>
<td>SIP</td>
<td>IOM</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>SIP</td>
<td>–</td>
<td>IOM</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>SDAR</td>
<td>–</td>
<td>IOM</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>IOM</td>
<td>IOM</td>
<td>–</td>
</tr>
</tbody>
</table>

Semiconcuctor Group 136
C2C1, C2C0   Channel 2 Connect
Switching of B2-channel

<table>
<thead>
<tr>
<th>C2R</th>
<th>B2CR</th>
<th>Read</th>
<th>Write</th>
<th>Read</th>
<th>Application(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>SIP</td>
<td>SIP</td>
<td>IOM</td>
<td>B2 not switched, SIP-looping</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>SIP</td>
<td>–</td>
<td>IOM</td>
<td>B2 switched to/from SIP</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>SDAR</td>
<td>–</td>
<td>IOM</td>
<td>B2 switched to/from SPA (SSI)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>IOM</td>
<td>IOM</td>
<td>–</td>
<td>IOM-looping</td>
</tr>
</tbody>
</table>

4.2.2 Command/Indication Receive Register  CIRR  Read  Address 31H

Value after reset: 7CH.

<table>
<thead>
<tr>
<th></th>
<th>BAS</th>
<th>C</th>
<th>O</th>
<th>D</th>
<th>R</th>
<th>CIC0</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

BAS   Bus Access Status
Indicates the state of the TIC-bus:
0: the ICC-B itself occupies the D-and C/I-channel
1: another device occupies the D-and C/I-channel

CODR  C/I-code Receive
Value of the receive Command/Indication code. A C/I-code is loaded in CODR
only after being the same in two consecutive IOM-frames and the previous
code has been read from CIRR.

CIC0  C/I-Code Change
A change in the received Command/Indication code has been recognized.
This bit is set only when a new code is detected in two consecutive IOM-frames.
It is reset by a read of CIRR.

Note: The BAS and CODR bits are updated every time a new C/I-code is detected
in two consecutive IOM-frames.
If several consecutive codes are detected and CIRR is not read, only the first
and the last C/I-code (and BAS bit) is made available in CIRR at the first and
second read of that register, respectively.
4.2.3 Command/Indication Transmit Register

Value after reset: 3CH.

<table>
<thead>
<tr>
<th>RSS</th>
<th>BAC</th>
<th>C</th>
<th>O</th>
<th>D</th>
<th>X</th>
<th>TCX</th>
<th>ECX</th>
</tr>
</thead>
</table>

**RSS**  
Reset Source Select  
Only valid if the terminal specific functions are activated (STCR:TSF).

0 → **Subscriber or Exchange Awake**

As reset source serves:

- a falling edge on the EAW-line (External Subscriber Awake)
- a C/I-code change (Exchange Awake).

A logical zero on the EAW-line activates also the IOM-interface clock and frame signal, just as the SPU-bit (SPCR) does.

1 → **Watchdog Timer**

The expiration of the watchdog timer generates a reset pulse.

The watchdog timer will be reset and restarted, when two specific bit combinations are written in the ADF1-register within the time period of 128 ms (see also ADF1 register description).

After a reset pulse generated by the ICC-B and the corresponding interrupt (WOV, SAW or CIC) the actual reset source can be read from the ISTA and EXIR-register.

**BAC**  
Bus Access Control  
Only valid if the TIC-bus feature is enabled (MODE:DIM2-0).

If this bit is set, the ICC-B will try to access the TIC-bus to occupy the C/I-channel even if no D-channel frame has to be transmitted. It should be reset when the access has been completed to grant a similar access to other devices transmitting in that IOM-channel.

**Note:** Access is always granted by default to the ICC-B with TIC-bus Address (TBA2-0, STCR register) “7”, which is the lowest priority in a bus configuration.

**CODX**  
C/I-Code Transmit  
Code to be transmitted in the C/I-channel.

**TCX**  
T-channel transmit  
Output on IOM in T-channel.

**ECX**  
E-channel transmit  
Output on IOM in E-channel.
4.2.4 MONITOR Receive Register  MOR  Read  Address 32H

7                      0

Contains the MONITOR data received according to the MONITOR channel protocol (E-bit = 0).

4.2.5 MONITOR Transmit Register  MOX  Write  Address 32H

7                      0

The byte written into MOX is transmitted once in the MONITOR channel.

4.2.6 SIP Signaling Code Receive  SSCR  Read  Address 33H

7                      0

SSCR  SIP-signaling code received; only valid in timing mode 0 (SPCR:SPM = 0).
The signaling byte received on SIP can be read from this register.

4.2.7 SIP Signaling Code Transmit  SSCX  Write  Address 33H

Value after reset: FFH

7                      0
**SSCX**  SIP signaling code transmit; significant only in timing mode 0 (SPCR:SPM = 0).
The contents of SSCX are continuously output in the signaling byte on SIP (SLD).

### 4.2.8 SIP Feature Control Read

**SFCR**  Read  
Address 34H

```
7 0
```
Contains the FC-data received on SIP (timing mode 0 only, SPCR:SPM = 0).

### 4.2.9 SIP Feature Control Write

**SFCW**  Write  
Address 34H

```
7 0
```
The byte written into SFCW is output once on SIP in the FC-channel (timing mode 0 only, SPCR:SPM = 0).

### 4.2.10 Channel Register 1

**C1R**  Read/Write  
Address 35H

```
7 0
```
Contains the value received/transmitted in the B1-channel (cf. C1C1, C1C0, SPCR-register).

### 4.2.11 Channel Register 2

**C2R**  Read/Write  
Address 36H

```
7 0
```
Contains the value received/transmitted in the B2-channel (cf. C2C1, C2C0, SPCR-register).
4.2.12 B1 Channel Register

<table>
<thead>
<tr>
<th>B1CR</th>
<th>Read</th>
<th>Address 37H</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Contains the value received in the B1-channel, as if programmed (cf. C1C1, C1C0, SPCR-register).

4.2.13 Synchronous Transfer Control Register

<table>
<thead>
<tr>
<th>STCR</th>
<th>Write</th>
<th>Address 37H</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Value after reset: 00H

TSF Terminal Specific Functions

<table>
<thead>
<tr>
<th>TSF</th>
<th>TBA2</th>
<th>TBA1</th>
<th>TBA0</th>
<th>ST1</th>
<th>ST0</th>
<th>SC1</th>
<th>SC0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- No terminal specific functions
- The terminal specific functions are activated, such as
  - Watchdog Timer
  - Subscriber/Exchange Awake (SIP/EAW).

In this case the SIP/EAW-line is always an input signal which can serve as a request signal from the subscriber to initiate the awake function in a terminal.

A falling edge on the EAW-line generates an SAW interrupt (EXIR).

When the RSS-bit in the CIXR-register is zero, a falling edge on the EAW-line (Subscriber Awake) or a C/I-code change (Exchange Awake) initiates a reset pulse.

When the RSS-bit is set to one a reset pulse is triggered only by the expiration of the watchdog timer (see also CIXR-register description).

Note: The TSF-bit will be cleared only by hardware reset.

TBA2-0 TIC Bus Address

Defines the individual address for the ICC-B on the IOM-bus.

This address is used to access the C/I and D-channel on the IOM.

Note: One device liable to transmit in C/I and D-fields on IOM should always be given the address value “7”.
ST1  Synchronous Transfer 1
When set, causes the ICC-B to generate an SIN-interrupt status (ISTA register) at the beginning of an IOM-frame.

ST0  Synchronous Transfer 0
When set, causes the ICC-B to generate an SIN-interrupt status (ISTA register) at the middle of an IOM-frame.

SC1  Synchronous Transfer 1 Completed
After an SIN-interrupt the processor has to acknowledge the interrupt by setting the SC1-bit before the middle of the IOM-frame, if the interrupt was originated from a Synchronous Transfer 1 (ST1).
Otherwise an SOV-interrupt (EXIR register) will be generated.

SC0  Synchronous Transfer 0 Completed
After an SIN-interrupt the processor has to acknowledge the interrupt by setting the SC0-bit before the start of the next IOM-frame, if the interrupt was originated from a Synchronous Transfer 0 (ST0).
Otherwise an SOV-interrupt (EXIR register) will be generated.

Note: ST0/1 and SC0/1 are useful for synchronizing MP-accesses and receive/transmit operations.

4.2.14  B2 Channel Register
        B2CR       Read       Address 38H

              7         0

Contains the value received in the B2-channel, as if programmed (cf. C2C1, C2C0, SPCR-register).

4.2.15  Additional Feature Register 1
        ADF1       Write       Address 38H

Value after reset: 00H

              7         0

    WTC1  WTC2  0  0  0  0  0  ITF
WTC1, WTC2  Watchdog Timer Control 1, 2

After the watchdog timer mode has been selected (STCR:TSF = CIXR:RSS = 1) the watchdog timer is started.

During every time period of 128 ms the processor has to program the WTC1- and WTC2-bit in the following sequence:

<table>
<thead>
<tr>
<th></th>
<th>WTC1</th>
<th>WTC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2.</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

to reset and restart the watchdog timer.

If not, timer expires and a WOV-interrupt (EXIR) together with a reset pulse is generated.

ITF  Inter-frame Time Fill

Selects the inter-frame time fill signal which is transmitted between HDLC-frames.

0: idle (continuous 1 s),

1: flags (sequence of patterns: “0111 1110”)

Note: In TE- and LT-T-applications with D-channel access handling (collision resolution), the only possible inter-frame time fill signal is idle (continuous 1s). Otherwise the D-channel on the S/T-bus cannot be accessed.

4.2.16  Additional Feature Register 2  ADF2  Read/Write  Address 39H

Value after reset: 00H

<table>
<thead>
<tr>
<th></th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMS</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

IMS  IOM-mode selection

IOM-1 interface mode is selected when IMS = 0.
4.3 Special Purpose Registers: IOM-2 Mode

The following register description is only valid if IOM-2 is selected (ADF2:IMS-1). For IOM-1 mode refer to chapter 4.2.

4.3.1 Serial Port Control Register  SPCR  Read/Write  Address 30H

Value after reset: 00H

<table>
<thead>
<tr>
<th></th>
<th>SPU</th>
<th>SPM</th>
<th>TLP</th>
<th>C1C1</th>
<th>C1C0</th>
<th>C2C1</th>
<th>C2C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Important Note: After a hardware reset the pins SDAX/SDS1 and SCA/FSD/SDS2 are both “low” and have the functions of SDS1 and SDS2 in terminal timing mode (since SPM = 0), respectively, until the SPCR is written to for the first time. From that moment, the function taken on by these pins depends on the state of the IOM Mode Select bit IMS (ADF2 register).

SPU  Software Power UP. Used in TE-mode only.

Setting this bit to 1 and ADF1:IDC to 1 will pull the IDP1-line to low. This will enforce connected layer 1 devices to deliver IOM-clocking.

After power down in TE-mode the SPU-bit and the ADF1:IDC bit have to be set to “1” and then cleared again.

After a subsequent CIC-interrupt (C/I-code change; ISTA) and reception of the C/I-code “PU” (Power Up indication in TE-mode) the reaction of the processor would be:

– to write an Activate Request command as C/I-code in the CIX0-register.
– to reset the SPU and SQXR:IDC bits and wait for the following CIC-interrupt.

SPM  Serial Port Timing Mode

0  Terminal mode; all three channels of the IOM-2 interface are used
application: TE-mode

1  Non-terminal mode; the programmed IOM-channel (ADF1:CSEL2-0) is used
applications: LT-T, LT-S modes (8 channels structure IOM-2)

TLP  Test Loop

When set to 1 the IDP1 and IDP0-lines are internally connected together, and the times T1 and T2 are reduced (cf. TIMR).
C1C1, C1C0  Channel 1 Connect
Determines which of the two channels B1 or IC1 is connected to register C1R and/or B1CR, for monitoring, test-looping and switching data to/from the processor.

<table>
<thead>
<tr>
<th>C1C1</th>
<th>C1C0</th>
<th>Read</th>
<th>Write</th>
<th>Read</th>
<th>Application(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>IC1</td>
<td>–</td>
<td>B1</td>
<td>B1-monitoring + IC1-monitoring</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>IC1</td>
<td>IC1</td>
<td>B1</td>
<td>B1-monitoring + IC1-looping from/to IOM</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>–</td>
<td>B1</td>
<td>B1</td>
<td>B1-access from/to S0; transmission of a constant value in B1-channel to S0.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>B1</td>
<td>B1</td>
<td>–</td>
<td>B1-looping from S0; transmission of a variable pattern in B1-channel to S0.</td>
</tr>
</tbody>
</table>

C2C1, C2C0  Channel 2 Connect
Determines which of the two channels B2 or IC2 is connected to register C2R and/or B2CR, for monitoring, test-looping and switching data to/from the processor.

<table>
<thead>
<tr>
<th>C2C1</th>
<th>C2C0</th>
<th>Read</th>
<th>Write</th>
<th>Read</th>
<th>Application(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>IC2</td>
<td>–</td>
<td>B2</td>
<td>B2-monitoring + IC2-monitoring</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>IC2</td>
<td>IC2</td>
<td>B2</td>
<td>B2-monitoring + IC2-looping from/to IOM</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>–</td>
<td>B2</td>
<td>B2</td>
<td>B2-access from/to S0; transmission of a constant value in B2-channel to S0.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>B2</td>
<td>B2</td>
<td>–</td>
<td>B2-looping from S0; transmission of a variable pattern in B2-channel to S0.</td>
</tr>
</tbody>
</table>

Note:  B-channel access is only possible in TE-mode.
4.3.2 Command/Indication Receive 0 CIR0 Read Address 31H

Value after reset: 7CH

<table>
<thead>
<tr>
<th>0</th>
<th>BAS</th>
<th>C</th>
<th>O</th>
<th>D</th>
<th>R</th>
<th>0</th>
<th>CIC0</th>
<th>CIC1</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**BAS**  
Bus Access Status  
Indicates the state of the TIC-bus:  
0: the ICC-B itself occupies the D- and C/I-channel  
1: another device occupies the D- and C/I-channel

**CODR0**  
C/I code 0 Receive  
Value of the received Command/Indication code. A C/I-code is loaded in CODR0 only after being the same in two consecutive IOM-frames and the previous code has been read from CIR0.

**CIC0**  
C/I Code 0 Change  
A change in the received Command/Indication code has been recognized. This bit is set only when a new code is detected in two consecutive IOM-frames. It is reset by a read of CIR0.

**CIC1**  
C/I Code 1 Change  
A change in the received Command/Indication code in IOM-channel 1 has been recognized. This bit is set when a new code is detected in one IOM-frame. It is reset by a read of CIR0.  
CIC1 is only used if Terminal Mode is selected.

**Note:** The BAS and CODR0 bits are update every time a new C/I-code is detected in two consecutive IOM-frames.  
If several consecutive valid new codes are detected and CIR0 is not read, only the first and the last C/I code (and BAS bit) is made available in CIR0 at the first and second read of that register, respectively.

4.3.3 Command/Indication Transmit 0 CIX0 Write Address 31H

Value after reset: 3FH

<table>
<thead>
<tr>
<th>7</th>
<th>BAS</th>
<th>C</th>
<th>O</th>
<th>D</th>
<th>X</th>
<th>0</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>RSS</td>
<td>BAC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
RSS  Reset Source Select
Only valid if the terminal specific functions are activated (STCR:TSF).

0  →  **Subscriber or Exchange Awake**
   As reset source serves:
   – a falling edge on the EAW-line (External Subscriber Awake)
   – a C/I code change (Exchange Awake).
   A logical zero on the EAW-line activates also the IOM-interface clock and frame signal, just as the SPU-bit (SPCR) does.

1  →  **Watchdog Timer**
The expiration of the watchdog timer generates a reset pulse.
The watchdog timer will be reset and restarted, when two specific bit combinations are written in the ADF1-register within the time period of 128 ms (see also ADF1 register description).
After a reset pulse generated by the ICC-B and the corresponding interrupt (WOV, SAW or CIC) the actual reset source can be read from the ISTA and EXIR-register.

BAC  Bus Access Control
Only valid if the TIC-bus feature is enabled (MODE:DIM2-0).
If this bit is set, the ICC-B will try to access the TIC-bus to occupy the C/I-channel even if no D-channel frame has to be transmitted. It should be reset when the access has been completed to grant a similar access to other devices transmitting in that IOM-channel.
**Note:** Access is always granted by default to the ICC-B with TIC-Bus Address (TBA2-0, STCR register) “7”, which has the lowest priority in a bus configuration.

CODX0  C/I-Code 0 Transmit
Code to be transmitted in the C/I-channel / C/I-channel 0.

4.3.4  **MONITOR Receive Channel 0**
**MOR0**  Read  **Address 32H**

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>
Contains the MONITOR data received in IOM-MONITOR Channel/MONITOR channel 0 according to the MONITOR channel protocol.
### Register Description

#### 4.3.5 MONITOR Transmit Channel 0  MOX0  Write  Address 32H

<table>
<thead>
<tr>
<th>7</th>
<th>0</th>
</tr>
</thead>
</table>

Contains the MONITOR data transmitted in IOM-MONITOR Channel/MONITOR channel 0 according to the MONITOR channel protocol.

#### 4.3.6 Command/Indication Receive 1  CIR1  Read  Address 33H

<table>
<thead>
<tr>
<th>7</th>
<th>0</th>
</tr>
</thead>
</table>

| C | O | D | R | 1 | MR1 | MX1 |

**CODR1**  C/I-Code 1 Receive; only valid in terminal mode (SPCR:SPM = 0)

Bits 7-2 of C/I-channel 1

**MR1**  MR Bit

Bit 1 of C/I-channel 1

**MX1**  MX Bit

Bit 0 of C/I-channel 1

#### 4.3.7 Command/Indication Transmit 1  CIX1  Write  Address 33H

Value after reset: FFH

<table>
<thead>
<tr>
<th>7</th>
<th>0</th>
</tr>
</thead>
</table>

| C | O | D | X | 1 | 1 | 1 |

**CODX1**  C/I-Code 1 Transmit; significant only in terminal mode (SPCR:SPM = 0).

Bits 7-2 of C/I-channel 1
4.3.8 MONITOR Receive Channel 1 MOR1 Read Address 34H

7 0

Used only in terminal mode (SPCR:SPM = 0).

Contains the MONITOR data received in IOM-channel 1 according to the MONITOR channel protocol.

MONITOR Transmit Channel 1 MOX1 Write Address 34H

7 0

Used only in terminal mode (SPCR:SPM = 0).

Contains the MONITOR data to be transmitted in IOM-channel 1 according to the MONITOR channel protocol.

4.3.9 Channel Register 1 C1R Read/Write Address 35H

7 0

Used only in terminal mode (SPCR:SPM = 0).

Contains the value received/transmitted in IOM-channel B1 or IC1, as the case may be (cf. C1C1, C1C0, SPCR-register).

4.3.11 Channel Register 2 C2R Read/Write Address 36H

7 0

Used only in terminal mode (SPCR:SPM = 0).

Contains the value received/transmitted in IOM-channel B2 or IC2, as the case may be (cf. C2C1, C2C0, SPCR-register).
4.3.12  B1 Channel Register  B1CR  Read  Address 37H

| 7 | 0 |

Used only in terminal mode (SPCR:SPM = 0).

Contains the value received in IOM-channel B1, if programmed (cf. C1C1, C1C0, SPCR-register).

4.3.13  Synchronous Transfer Control Register  STCR  Write  Address 37H

Value after reset: 00H

| 7 | 0 |

TSF  Terminal Specific Functions

0 → No terminal specific functions

1 → The terminal specific functions are activated, such as

   – Watchdog Timer
   – Subscriber/Exchange Awake (SIP/EAW).

   In this case the SIP/EAW-line is always an input signal which can serve as a request signal from the subscriber to initiate the awake function in a terminal.

   A falling edge on the EAW-line generates an SAW-interrupt (EXIR).

   When the RSS-bit in the CIX0-register is zero, a falling edge on the EAW-line (Subscriber Awake) or a C/I-code change (Exchange Awake) initiates a reset pulse.

   When the RSS-bit is set to one a reset pulse is triggered only by the expiration of the watchdog timer (see also CIX0-register description).

Note: The TSF-bit will be cleared only by a hardware reset.
Register Description

TBA2-0  TIC Bus Address
Defines the individual address for the ICC-B on the IOM-bus.
This address is used to access the C/I- and D-channel on the IOM.

Note: One device liable to transmit in C/I- and D-fields on the IOM should always be given the address value “7”.

ST1  Synchronous Transfer 1
When set, causes the ISAC-S to generate an SIN-interrupt status (ISTA-register) at the beginning of an IOM-frame.

ST0  Synchronous Transfer 0
When set, causes the ICC-B to generate an SIN-interrupt status (ISTA-register) at the middle of an IOM-frame.

SC1  Synchronous Transfer 1 Completed
After an SIN-interrupt the processor has to acknowledge the interrupt by setting the SC1-bit before the middle of the IOM-frame, if the interrupt was originated from a Synchronous Transfer 1 (ST1).
Otherwise an SOV-interrupt (EXI- register) will be generated.

SC0  Synchronous Transfer 0 Completed
After an SIN-interrupt the processor has to acknowledge the interrupt by setting the SC0-bit before the start of the next IOM-frame, if the interrupt was originated from a Synchronous Transfer 0 (ST0).
Otherwise an SOV-interrupt (EXI- register) will be generated.

Note: ST0/1 and SC0/1 are useful for synchronizing MP-accesses and receive/transmit operations.

4.3.14 B2 Channel Register B2CR Read Address 38H

<p>| | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Used only in terminal mode (SPC-SPM = 0).

Contains the value received in the IOM-channel B2, if programmed (cf. C2C1, C2C0, SPCR-register).
4.3.15 Additional Feature Register 1

ADF1 Write Address 38H

Value after reset: 00H

<table>
<thead>
<tr>
<th>WTC1</th>
<th>WTC2</th>
<th>CI1E</th>
<th>IDC</th>
<th>CSEL2</th>
<th>CSEL1</th>
<th>CSEL0</th>
<th>ITF</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**WTC1, WTC2**  Watchdog Timer Control 1, 2

After the watchdog timer mode has been selected (STCR:TSF = CIX0:RSS = 1) the watchdog timer is started.

During every time period of 128 ms the processor has to program the WTC1- and WTC2-bit in the following sequence:

<table>
<thead>
<tr>
<th></th>
<th>WTC1</th>
<th>WTC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2.</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

to reset and restart the watchdog timer.

If not, the timer expires and a WOV-interrupt (EXIR) together with a reset pulse is generated.

**CI1E**  C/I-channel 1 interrupt enable

Interrupt generation of CIR0:CIC1 is enabled (1) or masked (0).

**IDC**  IOM-direction control

Terminal mode (SPCR:SPM = 0)

0 ... Master mode

Layer-2 transmits IOM-channel 0 and 2 on IDP1, channel 1 on IDP0.

1 ... Slave mode

Layer-2 transmits IOM-channel 0, 1 and 2 on IDP1.

Non-Terminal mode (SPCR:SPM = 1)

0 ... normal mode

MONITOR, D- and C/I-channels are transmitted on IDP1 from layer-2 to layer-1

1 ... reversed mode

MONITOR, D- and C/I-channels are transmitted on IDP0 from layer-2 to the system.
CSEL2-0  Channel Select. Used in non-terminal mode (SPCR:SPM = 1).
Select one IOM-channel out of 8, where the ICC-B is to receive/transmit.
“000” channel 0 (first channel in IOM-frame)
“001” channel 1
...
“111” channel 7 (last channel in IOM-frame)

ITF  Inter-Frame Time Fill
Selects the inter-frame time fill signal which is transmitted between HDLC-frames.
0: idle (continuous 1 s),
1: flags (sequence of patterns: “0111 1110”)

Note: In TE- and LT-T-applications with D-channel access handling (collision resolution), the only possible inter-frame time fill signal is idle (continuous 1s). Otherwise the D-channel on the S/T-bus cannot be accessed.

4.3.16  Additional Feature Register 2  ADF2  Read/Write  Address 39H

Value after reset: 00H

<p>| | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>IMS</td>
<td>D2C2</td>
<td>D2C1</td>
<td>D2C0</td>
<td>ODS</td>
<td>D1C2</td>
<td>D1C1</td>
</tr>
</tbody>
</table>
IMS
IOM-mode selection
IOM-2 interface mode is selected when IMS = 1.

D2C2-0
Data strobe control; used in IOM-2 mode only.

D1C2-0
These bits determine the polarity of the two independent strobe signals SDS1 and SDS2 as follows:

<table>
<thead>
<tr>
<th>DxC2</th>
<th>DxC1</th>
<th>DxC0</th>
<th>SDSx</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>always low</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>high during B1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>high during B2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>high during B1 + B2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>always low</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>high during IC1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>high during IC2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>high during IC1 + IC2</td>
</tr>
</tbody>
</table>

The strobe signals allow standard combos or data devices to access a programmable channel.

**Note:** In non-terminal mode (SPCR:SPM = 1) IC1, IC2 correspond to B1, B2 channels of the IOM-channel as programmed to ADF1:CSEL 2 - 0 + 1.

ODS
Output driver selection;
Tristate drivers (1) or open drain drivers (0) are used for the IOM-interface.

4.3.17 MONITOR Status Register

MOSR Read Address 3AH

Value after reset: 00H

<table>
<thead>
<tr>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDR1</td>
<td>MER1</td>
</tr>
</tbody>
</table>
MDR1  MONITOR channel 1 Data Received
MER1  MONITOR channel 1 End of Reception
MDA1  MONITOR channel 1 Data Acknowledged
The remote end has acknowledged the MONITOR byte being transmitted.
MAB1  MONITOR channel 1 Data Abort
MDR0  MONITOR channel 0 Data Received
MER0  MONITOR channel 0 End of Reception
MDA0  MONITOR channel 0 Data Acknowledged
The remote end has acknowledged the MONITOR byte being transmitted.
MAB0  MONITOR channel 0 Data Abort

4.3.18 MONITOR Control Register MOCR Write Address 3A\text{H}

Value after reset: 00\text{H}

7 0

\begin{tabular}{cccccccc}
MRE1 & MRC1 & MIE1 & MXC1 & MRE0 & MRC0 & MIE0 & MXC0 \\
\end{tabular}

MRC1,0  MR Bit Control (IOM-channel 1,0)
Determines the value of the MR-bit:
0.. MR always “1”. In addition, the MDR1/MDR0 interrupt is blocked, except for
the first byte of a packet (if MRE 1/0=1).
1.. MR internally controlled by the ICC-B according to MONITOR channel
protocol. In addition, the MDR1/MDR0-interrupt is enabled for all received bytes
according to the MONITOR channel protocol (if MRE1,0=1).

MXC1,0  MX Bit Control (IOM-channel 1,0)
Determines the value of the MX-bit:
0.. MX always “1”.
1.. MX internally controlled by the ICC-B according to MONITOR channel
protocol.

MIE1,0  MONITOR transmit interrupt enable (IOM-channel 1,0)
MONITOR interrupt status MER1/0, MDA1/0, MAB1/0 generation is
enabled (1) or masked (0).

MRE1,0  MONITOR receive interrupt enable (IOM-channel 1,0)
MONITOR interrupt status MDR1/MDR0 generation is enabled (1) or
masked (0).
5 Electrical Characteristics

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage on any pin with respect to ground</td>
<td>$V_S$</td>
<td>$-0.4$ to $V_{DD} + 0.4$</td>
<td>V</td>
</tr>
<tr>
<td>Ambient temperature under bias</td>
<td>$T_A$</td>
<td>0 to 70</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>$T_A$</td>
<td>-40 to 85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td>$-65$ to 125</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note:** Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

PEB 2070: $T_A = 0$ to 70 °C, $V_{DD} = 5$ V, $V_{SS} = 0$ V.
PEF 2070: $T_A = -40$ to 85 °C, $V_{DD} = 5$ V, $V_{SS} = 0$ V.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>L-input voltage</td>
<td>$V_{IL}$</td>
<td>$-0.4$ to $0.8$</td>
<td>V</td>
<td>$I_{OL} = 7$ mA pin IDP0, IDP1</td>
</tr>
<tr>
<td>H-input voltage</td>
<td>$V_{IH}$</td>
<td>2.0 to $V_{DD} + 0.4$</td>
<td>V</td>
<td>$I_{OL} = 2$ mA all other pins</td>
</tr>
<tr>
<td>L-output voltage</td>
<td>$V_{OL}$</td>
<td>$0.45$</td>
<td>V</td>
<td>$I_{OH} = -400$ µA</td>
</tr>
<tr>
<td>H-output voltage</td>
<td>$V_{OH}$</td>
<td>2.4 to $V_{DD} - 0.5$</td>
<td>V</td>
<td>$I_{OH} = -100$ µA</td>
</tr>
<tr>
<td>Power supply current</td>
<td>$I_{CC}$</td>
<td>1.6 to 8.0</td>
<td>mA</td>
<td>DLC: 512 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.5 to 8.0</td>
<td>mA</td>
<td>DLC: 1536 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.0 to 8.0</td>
<td>mA</td>
<td>DLC: 4096 kHz</td>
</tr>
<tr>
<td>Input leakage current</td>
<td>$I_{LI}$</td>
<td>0.6</td>
<td>mA</td>
<td>$V_{DD} = 5$ V inputs at 0 V</td>
</tr>
<tr>
<td>Output leakage current</td>
<td>$I_{LO}$</td>
<td>10</td>
<td>µA</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 &lt; $V_{IN}$, $V_{DD}$ to 0 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 &lt; $V_{OUT}$ &lt; $V_{DD}$ to 0 V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Capacitances

\( T_A = 25^\circ C, \ V_{DD} = 5 \text{ V} \pm 5 \% , \ V_{SS} = 0 \text{ V}, f_C = 1 \text{ MHz}, \) unmeasured pins returned to \( \text{GND} \).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input capacitance</td>
<td>( C_{\text{IN}} )</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Output capacitance ( f_C = 1 \text{ MHz} )</td>
<td>( C_{\text{OUT}} )</td>
<td>8</td>
<td>15</td>
</tr>
<tr>
<td>I/O capacitance ( f_C = 1 \text{ MHz} )</td>
<td>( C_{\text{IO}} )</td>
<td>10</td>
<td>20</td>
</tr>
</tbody>
</table>

AC Characteristics

PEB 2070: \( T_A = 0 \text{ to } 70^\circ C, \ V_{DD} = 5 \text{ V} \pm 5\% \)
PEF 2070: \( T_A = -40 \text{ to } 85^\circ C, \ V_{DD} = 5 \text{ V} \pm 5\% \)

Inputs are driven to 2.4 V for logical “1” and to 0.4 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and 0.8 V for a logical “0”. The AC testing input/output waveforms are shown below.

![Input/Output Waveform and Load Circuit for AC Tests](image)
Microprocessor Interface Timing
Siemens/Intel Bus Mode

Figure 35
μP Write Cycle

Figure 36
μP Write Cycle
Figure 37
Multiplexed Address Timing

Figure 38
Non-Multiplexed Address Timing
Motorola Bus Mode

Figure 39
μP Read Cycle

Figure 40
μP Write Cycle

Figure 41
Address Timing
### Electrical Characteristics

#### Parameter and Values of the Bus Modes

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>min.</td>
<td>max.</td>
</tr>
<tr>
<td>ALE pulse width</td>
<td>$t_{AA}$</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>Address setup time to ALE</td>
<td>$t_{AL}$</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>Address hold time from ALE</td>
<td>$t_{LA}$</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Address latch setup time to $WR, RD$</td>
<td>$t_{ALS}$</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>Address setup time to $WR, RD$</td>
<td>$t_{AS}$</td>
<td>35</td>
<td>ns</td>
</tr>
<tr>
<td>Address hold time from $WR, RD$</td>
<td>$t_{AH}$</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>ALE pulse delay</td>
<td>$t_{AD}$</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>DS delay after R/W setup</td>
<td>$t_{DSD}$</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>RD pulse width</td>
<td>$t_{RR}$</td>
<td>110</td>
<td>ns</td>
</tr>
<tr>
<td>Data output delay from RD</td>
<td>$t_{RD}$</td>
<td></td>
<td>110</td>
</tr>
<tr>
<td>Data float from RD</td>
<td>$t_{DF}$</td>
<td></td>
<td>25</td>
</tr>
<tr>
<td>RD control interval</td>
<td>$t_{RI}$</td>
<td>70</td>
<td>ns</td>
</tr>
<tr>
<td>WR pulse width</td>
<td>$t_{WW}$</td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td>Data setup time to $WR \times CS$</td>
<td>$t_{DW}$</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>Data hold time from $WR \times CS$</td>
<td>$t_{WD}$</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>WR control interval</td>
<td>$t_{WI}$</td>
<td>70</td>
<td>ns</td>
</tr>
</tbody>
</table>
Serial Interface Timing

IOM® Timing

Figure 42
IOM® Timing
### IOM® Mode

#### Parameters and Values of IOM Mode

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOM output data delay</td>
<td>$t_{IOD}$</td>
<td>20</td>
<td>140</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>IOM input data setup</td>
<td>$t_{IIS}$</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>IOM input data hold</td>
<td>$t_{IIH}$</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>IOM output from FSC</td>
<td>$t_{IOF}$</td>
<td></td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>Strobe signal delay</td>
<td>$t_{SDD}$</td>
<td></td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>Strobe delay from FSC</td>
<td>$t_{SDF}$</td>
<td></td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>Frame sync setup</td>
<td>$t_{FSS}$</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Frame sync hold</td>
<td>$t_{FSH}$</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Frame sync width</td>
<td>$t_{FSW}$</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>FSD delay</td>
<td>$t_{FDD}$</td>
<td>20</td>
<td>140</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note:** This delay is applicable in two cases only:

1) When FSC appears for the first time, e.g. at system power-up
2) When FSC appears before the expected start of a frame.
**HDLC Mode**

Figure 43
FSC (Strobe) Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSC set-up time</td>
<td>$t_{FS1}$</td>
<td>100</td>
<td>$t_{CPH} + 70$</td>
</tr>
<tr>
<td>FSC hold time</td>
<td>$t_{FH1}$</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>Output data from high impedance to active</td>
<td>$t_{OZD}$</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>Output data from active to high impedance</td>
<td>$t_{ODZ}$</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>Output data delay from DCL</td>
<td>$t_{ODD}$</td>
<td>20</td>
<td>100</td>
</tr>
<tr>
<td>Input data setup</td>
<td>$t_{IDS}$</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Input data hold</td>
<td>$t_{IDH}$</td>
<td>30</td>
<td></td>
</tr>
</tbody>
</table>
Serial Port A (SSI) Timing

**Figure 44**
SSI Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCA clock delay</td>
<td>$t_{SCD}$</td>
<td>20 140</td>
<td>ns</td>
</tr>
<tr>
<td>SSI data delay</td>
<td>$t_{SSD}$</td>
<td>20 140</td>
<td>ns</td>
</tr>
<tr>
<td>SSI data setup</td>
<td>$t_{SSS}$</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>SSI data hold</td>
<td>$t_{SSH}$</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>Frame sync setup</td>
<td>$t_{FSS}$</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Frame sync hold</td>
<td>$t_{FSH}$</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>Frame sync width</td>
<td>$t_{FSW}$</td>
<td>40</td>
<td>ns</td>
</tr>
</tbody>
</table>
**Electrical Characteristics**

**SLD Timing**

*Figure 45*  
SLD Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLD data delay</td>
<td>$t_{SLD}$</td>
<td>20</td>
<td>140</td>
</tr>
<tr>
<td>SLD data setup</td>
<td>$t_{SLS}$</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>SLD data hold</td>
<td>$t_{SLH}$</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>Frame sync setup</td>
<td>$t_{FSS}$</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>Frame sync hold</td>
<td>$t_{FSH}$</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>Frame sync width</td>
<td>$t_{FSW}$</td>
<td>40</td>
<td></td>
</tr>
</tbody>
</table>
Clock Timing

Figure 46
Definition of Clock Period and Width

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock period</td>
<td>$t_P$</td>
<td>1000</td>
<td>ns</td>
<td>IOM-1</td>
</tr>
<tr>
<td>Clock width high</td>
<td>$t_{WH}$</td>
<td>200</td>
<td>ns</td>
<td>IOM-1</td>
</tr>
<tr>
<td>Clock width low</td>
<td>$t_{WL}$</td>
<td>200</td>
<td>ns</td>
<td>IOM-1</td>
</tr>
<tr>
<td>Clock period</td>
<td>$t_P$</td>
<td>240</td>
<td>ns</td>
<td>IOM-2</td>
</tr>
<tr>
<td>Clock width high</td>
<td>$t_{WH}$</td>
<td>100</td>
<td>ns</td>
<td>IOM-2</td>
</tr>
<tr>
<td>Clock width low</td>
<td>$t_{WL}$</td>
<td>100</td>
<td>ns</td>
<td>IOM-2</td>
</tr>
</tbody>
</table>

Reset

Figure 47
Reset Signal Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit Values</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length of active high state</td>
<td>$t_{RES}$</td>
<td>2 x DCL clock cycles</td>
<td>During power up</td>
</tr>
</tbody>
</table>
6 Package Outlines

Plastic Package, P-DIP-24
(Plastic Dual-In-Line Package)

Plastic Package, P-LCC-28-R (SMD)
(Plastic-Leaded Chip Carrier)

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm