OsmoTRX - Support #3316

osmo-trx-uhd fails after OpenBTS starts, LimeSDR

06/04/2018 01:44 AM - Xhizors

Status:	Closed	**Start date:**	06/04/2018
Priority:	Normal	**Due date:**	
Assignee:		**% Done:**	0%
Category:			
Target version:			
Spec Reference:			

Description

Hello osmocom community, I'm trying to run OpenBTS with LimeSDR-USB v1.4
I installed LimeSuite(v18.04.2), UHD and SoapyUHD(libuhdSupport.so 0.3.4-55da7da) and OSMO-TRX on Ubuntu 18.04 system.
LimeSDR-USB_HW_1.4_r2.16.rbf

After I start the osmo-trx-uhd the transceiver starts, but 1 minute after I start OpenBTS it crashes with "UHD: Device send timed out"

```
# osmo-trx-uhd -C ~/Downloads/osmo-trx-limesdr.cfg

Info: SSE3 support compiled in and supported by CPU
Info: SSE4.1 support compiled in and supported by CPU
Sun Jun  3 05:32:52 2018 DLGLOBAL <0002> telnet_interface.c:104 telnet at 127.0.0.1 4237
Sun Jun  3 05:32:52 2018 DLCTRL <0009> control_if.c:886 CTRL at 127.0.0.1 4236
Config Settings
   Log Level............... 3
   Device args.............
   TRX Base Port........... 5700
   TRX Address............. 127.0.0.1
   GSM BTS Address......... 127.0.0.1
   Channels................ 1
   Tx Samples-per-Symbol... 4
   Rx Samples-per-Symbol... 4
   EDGE support............ 0
   Reference............... 0
   C0 Filler Table......... 1
   Multi-Carrier........... 0
   Tuning offset........... 0
   RSSI to dBm offset...... 0
   Swap channels........... 0
   Tx Antennas............. 'BAND1'
   Rx Antennas............. 'LNAW'

[INFO] [UHD] linux; GNU C++ version 7.3.0; Boost_106501; UHD_3.12.0.0-9-gd19c7590
Sun Jun  3 05:32:53 2018 DMAIN <0000> UHDDevice.cpp:667 [tid=140646755682240] Using discovered UHD
 device addr=1d50:6108,driver=lime,label=LimeSDR-USB [USB 3.0] 9060B00472B27,media=USB 3.0,module=
FX3,name=LimeSDR-USB,serial=0009060B00472B27,type=soapy
[INFO] [UHDSoapyDevice] Make connection: 'LimeSDR-USB [USB 3.0] 9060B00472B27'
[INFO] [UHDSoapyDevice] Reference clock 30.72 MHz
[INFO] [UHDSoapyDevice] Device name: LimeSDR-USB
[INFO] [UHDSoapyDevice] Reference: 30.72 MHz
[INFO] [UHDSoapyDevice] LMS7002M calibration values caching Disable
Sun Jun  3 05:32:55 2018 DMAIN <0000> UHDDevice.cpp:484 [tid=140646755682240] Antennas configured
successfully
Sun Jun  3 05:32:55 2018 DMAIN <0000> UHDDevice.cpp:458 [tid=140646755682240] Rates configured for
 LimeSDR 4 SPS
[INFO] [UHDSoapyDevice] Filter calibrated. Filter order-4th, filter bandwidth set to 6 MHz.Real po
le 1st order filter set to 2.5 MHz. Preemphasis filter not active
[INFO] [UHDSoapyDevice] TX LPF configured
[INFO] [UHDSoapyDevice] RX LPF configured
Sun Jun  3 05:32:56 2018 DMAIN <0000> UHDDevice.cpp:418 [tid=140646755682240] Supported Tx gain ra
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```
nge [-12; 64]
Sun Jun  3 05:32:56 2018 DMAIN <0000> UHDDevice.cpp:423 [tid=140646755682240] Supported Rx gain ra
nge [-12; 61]
Sun Jun  3 05:32:56 2018 DMAIN <0000> UHDDevice.cpp:427 [tid=140646755682240] Default setting Tx g
ain for channel 0 to 26
Sun Jun  3 05:32:56 2018 DMAIN <0000> UHDDevice.cpp:434 [tid=140646755682240] Default setting Rx g
ain for channel 0 to 24.5
Sun Jun  3 05:32:57 2018 DMAIN <0000> UHDDevice.cpp:761 [tid=140646755682240]
Single USRP:
  Device: FX3
  Mboard 0: LimeSDR-USB
  RX Channel: 0
    RX DSP: 0
    RX Dboard: 0
    RX Subdev: SoapyRF
  RX Channel: 1
    RX DSP: 1
    RX Dboard: 1
    RX Subdev: SoapyRF
  TX Channel: 0
    TX DSP: 0
    TX Dboard: 0
    TX Subdev: SoapyRF
  TX Channel: 1
    TX DSP: 1
    TX Dboard: 1
    TX Subdev: SoapyRF
-- Transceiver active with 1 channel(s)
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is POWEROF
F
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is READFAC
TORY sdrsn
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:836 [tid=140646755919616] bogus command READ
FACTORY sdrsn on control interface.
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is RXTUNE
900200
Sun Jun  3 05:36:54 2018 DMAIN <0000> UHDDevice.cpp:1149 [tid=140646755919616]
Tune Result:
    Target RF  Freq: 900.200000 (MHz)
    Actual RF  Freq: 900.199995 (MHz)
    Target DSP Freq: -0.000005 (MHz)
    Actual DSP Freq: -0.000005 (MHz)

Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is TXTUNE
945200
Sun Jun  3 05:36:54 2018 DMAIN <0000> UHDDevice.cpp:1149 [tid=140646755919616]
Tune Result:
    Target RF  Freq: 945.200000 (MHz)
    Actual RF  Freq: 945.199995 (MHz)
    Target DSP Freq: 0.000005 (MHz)
    Actual DSP Freq: 0.000005 (MHz)

Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETTSC
2
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:811 [tid=140646755919616] Changing TSC from
0 to 2
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETMAXD
LY 4
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETRXGA
IN 47
Sun Jun  3 05:36:54 2018 DMAIN <0000> UHDDevice.cpp:532 [tid=140646755919616] Set RX gain to 47dB
(asked for 47dB)
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is POWERON
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:238 [tid=140646755919616] Starting the trans
ceiver
Sun Jun  3 05:36:54 2018 DMAIN <0000> radioInterface.cpp:168 [tid=140646755919616] Starting radio
device
```

```
Sun Jun  3 05:36:54 2018 DMAIN <0000> UHDDevice.cpp:839 [tid=140646755919616] Starting USRP...
[INFO] [UHDSoapyDevice] Tx calibration finished
[FATAL] [UHDSoapyDevice] Rx Calibration: Frequency out of range, available range: from 2.5 to 120 MHz
Sun Jun  3 05:36:54 2018 DMAIN <0000> UHDDevice.cpp:814 [tid=140646755919616] Initial timestamp 128520
Sun Jun  3 05:36:54 2018 DMAIN <0000> UHDDevice.cpp:860 [tid=140646755919616] The current time is 0.119575 seconds
Sun Jun  3 05:36:54 2018 DMAIN <0000> radioInterface.cpp:189 [tid=140646755919616] Radio started
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETPOWER 10
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:1018 [tid=140646755845888] ClockInterface: sending IND CLOCK 46656
Sun Jun  3 05:36:54 2018 DMAIN <0000> UHDDevice.cpp:517 [tid=140646755919616] Set TX gain to 52dB (asked for 54dB)
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETSLOT 0 5
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:376 [tid=140646755882752] chan 0 dumping STALE burst in TRX->USRP interface (0:46656 vs 3:46658), retrans=0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:376 [tid=140646755882752] chan 0 dumping STALE burst in TRX->USRP interface (0:46681 vs 3:46681), retrans=0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:376 [tid=140646755882752] chan 0 dumping STALE burst in TRX->USRP interface (0:46691 vs 7:46691), retrans=0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:376 [tid=140646755882752] chan 0 dumping STALE burst in TRX->USRP interface (0:46701 vs 3:46702), retrans=0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:376 [tid=140646755882752] chan 0 dumping STALE burst in TRX->USRP interface (0:46702 vs 3:46702), retrans=0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETSLOT 1 1
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 1
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 1
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETSLOT 2 1
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 2
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 2
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETSLOT 3 1
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 3
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDOVER 3
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Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETSLOT
 4 1
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDO
VER 4
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDO
VER 4
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETSLOT
 5 1
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDO
VER 5
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDO
VER 5
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETSLOT
 6 1
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDO
VER 6
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDO
VER 6
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETSLOT
 7 1
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDO
VER 7
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is NOHANDO
VER 7
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:709 [tid=140646755919616] command is SETPOWE
R 10
Sun Jun  3 05:36:54 2018 DMAIN <0000> UHDDevice.cpp:517 [tid=140646755919616] Set TX gain to 52dB
(asked for 54dB)
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:376 [tid=140646755882752] chan 0 dumping STA
LE burst in TRX->USRP interface (0:46732 vs 7:46732), retrans=0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:376 [tid=140646755882752] chan 0 dumping STA
LE burst in TRX->USRP interface (1:46748 vs 3:46748), retrans=0
Sun Jun  3 05:36:54 2018 DMAIN <0000> Transceiver.cpp:376 [tid=140646755882752] chan 0 dumping STA
LE burst in TRX->USRP interface (1:46752 vs 3:46752), retrans=0
...
Sun Jun  3 05:36:55 2018 DMAIN <0000> Transceiver.cpp:376 [tid=140646755882752] chan 0 dumping STA
LE burst in TRX->USRP interface (5:46869 vs 7:46869), retrans=0
Sun Jun  3 05:36:55 2018 DMAIN <0000> Transceiver.cpp:376 [tid=140646755882752] chan 0 dumping STA
LE burst in TRX->USRP interface (6:46869 vs 7:46869), retrans=0
Sun Jun  3 05:36:55 2018 DMAIN <0000> Transceiver.cpp:1018 [tid=140646755845888] ClockInterface: s
ending IND CLOCK 46872
...
Sun Jun  3 05:36:56 2018 DMAIN <0000> Transceiver.cpp:1018 [tid=140646755845888] ClockInterface: s
ending IND CLOCK 47089
Sun Jun  3 05:36:57 2018 DMAIN <0000> Transceiver.cpp:1018 [tid=140646755845888] ClockInterface: s
ending IND CLOCK 47306
Sun Jun  3 05:36:58 2018 DMAIN <0000> Transceiver.cpp:1018 [tid=140646755845888] ClockInterface: s
ending IND CLOCK 47522
Sun Jun  3 05:36:59 2018 DMAIN <0000> Transceiver.cpp:1018 [tid=140646755845888] ClockInterface: s
ending IND CLOCK 47739
[WARNING] [UHDSoapyDevice] L
[WARNING] [UHDSoapyDevice] L
Sun Jun  3 05:37:40 2018 DMAIN <0000> Transceiver.cpp:1018 [tid=140646755845888] ClockInterface: s
ending IND CLOCK 56630
Sun Jun  3 05:37:41 2018 DMAIN <0000> Transceiver.cpp:1018 [tid=140646755845888] ClockInterface: s
ending IND CLOCK 56847
Sun Jun  3 05:37:42 2018 DMAIN <0000> Transceiver.cpp:1018 [tid=140646755845888] ClockInterface: s
ending IND CLOCK 57063
Sun Jun  3 05:37:43 2018 DMAIN <0000> UHDDevice.cpp:1071 [tid=140646755882752] UHD: Device send ti
med out
Sun Jun  3 05:37:43 2018 DMAIN <0000> UHDDevice.cpp:1071 [tid=140646755882752] UHD: Device send ti
med out
Sun Jun  3 05:37:43 2018 DMAIN <0000> UHDDevice.cpp:1071 [tid=140646755882752] UHD: Device send ti
med out
```

Also configured osmo-trx-lms and osmo-trx but cant seem to start the transceiver with them:

```
# osmo-trx -e -a “driver=lime,device=0”
linux; GNU C++ version 7.3.0; Boost_106501; UHD_003.010.003.000-0-unknown

opening configuration table from path :memory:
Config Settings
   Log Level.............. NOTICE
   Device args............ “driver=lime,device=0”
   TRX Base Port.......... 5700
   TRX Address............ 127.0.0.1
   Channels............... 1
   Tx Samples-per-Symbol... 4
   Rx Samples-per-Symbol... 4
   EDGE support........... Enabled
   Reference.............. Internal
   C0 Filler Table........ Disabled
   Multi-Carrier.......... Disabled
   Diversity.............. Disabled
   Tuning offset.......... 0
   RSSI to dBm offset..... 0
   Swap channels.......... 0

Exception in static block reg_basic_and_lf_dboards
  LookupError: KeyError: The dboard id 0x0000 is already registered to Basic TX.
Exception in static block reg_rfx_dboards
  LookupError: KeyError: The dboard id pair [0x0024, 0x0028] is already registered to RFX400.
Exception in static block reg_xcvr2450_dboard
  LookupError: KeyError: The dboard id pair [0x0061, 0x0060] is already registered to XCVR2450.
Exception in static block reg_sbx_dboards
  LookupError: KeyError: The dboard id pair [0x0054, 0x0055] is already registered to SBX.
Exception in static block reg_ubx_dboards
  LookupError: KeyError: The dboard id pair [0x0074, 0x0073] is already registered to UBX v0.3.
Exception in static block reg_wbx_simple_dboards
  LookupError: KeyError: The dboard id pair [0x0053, 0x0052] is already registered to WBX.
Exception in static block reg_dbsrx_dboard
  LookupError: KeyError: The dboard id 0x000d is already registered to DBSRX.
Exception in static block reg_unknown_dboards
  LookupError: KeyError: The dboard id 0xfff0 is already registered to Unknown TX.
Exception in static block reg_tvrx_dboard
  LookupError: KeyError: The dboard id 0x0040 is already registered to TVRX.
Exception in static block reg_dbsrx2_dboard
  LookupError: KeyError: The dboard id 0x0012 is already registered to DBSRX2.
Exception in static block reg_tvrx2_dboard
  LookupError: KeyError: The dboard id 0x0046 is already registered to TVRX2.
Exception in static block reg_twinrx_dboards
  LookupError: KeyError: The dboard id 0x0091 is already registered to TwinRX Rev A.
double free or corruption (out)[
INFO] [UHD] Aborted (core dumped)
```

and with osmo-trx-lms:

```
# osmo-trx-lms -C ~/Downloads/osmo-trx-limesdr.cfg
Info: SSE3 support compiled in and supported by CPU
Info: SSE4.1 support compiled in and supported by CPU
Mon Jun  4 04:29:37 2018 DLGLOBAL <0002> telnet_interface.c:104 telnet at 127.0.0.1 4237
Mon Jun  4 04:29:37 2018 DLCTRL <0009> control_if.c:886 CTRL at 127.0.0.1 4236
Config Settings
   Log Level.............. 3
   Device args.............
   TRX Base Port.......... 5700
   TRX Address............ 127.0.0.1
   GSM BTS Address........ 127.0.0.1
```

```
   Channels................. 1
   Tx Samples-per-Symbol... 4
   Rx Samples-per-Symbol... 4
   EDGE support............. 0
   Reference................ 0
   C0 Filler Table......... 1
   Multi-Carrier............ 0
   Tuning offset............ 0
   RSSI to dBm offset...... 0
   Swap channels............ 0
   Tx Antennas.............. 'BAND1'
   Rx Antennas.............. 'LNAW'

Mon Jun  4 04:29:37 2018 DMAIN <0000> LMSDevice.cpp:46 [tid=140364825490368] creating LMS device..
.
Mon Jun  4 04:29:37 2018 DMAIN <0000> LMSDevice.cpp:96 [tid=140364825490368] Opening LMS device..
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] Estimated reference cl
ock 30.6588 MHz
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] Reference clock 30.72
MHz
Mon Jun  4 04:29:37 2018 DMAIN <0000> LMSDevice.cpp:123 [tid=140364825490368] Init LMS device
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] INT 158, FRAC 797354,
DIV_LOCH 1, EN_DIV2_DIVPROG 0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCO 5000.00 MHz, RefCl
k 30.72 MHz
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] ICT_VCO: 180
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=64    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=96    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=112    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=120    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=124    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=126    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=127    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] Failed to lock
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=192    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=224    cmphl=2
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=240    cmphl=3
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=232    cmphl=3
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=228    cmphl=3
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=226    cmphl=3
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=225    cmphl=3
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] Failed to lock
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] cmphl=2
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCOL : csw=221 tune ok
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] ICT_VCO: 180
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] TuneVCO(SXT) - VCO too
 high
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCOM : csw=0 tune fail
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] ICT_VCO: 180
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] TuneVCO(SXT) - VCO too
 high
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCOH : csw=0 tune fail
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] Selected: VCOL
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] INT 152, FRAC 262144,
DIV_LOCH 1, EN_DIV2_DIVPROG 0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCO 4800.00 MHz, RefCl
k 30.72 MHz
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] ICT_VCO: 180
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=64    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=96    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=112    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=120    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=124    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=126    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=127    cmphl=0
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] Failed to lock
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=192    cmphl=0
```

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Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=224    cmphl=3
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=208    cmphl=3
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=200    cmphl=2
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=204    cmphl=3
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=202    cmphl=3
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw=201    cmphl=3
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] Failed to lock
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] cmphl=2
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCOL : csw=198 tune ok
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] ICT_VCO: 180
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] TuneVCO(SXR) - VCO too
 high
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCOM : csw=0 tune fail
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] ICT_VCO: 180
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] TuneVCO(SXR) - VCO too
 high
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCOH : csw=0 tune fail
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] Selected: VCOL
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] INT 77, FRAC 131072, D
IV_OUTCH_CGEN 14
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCO 2400.00 MHz, RefCl
k 30.72 MHz
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw 169; interval [166
, 172]
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] INT 77, FRAC 131072, D
IV_OUTCH_CGEN 14
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCO 2400.00 MHz, RefCl
k 30.72 MHz
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw 169; interval [166
, 172]
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] M=195, N=3, Fvco=1300.
000 MHz
Mon Jun  4 04:29:37 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] M=195, N=3, Fvco=1300.
000 MHz
Mon Jun  4 04:29:38 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] INT 71, FRAC 233016, D
IV_OUTCH_CGEN 7
Mon Jun  4 04:29:38 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCO 2218.67 MHz, RefCl
k 30.72 MHz
Mon Jun  4 04:29:38 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw 129; interval [125
, 133]
Mon Jun  4 04:29:38 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] INT 71, FRAC 233016, D
IV_OUTCH_CGEN 7
Mon Jun  4 04:29:38 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCO 2218.67 MHz, RefCl
k 30.72 MHz
Mon Jun  4 04:29:38 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw 129; interval [125
, 133]
Mon Jun  4 04:29:38 2018 DMAIN <0000> LMSDevice.cpp:179 [tid=140364825490368] Setting LPFBW chan 0
Mon Jun  4 04:29:38 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] MCU algorithm time: 10
 ms
Mon Jun  4 04:29:38 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] MCU algorithm time: 0
ms
Mon Jun  4 04:29:38 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] MCU Ref. clock: 30.72
MHz
Mon Jun  4 04:29:38 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] MCU algorithm time: 0
ms
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] MCU algorithm time: 20
5 ms
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] RX LPF configured
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] INT 75, FRAC 0, DIV_OU
TCH_CGEN 18
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCO 2334.72 MHz, RefCl
k 30.72 MHz
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw 155; interval [152
, 159]
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] MCU algorithm time: 0
ms
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] MCU algorithm time: 0
```

```
ms
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] MCU Ref. clock: 30.72
MHz
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] MCU algorithm time: 0
ms
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] MCU algorithm time: 70
 ms
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] INT 75, FRAC 0, DIV_OU
TCH_CGEN 18
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] VCO 2334.72 MHz, RefCl
k 30.72 MHz
Mon Jun  4 04:29:39 2018 DLMS <0001> LMSDevice.cpp:71 [tid=140364825490368] csw 155; interval [152
, 159]
Mon Jun  4 04:29:39 2018 DMAIN <0000> LMSDevice.cpp:198 [tid=140364825490368] Error in LMS open, c
losing:
Mon Jun  4 04:29:39 2018 DMAIN <0000> osmo-trx.cpp:446 [tid=140364825490368] Failed to create radi
o device
Shutting down transceiver...
```

I'm stuck at this point and feels too close to actually start over with older versions. If someone has any input on this issue, please share your thoughts.
Cheers

Related issues:

Related to OsmoTRX - Feature #2919: Native LimeSDR support	**Resolved**	**02/09/2018**
Is duplicate of OsmoTRX - Bug #2723: osmo-trx-uhd: failure to update CLOCK IN...	**New**	**12/08/2017**

History

#1 - 06/04/2018 11:56 AM - fixeria

OpenBTS is not a part of Osmocom project. OsmoTRX was forked from there, and backward compatibility is not guaranteed.
In Osmocom, there is OsmoBTS. Probably, you meant exactly OsmoBTS.

In any case, LimeSDR is not (yet) supported by OsmoTRX, and this hardware works fairly unstable itself.
Please see: https://osmocom.org/issues/2919

#2 - 06/04/2018 01:25 PM - Y2Kot

fixeria wrote:

> OpenBTS is not a part of Osmocom project. OsmoTRX was forked from there, and backward compatibility is not guaranteed.
> In Osmocom, there is OsmoBTS. Probably, you meant exactly OsmoBTS.
>
> In any case, LimeSDR is not (yet) supported by OsmoTRX, and this hardware works fairly unstable itself.
> Please see: https://osmocom.org/issues/2919

Also as

Xhizors wrote:

> Hello osmocom community, I'm trying to run OpenBTS with LimeSDR-USB v1.4
> I installed LimeSuite(v18.04.2), UHD and SoapyUHD(libuhdSupport.so 0.3.4-55da7da) and OSMO-TRX on Ubuntu 18.04 system.
> LimeSDR-USB_HW_1.4_r2.16.rbf
>
> After I start the osmo-trx-uhd the transceiver starts, but 1 minute after I start OpenBTS it crashes with "UHD: Device send timed out"
> [...]

Also configured osmo-trx-lms and osmo-trx but cant seem to start the transceiver with them:

[...]

and with osmo-trx-lms:
[...]

I'm stuck at this point and feels too close to actually start over with older versions. If someone has any input on this issue, please share your thoughts.
Cheers

For possible fix you can try to read https://discourse.myriadrf.org/t/limesdr-report-module-as-fx3-instead-of-stream/2529/10
Lime dev advise to use older version of their suite (17.12 is the most stable as for me) and wait before osmo-trx-lms will be complete.

#3 - 06/12/2018 04:30 PM - pespin

- Is duplicate of Bug #2723: osmo-trx-uhd: failure to update CLOCK IND, timeout with LimeSDR added

#4 - 06/12/2018 04:30 PM - pespin

- Related to Feature #2919: Native LimeSDR support added

#5 - 06/12/2018 04:31 PM - pespin

- Status changed from New to Closed

Closing as LimeSDR issues with UHD are being already handled in #2723 and Native LimeSDR status is reported in #2919.