osmo-clock-gen - Bug #3857

Use SAMD XOSC / PLL / GCLK to allow lower reference frequencies

03/24/2019 10:36 AM - laforge

Status:	Resolved	**Start date:**	03/24/2019
Priority:	Normal	**Due date:**	
Assignee:	mschramm	**% Done:**	100%
Category:			
Target version:	hw-v2		
Spec Reference:			

Description

Dieter has suggested a feature to allow using a reference clock at lower frequencies, such as 1MHz.

This is too low to use as an input directly into the Si5351C. However, the XOSC of the SAMD allows for input frequencies down to 400kHz. The crystal oscillator can also be disabled, allowing logig-level clock input. Internal fractional PLL can be used to generate a clock up to 96 MHz from it, and that clocks can then be output via a GCLK block on any of the GCLK_IO pins.

The resulting output could be routed to the secondary input of the Si5351C. This way, we could support e.g. multiplying from 1 MHz to 10 MHz in the SAMD, and then drive the Si5351C as we would with a direct 10MHz reference.

I of course don't know how good the phase noise of the SAMD internal PLL is...

Related issues:

Precedes osmo-clock-gen - Feature #3858: Make more GPIOs avaliable for future...	**Resolved**	**03/25/2019**	**03/25/2019**

History

#1 - 03/24/2019 10:37 AM - laforge

- Target version set to hw-v2

#2 - 03/24/2019 03:51 PM - horiz0n

Additional information on what the clock chip can actually achieve is available at

http://www.simonsdialogs.com/2018/11/si5351a-any-frequency-cmos-clock-generator-and-vco-specifications-myths-and-truth/
http://www.simonsdialogs.com/2018/11/si5351a-u-blox-m7-clock-generator-tests/

#3 - 04/06/2019 04:37 PM - laforge

- Status changed from New to In Progress

- % Done changed from 0 to 10

Most likely candidate is a ATSAMD21E18A-MUT which is in QFN-32 package (current: QFN-24) and has 256k flash and 32kBytes of RAM. It's readily available from e.g.Digikey in large volume.

#4 - 05/10/2019 09:37 AM - laforge

- Assignee changed from laforge to mschramm

#5 - 05/15/2019 06:51 PM - mschramm

- Precedes Feature #3858: Make more GPIOs avaliable for future use added

#6 - 05/29/2019 07:43 PM - mschramm

- Status changed from In Progress to Resolved

- % Done changed from 10 to 100

XA input of Si5351C is now connected to Cortex' PA10, which also can be GCLK_IO4. They are connected via a series resistor and a voltage divider of 47k/30k , as the XA input has V_max = 1,3V. Those two resistors are already in the BOM, and they give 1,286V at 3V3 input. The series resistor ahead of 47k might get little bigger than 0R.

#7 - 06/13/2019 02:26 PM - laforge

- Status changed from Resolved to In Progress

- % Done changed from 100 to 70

It looks like only the XA output is connected to the Si5351C, but the XOSC input part on the SAMD has not been implemented.

#8 - 06/13/2019 03:54 PM - mschramm

PA14 is XIN, and is already routed to the GPIO expansion header (see #3858). As discussed with laforge, we simply don't have more PCB space for adding a RF-grade connector. maximum frequency on that pad is 32 MHz, so I think this is acceptable.

All external connections on this header and on UEXT will get additional TVS diodes added.

#9 - 06/18/2019 03:31 PM - mschramm

- Status changed from In Progress to Resolved

- % Done changed from 70 to 100

(all TVS diodes placed)