osmo-clock-gen - Feature #3905

allow user to supply different output voltage

04/06/2019 05:50 PM - laforge

Status:	Resolved	**Start date:**	04/06/2019
Priority:	Normal	**Due date:**	
Assignee:	mschramm	**% Done:**	100%
Category:			
Target version:			

Description

The Silabs chip allows to generate clock outputs in different voltage domains, let's make this capability available to the user, at least via some jumpers so he can provide another external voltage reference.

History

#1 - 05/08/2019 03:12 PM - laforge

- Assignee changed from laforge to mschramm

#2 - 05/19/2019 07:16 PM - laforge

- Status changed from New to In Progress

- % Done changed from 0 to 30

please make sure to keep the ticket updated. latest idea here was to

- have jumpers in-line of two of the four output banks of the PLL chipc
- jumper closed: reference is drawn from one (shared) "other voltage" LDO onboard
- jumper open: reference voltage can be provided/injected by user from external reference

What's still open to discuss is whether or not the LDO will be fixed (you have to change resistors to change the voltage) or adjustable. In the latter case, we'd apply the DAC output of the SAMD21 as an input to the tracking input of the LDO. However, this would mean that we'd no longer have the DAC output for driving a VCTCXO.

#3 - 05/29/2019 06:58 PM - mschramm

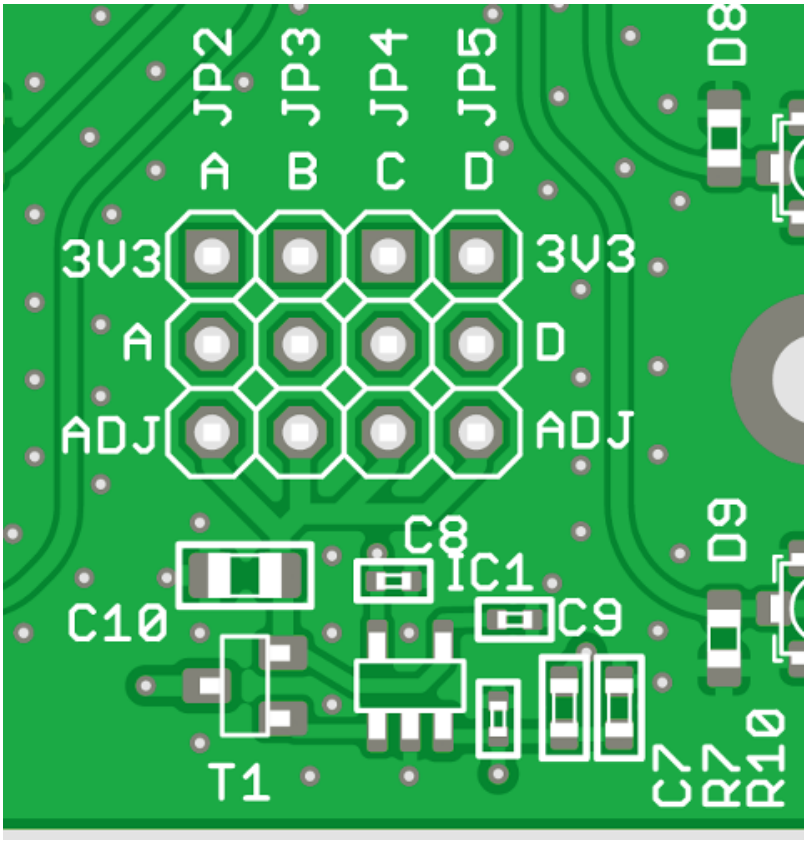
- File clockgen-VDDIO.png added

- Status changed from In Progress to Resolved

- % Done changed from 30 to 100

after discussion on the RFC mail from laforge, a single R2R / single supply / unity gain stable opamp w/ BJT follower was selected. This buffer stage gets its input voltage from PA02 (VOUT, formerly used for the trim voltage for VCTCXO). A 3 by 4 jumper block allows each PLL's VDDIO{A..D} to be jumpered to fixed 3V3 or the adjustable voltage.

The buffer stage has a weak PD (suggested 100k) on it's input to avoid spikes during power-on as long as the Cortex is not initialized (and e.g. a 1V8 sink is connected). This should not be needed as PULLEN bit is 0 at reset.
I'm aware that this forms a voltage divider together with the input wire's resistance.



Files

clockgen-VDDIO.png	125 KB	05/29/2019	mschramm